

Backside-Illuminated 4-T Pinned Avalanche Photodiode Pixel for Readout Noise-Limited Applications

Tomislav Resetar^{1,2}, Koen De Munck², Luc Haspeslagh², Piet De Moor², Paul Goetschalckx², Robert Puers^{1,2}, and Chris Van Hoof^{1,2}

¹KU Leuven, ESAT, 3001 Leuven, Belgium

²IMEC, 3001 Leuven, Belgium

Tel: +32 16 28 16 52, e-mail: Tomislav.Resetar@imec.be

Abstract—A novel pixel concept utilizing a backside-illuminated pinned avalanche photodiode (PAPD) manufactured in 130 nm minimally modified CMOS and operated by a standard four-transistor CMOS Image Sensor (CIS) readout is presented. This concept explores the possibility to increase the SNR by avalanche amplification in the low-light regime for applications that are limited by higher readout noise levels, e.g. high speed and global shutter. Customized avalanche junction implants were optimized and full pixel operation including pinning, light integration and charge transfer at -40 V substrate bias for a multiplication factor of 2–4 was simulated in 2D TCAD. Test arrays of 8x32 pixels with 5 and 10 μm pitch and fully-isolated on-chip CMOS readout were designed. Preliminary experimental results of avalanche and punch-through breakdowns on test-diodes show good agreement with TCAD simulations.

I. INTRODUCTION

Modern CMOS image sensors using 4-transistor (4-T) pixels have very low readout noise levels generally below 3 electrons rms [1], nevertheless, if operated in global-shutter mode or at high speeds, readout noise levels typically increase [2], [3]. Avalanche photodiodes (APDs) in linear mode are used because of their charge multiplication capability and wide bandwidth. However, due to the inherent noisiness of their amplification mechanism, their benefit needs to be evaluated in the overall SNR of the detection chain. The contribution of the avalanche noise is commonly described by the avalanche noise factor F which is an increasing function of the avalanche gain G [4]. For the proposed pixel concept, an optimum gain for maximum SNR improvement between 2 and 4 is predicted. Fig. 1 illustrates pixel SNR improvements calculated from expression (1) in low-light conditions for $G = 3$, $F = 2.1$ and different readout noise levels σ_R , as derived in [5]. 2D arrays of APDs typically suffer from poor fill-factors since each pixel utilizes a guard-ring for premature edge breakdown prevention and complex in-pixel amplifiers [6]. In that light, the goal of this work is to explore the possibility of benefiting from avalanche signal amplification while retaining as many advantages of standard compact 4-T CIS pixel design (e.g. good optical properties, dynamic range, CDS capability etc.)

$$SNR = \frac{GN}{\sqrt{G^2 F(N + D_A) + D_N + \sigma_R^2}} \quad (1)$$

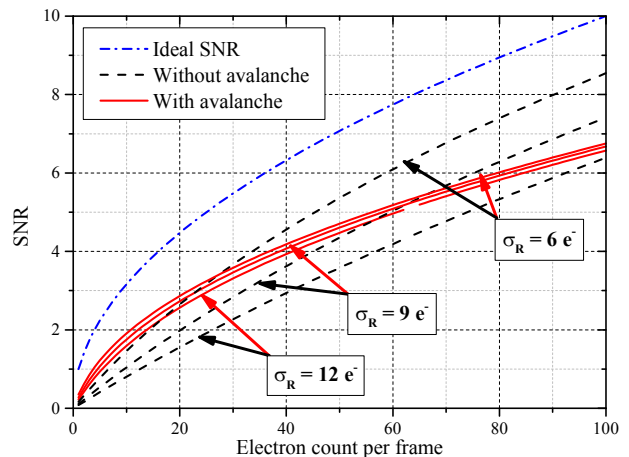


Fig. 1. SNR with and without avalanche amplification.

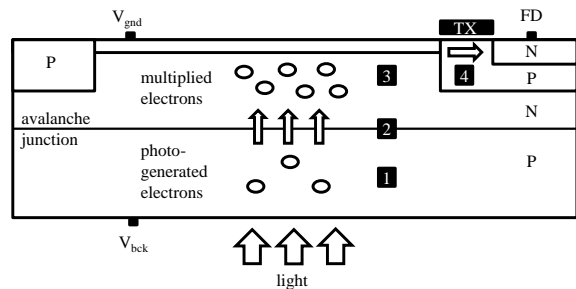


Fig. 2. 4-T PAPD pixel concept description in four main phases: 1 – light absorption, 2 – electron amplification, 3 – collection and 4 – transfer.

II. PIXEL CONCEPT DESCRIPTION

A simplified 2D cross-section of the 4-T PAPD pixel is shown in Fig. 2 [7]. The corresponding doping profile obtained from TCAD is presented in Fig. 3. The top part of the pixel operates in the same manner as a regular pinned photodiode, whereas the bottom part contains a reversely-biased p-n junction for electron amplification which is shared by the complete pixel array. This junction is formed by high-energy p-well and n-well implants added to the CIS process flow.

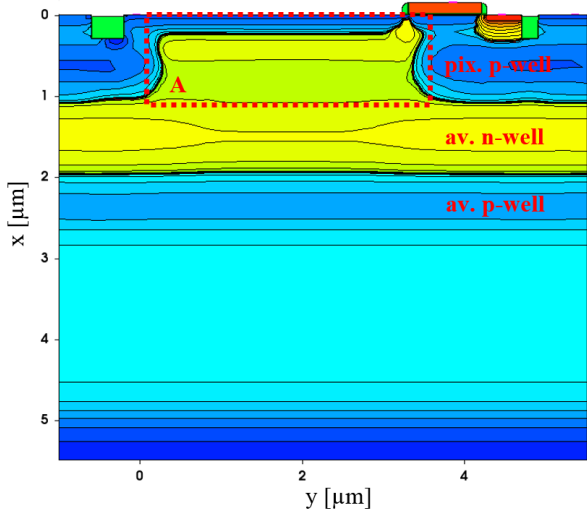


Fig. 3. 2D pixel doping profile obtained from TCAD.

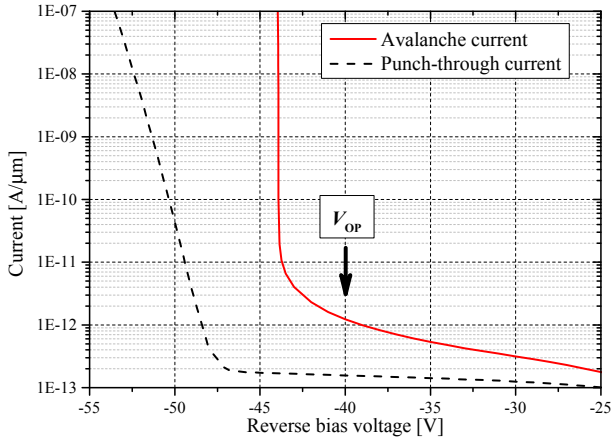


Fig. 4. Simulated avalanche and punch-through current of the p-n-p structure (along the cross-section X_2 in Fig. 6).

The purpose of the avalanche p-well implant is to bring the pixel avalanche breakdown voltage V_{avbd} below the avalanche breakdown of the readout part of the chip. The upper limit for the avalanche p-well dose is set by the demand for full depletion of the p-type epitaxial layer in the vicinity of V_{avbd} in order to avoid potential barriers on the charge-collection path from the backside. This ultimately determines the lowest possible V_{avbd} to approximately -35 V, finally dependent on the epitaxial layer properties e.g. doping concentration and thickness.

On one hand, the upper value of the avalanche n-well dose is primarily determined by the demand for full depletion of the pixel n-type region close to the V_{avbd} for kTC noise elimination. On the other hand, the doping concentration in the n-type region needs to be high enough to prevent the punch-through current from pixel p-well to the negatively-biased substrate. The punch-through breakdown is very sensitive to the avalanche n-well dose, making it one of the most important parameters in the pixel design. As an example, Fig. 4 shows the positions of both breakdown voltages obtained from TCAD and the corresponding operating voltage V_{OP} for one set of doping conditions. For a given V_{avbd} , the multiplication factor G can be estimated by a well-known expression (2) [8]. By taking a typical value of $n = 4$ [6],

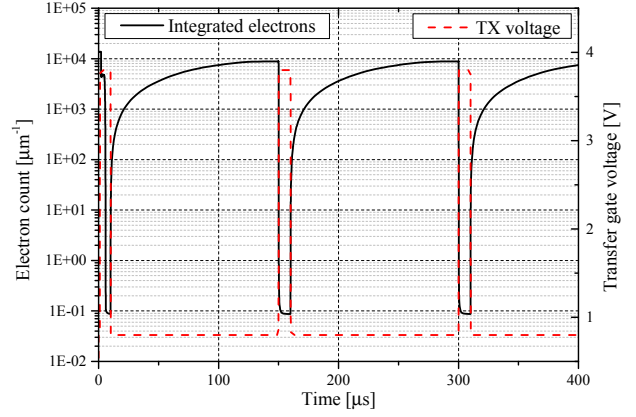


Fig. 5. Electron count in the photodiode area A shown in Fig. 3 (left) and the transfer gate voltage (right) throughout several cycles of operation.

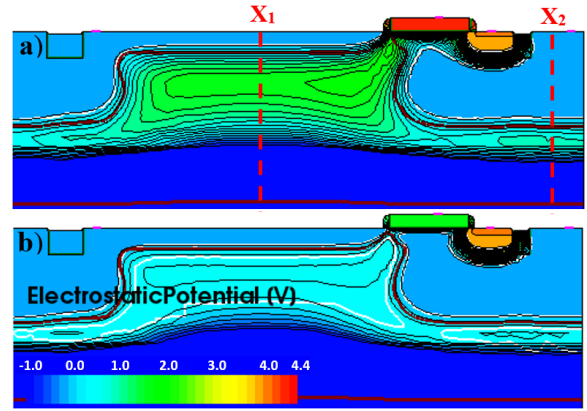


Fig. 6. 2D electrostatic potential profile a) empty pixel b) full pixel.

it can be calculated that for $G = 3$, the operating voltage V_{OP} needs to be 10 % below the breakdown voltage of the avalanche junction V_{avbd} .

$$G = \left[1 - \left(\frac{V_{bck}}{V_{avbd}} \right)^n \right]^{-1} \quad (2)$$

Complete simulation of the pixel operation is presented in Fig 5, showing several light integration cycles where the pixel operates between pinning and saturation. The 2D electrostatic potential distribution in the pixel empty state is shown in Fig. 6a and the corresponding 1D cuts X_1 and X_2 are presented as dashed lines in Fig. 7. Fig. 6b and the full lines in Fig. 7 describe the electrostatic potential in the pixel full state. The maximum electrostatic potential values are 1.5 V in the collection region and around 0.5 V underneath the pixel p-well, resulting in isolation between the neighboring pixels. It is important to note that, at saturation, the pixel is closest to the punch-through breakdown because of the drop of the potential barriers. For that reason, optimization of the avalanche n-well implant together with an efficient anti-blooming mechanism by transfer-gate leakage is required to keep the potential barriers in the n-type region above $\Delta V_{min} = 0.5$ V. Full-well capacity can be estimated to approximately 3×10^4 electrons for a $5 \times 5 \mu\text{m}$ pixel, dependent on the collection area in a particular layout.

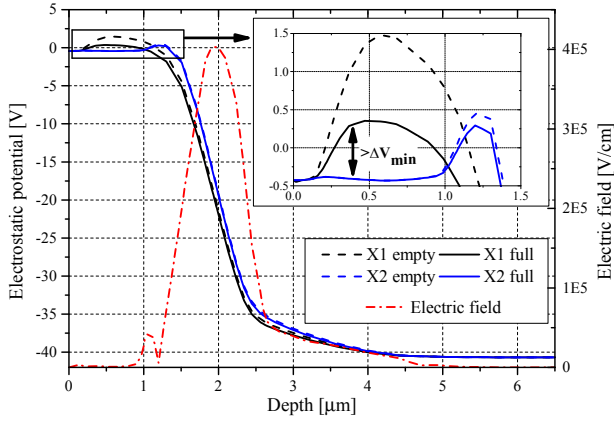


Fig. 7. Electrostatic potential cross sections from Fig. 6 (left) with the corresponding electric field profile (right).

Besides the expected SNR improvement in the low-light regime, two additional benefits can be expected from the BSI 4-T PAPD pixel concept – (1) good optical properties in terms of modulation-transfer function (MTF) and quantum efficiency (QE), originating from the full-depletion of the epitaxial layer and (2) high-speed collection of the photo-generated carriers originating from the high electric field of the avalanche junction. It can be estimated from TCAD that a carrier generated at the backside travels to the collection region *A* in Fig. 3 in a sub-nanosecond time-frame.

III. TEST CHIP AND RESULTS

A test-chip with test-structures and variations of 8x32 pixel test arrays was designed in order to experimentally evaluate the pixel performance. Two pixels are sharing one floating-diffusion (FD) node and are intended for rolling-shutter readout. One variation of the pixel design is shown in Fig. 8. It can be seen that there is a trade-off between the pixel p-well area, which is the region with the highest electric field that is mainly contributing to avalanche multiplication, and the PAPD collection area, which determines the full-well capacity. From the technology perspective, patterning of the high-energy avalanche n-well is needed for the formation of the PAPD collection area. For that reason a thick photoresist with a sufficient aspect-ratio is utilized imposing the limit for further scaling of the presented pixel concept. A snapshot of a pixel test-array layout is given in Fig. 9. Since all pixels share the same avalanche wells, guard-rings for premature edge breakdown prevention were implemented only at the edges of the pixel arrays.

The readout of the pixel array was designed in 130 nm 3.3 V CMOS technology with several design rule adaptations. Fig. 10 represents a schematic description of the readout isolation and the pixel array guard-ring. Most importantly, all electronics need to be isolated in separate deep n-well islands and sufficient spacing of all wells with large potential differences has to be foreseen. Moreover, electrostatic discharge (ESD) protection needs to be designed in order to allow high negative voltages on the bulk of the chip. It was experimentally verified that for both NMOS and PMOS, the transistor characteristics are invariant to the applied negative voltage. The avalanche breakdown of the deep-nwell to substrate was measured to be -80 V. Measurement results on test structures with

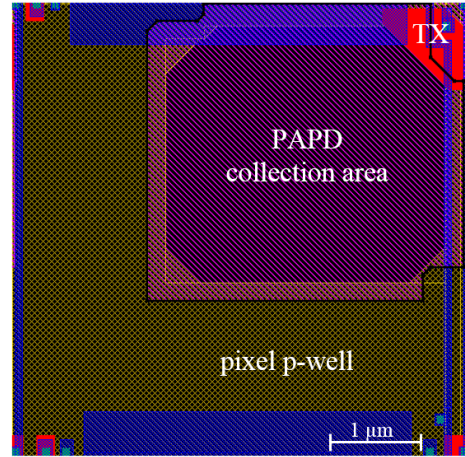


Fig. 8. Pixel layout example.

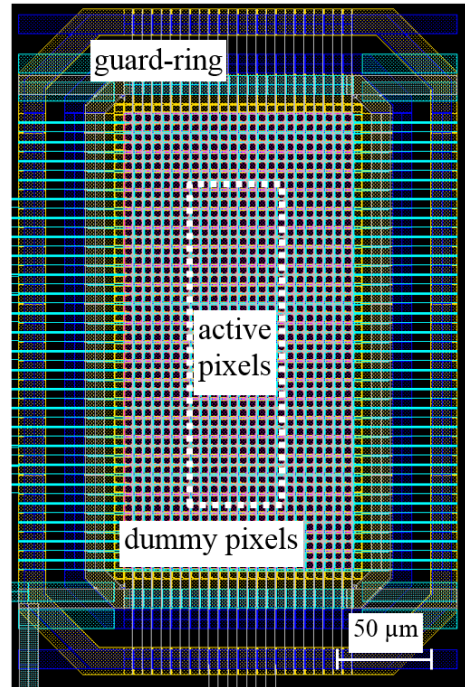


Fig. 9. 8x32 4-T PAPD pixel array layout example.

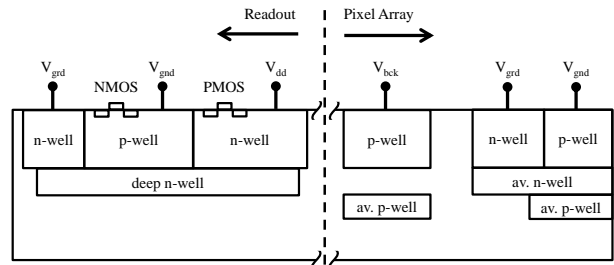


Fig. 10. Readout isolation and the pixel array guard-ring.

similar doping profiles to those required for the 4-T PAPD pixel are presented in Fig. 11 and 12. Good agreement for both avalanche and punch-through breakdown is achieved for varying avalanche n-well doses.

IV. CONCLUSION

To the best of our knowledge, this is the first study on pinned avalanche photodiodes to be used in 4-T based CMOS backside-illuminated image sensor arrays. The concept is aiming for improvements in pixel SNR in the low-light level regime for higher readout noise applications and potentially offering good optical properties as well as sub-nanosecond charge collection times. Main design parameters and their limitations are discussed and full pixel operation is shown in TCAD. The pixel test-array design is presented together with a solution for readout electronics isolation. Preliminary experimental results on the readout and pixel test structures are in good agreement with TCAD predictions. At the time of writing, further work on the pixel-array characterization is in progress.

REFERENCES

- [1] E. R. Fossum and D. B. Hondongwa, "A review of the pinned photodiode for CCD and CMOS image sensors," *IEEE J. Elec. Dev. Soc.*, vol. 2, p. 33, 2014.
- [2] G. Meynants, "Global shutter imagers for industrial applications," in *SPIE Photonics Europe*. International Society for Optics and Photonics, 2014, p. 914108.
- [3] Y. Zhou, Z. Cao, Q. Qin, Q. Li, C. Shi, and N. Wu, "A high speed 1000 fps CMOS image sensor with low noise global shutter pixels," *Science China Information Sciences*, vol. 57, no. 4, pp. 1–8, 2014.
- [4] R. McIntyre, "Multiplication noise in uniform avalanche diodes," *Electron Devices, IEEE Transactions on*, vol. 13, no. 1, pp. 164–168, 1966.
- [5] H. H. Barrett and K. J. Myers, *Foundations of Image Science*. New York: Wiley, 2003.
- [6] A. I. Biber, "Avalanche photodiode image sensing in standard silicon BiCMOS technology," Ph.D. dissertation, Eidgenössische Technische Hochschule (ETH), Zürich, 2000. [Online]. Available: <http://dx.doi.org/10.3929/ethz-a-003882060>
- [7] K. De Munck and T. Resetar, "Pinned photodiode (PPD) pixel architecture with separate avalanche region," U.S. Patent Application 20 140 374 867A1, Dec. 25, 2014.
- [8] S. L. Miller, "Avalanche breakdown in germanium," *Physical review*, vol. 99, no. 4, p. 1234, 1955.

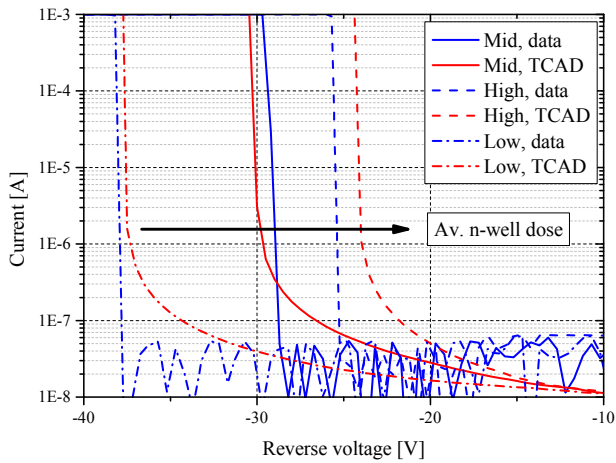


Fig. 11. Simulated and measured avalanche breakdown characteristics of test structures for different avalanche n-well doses: mid = $3.5 \times 10^{12} \text{ cm}^{-2}$, high = $4.1 \times 10^{12} \text{ cm}^{-2}$ and low = $2.9 \times 10^{12} \text{ cm}^{-2}$.

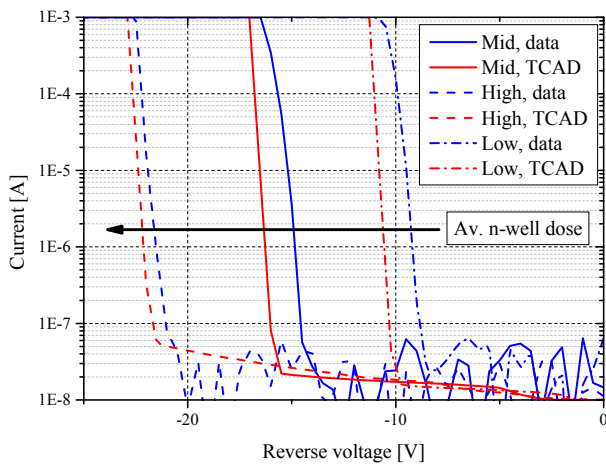


Fig. 12. Simulated and measured punch-through breakdown characteristics of test structures for different avalanche n-well doses: mid = $3.5 \times 10^{12} \text{ cm}^{-2}$, high = $4.1 \times 10^{12} \text{ cm}^{-2}$ and low = $2.9 \times 10^{12} \text{ cm}^{-2}$.