# A Flexible 32x32 SPAD Image Sensor with Integrated Microlenses

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**Abstract**

The first single-photon avalanche diode (SPAD) image sensor fully integrated on flexible substrate is reported. The design consists of an array of 1024 quenched pixels with CMOS readout and addressing circuitries. The flexible substrate was made compatible with sol-gel polymer, which will be used to imprint microlenses by quartz mold to improve fill factor. The SPAD pixel can operate both in frontside- (FSI) and backside-illumination (BSI) with similar peak photon detection probability (PDP) of 13%. The dark count rate (DCR) could be drastically reduced at a cryogenic temperature. Afterpulsing and cross-talk are negligible at the dead time.

## Introduction

Solid-state single-photon avalanche diode (SPAD) technology has existed for decades and is receiving wide attention for applications such as time-of-flight vision, time-correlated single-photon counting, fluorescence lifetime sensing and biomedical imaging. A SPAD is an avalanche photodiode (APD) operating above breakdown voltage, $V_{BD}$, in so-called Geiger mode and equipped with avalanche quenching and recharge mechanisms. Thanks to improved CMOS fabrication and Moore's Law, SPAD technology implemented in planar processes for imaging systems has significantly progressed in recent years [1].

However, the current SPAD technology is generally implemented on bulk silicon and it is still difficult to realize backside-illuminated devices [2] [3]. In our previous work, we demonstrated the world's first flexible SPAD fabricated in an ultrathin-body silicon-on-insulator (SOI) process followed by transfer post-processing to flexible substrate [4].

In this paper, we propose the first SPAD image sensor fully integrated on flexible substrate. The imager consists of an array of 1024 quenched pixels with CMOS readout and addressing circuitries. To improve fill factor, the flexible substrate was made compatible with sol-gel polymer, which will be used to imprint microlenses by quartz mold. The SPAD pixel can operate both in frontside- (FSI) and backside-illumination (BSI). Thanks to pixel-level CMOS buffer circuits, the excess bias could reach 4V, thereby enabling an increased peak photon detection probability (PDP). The dark count rate (DCR) could be drastically reduced by operating the SPADs at a cryogenic temperature as low as 80K. Afterpulsing and cross-talk are negligible at the dead time, thanks to reduced parasitic capacitance, obtained through the integration of the output buffer. The flexible CMOS compatible SPAD image sensor integrated with microlenses provides a suitable solution to advanced implantable photon counting devices for retinal prosthesis. Other applications include flexible multi-aperture imaging, anti-vignetting focal plane optimization, and (implantable) bio-compatible chronic medical monitoring.

## System architecture and fabrication

A block diagram of the 32x32 SPAD image sensor is shown in Fig. 1. All the functional blocks are designed to be on flexible substrate. As shown in Fig. 2, one pixel contains SPAD, quenching resistor, and CMOS buffer circuits. All the components are based on a trench-isolated silicon island structure to realize flexibility. Polyimide or polymer would be the flexible substrate and acts as a microlens to increase the fill factor at the same time.

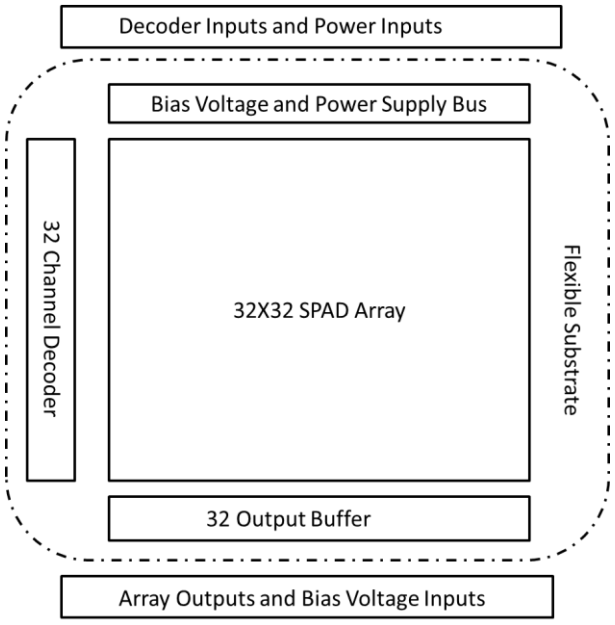


Fig.1. Block diagram of SPAD image sensor.

The SEM of single pixel is shown in Fig. 3. Fabrication begins with a p-type SOI wafer prepared by epitaxy technology. The N-well is formed by implantation and followed by a thermal drive-in process. After CMOS transistors are built, a N+P junction is formed by implantation. A P+ enhancement region is made to form the multiplication region and to prevent premature edge breakdown. After junction implantation, the device islands are formed and isolated with a trench by dry etching. Then, a passivation layer is deposited by two-time etch-back to form a spacer at the trench step. Contact holes are opened by dry etching. Then, a metallization layer is sputtered and patterned to realize the first metal interconnection. After the second metallization, which is similar to the first one,

the wafer is sent to alloy. The device fabrication flow is summarized in Fig. 4.

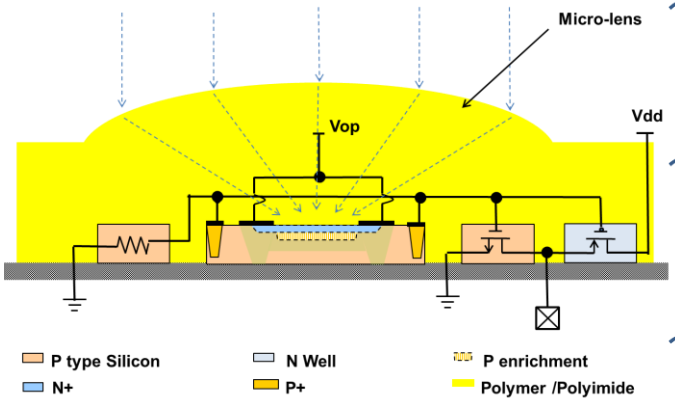


Fig. 2. Pixel schematic and SPAD cross-section.

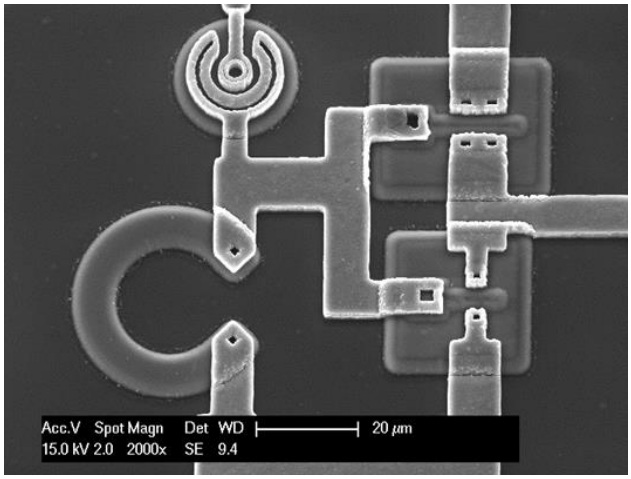


Fig. 3. SEM microphotograph of a pixel.

The flexible substrate transfer and microlens imprint process are summarized in Fig. 5. The sol-gel polymer is coated at the top of the device after metallization. Then, the polymer is patterned and the quartz mold is brought into contact with the polymer; pressure is applied to form the microlens array on top of the SPAD sensor [5] (The imprinting process is being complete at the time of the writing of the paper). The silicon substrate under the buried oxide layer is then etched away. The etching stops at the buried oxide layer and the SPAD image sensor layer on new flexible substrate can easily be released. Thanks to the function of the polymer layer as both flexible substrate and microlenses, the SPAD sensors with CMOS circuit systems can act as flexible imager with higher fill factor. According to our current design, the fill factor is expected to be higher than 10% with microlenses.

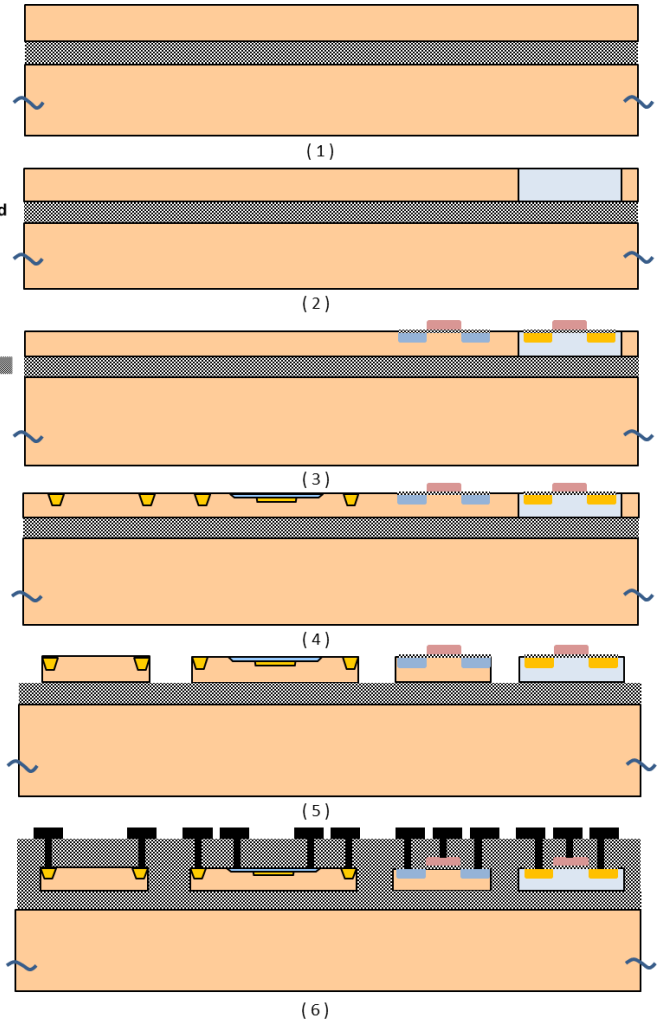


Fig. 4. Pixel device fabrication flow chart. (1) Epitaxy process; (2) N-Well implantation and driving in; (3) CMOS transistor fabrication; (4) trench etching process; (5) metallization. Note: Only $1_{st}$ metallization is shown in this figure.

## Measurement and analysis

The current-voltage (I-V) characteristics of the SPAD is shown in Fig. 6 for different light conditions. The breakdown voltage is around 26.5V at room temperature. The input-output response of the CMOS inverter, which consists of three-terminal SOI PMOS and NMOS transistors, is shown in Fig. 7. Compared with our previous work [6], the excess bias could be improved to 4V, by integrating CMOS buffering. The characterization of DCR as a function of excess bias is shown in Fig. 8. In this work, the pixel is operated at cryogenic temperature, as low as 80K, which is reported for the first time to our knowledge; DCR could be reduced dramatically as shown in Fig. 9.

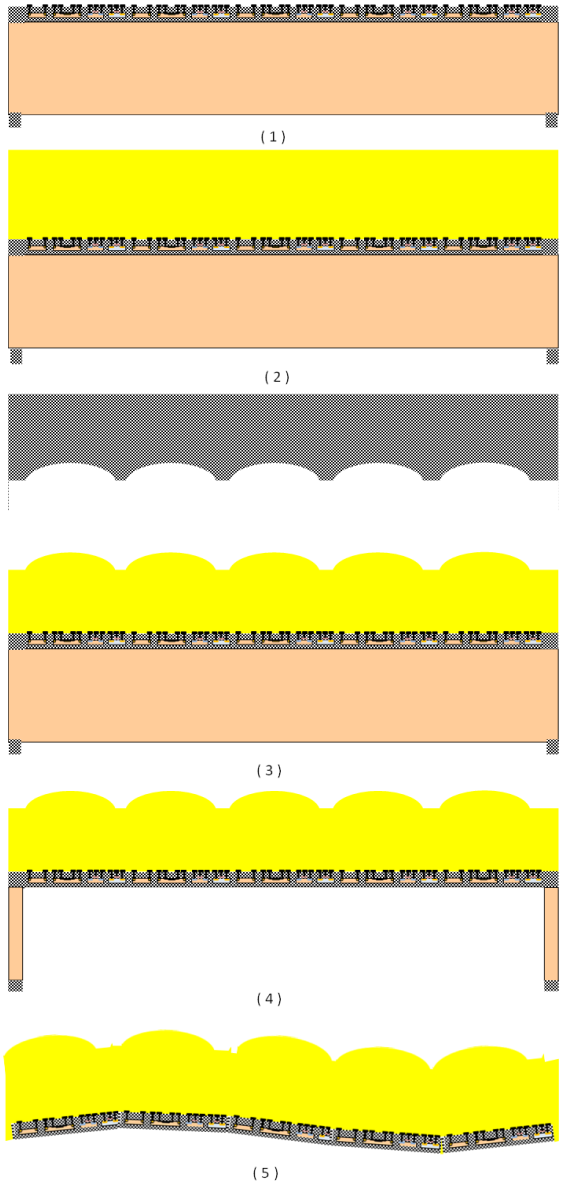


Fig. 5. Flexible substrate transfer and microlenses fabrication. (1) Oxide mask fabrication on backside; (2) sol-gel polymer coating; (3) microlenses imprinting; (4) substrate etching; (5) layer releasing.

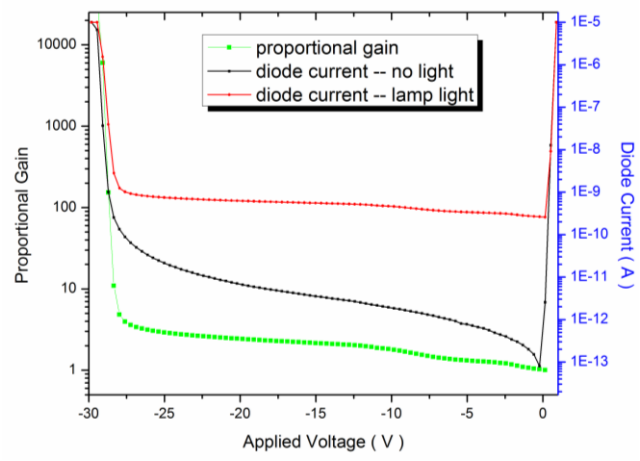


Fig. 6. I-V characteristics of SPAD.

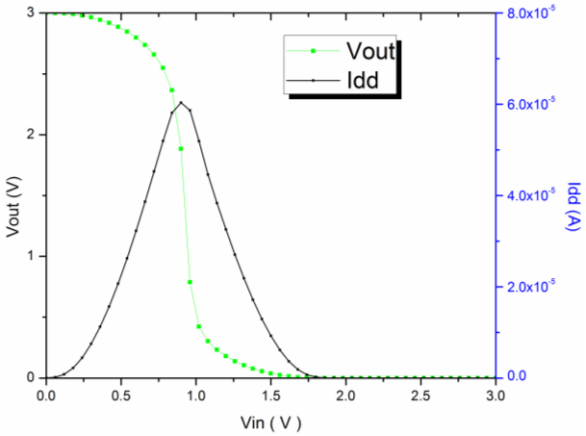


Fig. 7. DC transfer curve of CMOS Inverter.

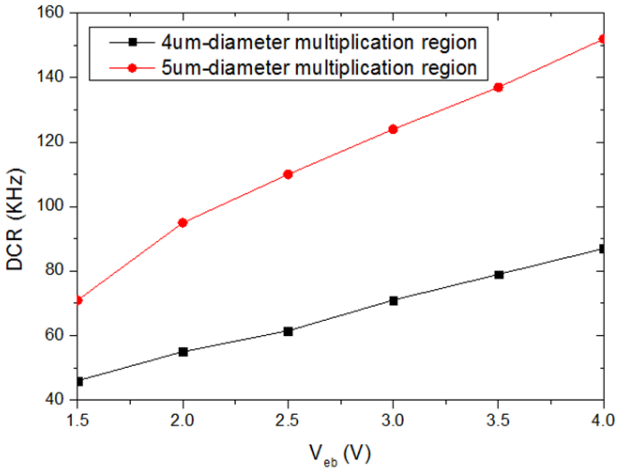


Fig. 8. DCR as a function of excess bias.

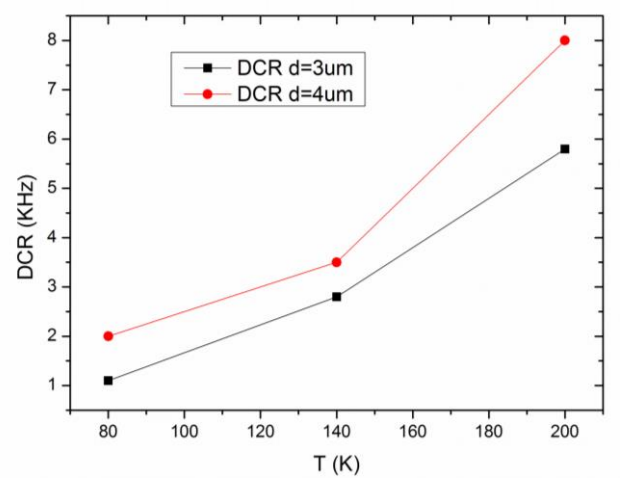


Fig. 9. DCR in a cryogenic environment. ($V_{eb}$=1.5V; d: diameter of multiplication region)

To characterize the sensitivity of the pixel, the PDP was measured in both FSI and BSI, as shown in Fig. 10. The peak PDP was measured to 13% in FSI and 12.5% in BSI, showing similar PDP performance. Thanks to the buffering circuits, the dead time reduced and consequently the PDP performance is enhanced because of the increased

saturation frequency. Furthermore, compared with our previous work [6], the PDP performance of BSI SPADs is also improved. The main reason is the epitaxy body doping diffusion into the intrinsic silicon layer on the top of buried oxide layer during a large amount of thermal budget in CMOS process. So the electric field across the neutral region near the buried oxide could be enhanced, resulting in larger probability for the photon-generated carriers in BSI to drift to the depletion region where avalanches are triggered.

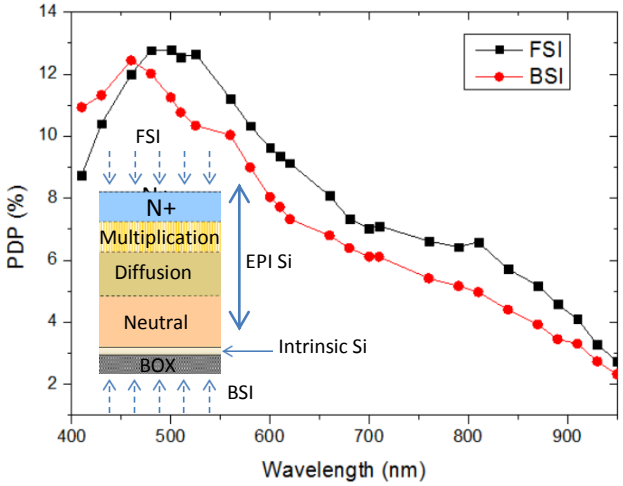


Fig. 10 PDP of frontside- and backside-illumination

With a dead time of 160ns, the afterpulsing probability is around 1.9%. At 1.3µs, the afterpulsing probability is less than 0.1% or about 5 times better than in [6]. The layout of the 32x32 array is shown in Fig. 12. The inset is the detail of single pixel. The microphotograph of a single pixel on flexible substrate and a photo of a bended sample are shown in Fig. 13.

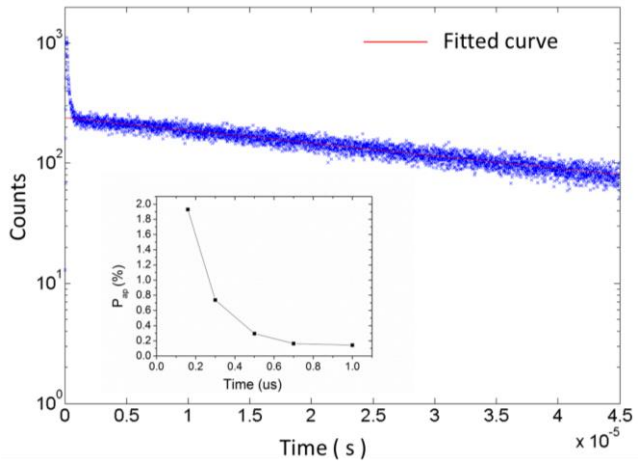


Fig. 11 Exponential fitted afterpulsing distribution of the SPAD pixel. Inset: afterpusling probability plot extracted from the distribution.

## Conclusions

To the best of our knowledge, the proposed design is the first flexible CMOS compatible SPAD image sensor with integrated microlenses reported to date. This technology is amenable to implantable, bio-compatible imaging sensors and wherever bended imaging sensors are essential.

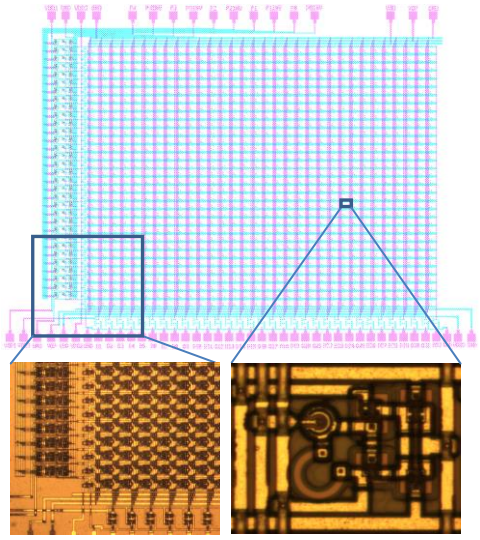

Fig. 12 32X32 SPAD image sensor layout top view.

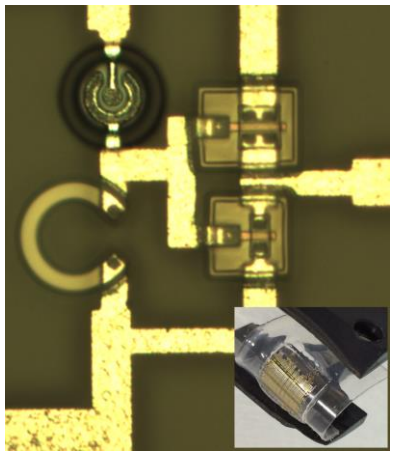

Fig.13 Microphotograph of pixel on flexible substrate. Inset: photo of bended flexible SPAD farm sample.

## References


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