A NIR-Sensitivity-Enhanced Single-Photon Avalanche Diode in 0.18µm CMOS

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***Abstract*—We introduce a single-photon avalanche diode with enhanced near-infrared sensitivity in 0.18µm CMOS technology. Despite its sensitivity to long-wavelength optical signals, the proposed SPAD has been designed to feature a relatively low breakdown voltage of approximately 20V. Experimental evaluation of the proposed SPAD has revealed photon detection efficiencies of 64.8% and 20.2% at 610nm and 870nm, respectively. Sensitivity with respect to the state-of-the-art has also been improved through fill factor optimization. Further device characterization has been carried out in terms of dark count rate, afterpulsing probability, and timing jitter.**

I. Introduction

An indispensable requirement in the evolution from advanced driver assistance systems (ADAS) towards automated driving technology is the realization of smart support functions that can perceive the environment, make decisions, and seamlessly maneuver the vehicle. The reliability of these functions, in turn, strongly depends on the accuracy and quality of the sensor data compiled from several sensor technologies. Among these technologies, light detection and ranging (LIDAR) has been used for the reliable detection and classification of particularly narrow objects at long distances. In this context, we have been working on low-cost long-range time-of-flight (TOF) sensors that acquire high-resolution 3D data in real-time [1]. In our sensors, we take advantage of avalanche photodiodes operating in the so-called Geiger mode. These devices, referred to as single-photon avalanche diodes (SPADs), generate accurately timed digital trigger signals upon detecting light with extremely low optical power, down to the single photon level [2]. In the near-infrared (NIR) spectral range however, until very recently [3], CMOS SPADs have exhibited rather low sensitivity. At the wavelength of interest in our application, i.e. 870nm, photon detection efficiencies (PDE) in CMOS have been typically lower than 5%. However, significant improvements in PDE for NIR have recently been achieved [3],[4]. For instance, the current state-of-the-art PDE of 20% at 870nm was obtained with an excess bias (V_E) of 12V in [4]. In addition, Webster et al. have also reported a fill factor of 21.6% for the same device in [5]. In this paper, we report on a new SPAD structure achieving similar PDE performance to that reported in [4], while also improving the sensitivity by optimizing the fill factor (FF).

II. Device Structure

An illustration showing a cross-section through the SPAD structure is shown in Fig. 1. The avalanching junction was engineered through the addition of two custom layers, i.e. n-SPAD and p-SPAD layers, to an existing 0.18µm CMOS process. The doping concentrations of these layers were optimized to achieve high avalanche gain with the p-SPAD layer fully depleted. As shown in the TCAD results in Fig. 2, the SPAD is characterized by a depletion layer that extends vertically from the bottom of the n-SPAD layer down to the intersection with the resulting p-type doping gradient in the epi-layer. As a result, photogenerated carriers are not only

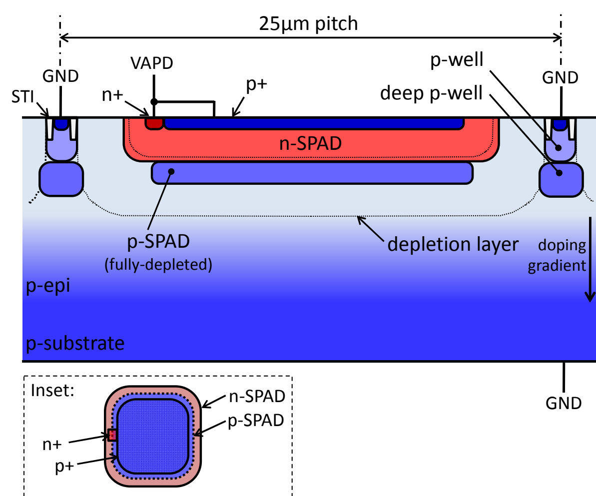

Fig.1. Simplified cross-section of the SPAD. Inset: view from top illustrating how the SPAD is electrically contacted to the n+ layer.

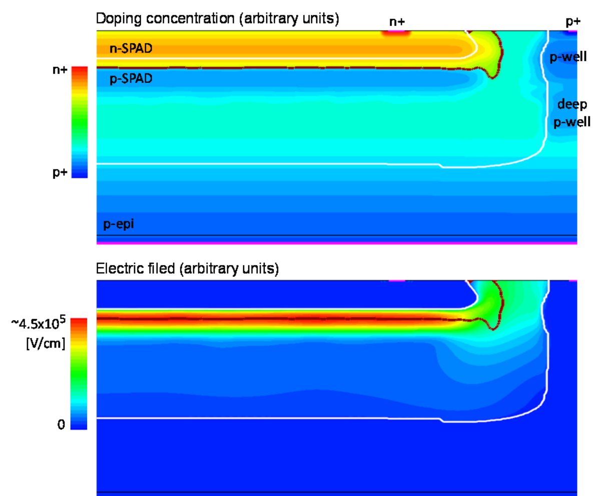

Fig. 2. Top: TCAD simulation model used for the optimization of the n-SPAD and p-SPAD layers. In this model, the p+ layer inside the device as well as the STI inside the p-well is omitted. Bottom: TCAD simulation result depicting the electric field as well as the depletion layer boundaries.

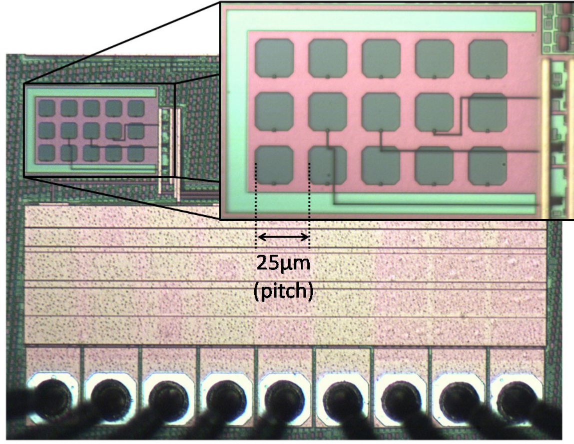

Fig. 3. Photomicrograph of a sample chip comprising an array of 5×3 SPADs and three quenching/readout circuits. Only the inner three SPADs are connected as depicted in the inset. The remaining 12 SPADs are used as "dummy" devices.

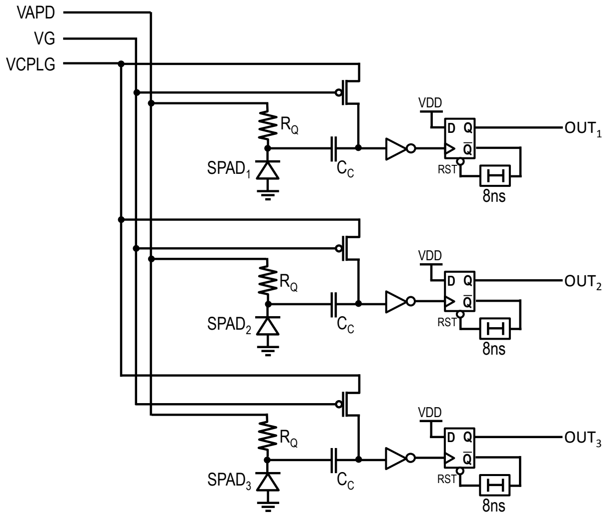

Fig. 4. On-chip quenching and readout circuit used for device characterization. Voltage pulses with an amplitude of $V_E \cong$ VAPD - V_{BD} at the SPAD cathode are capacitively coupled to the inverter, which triggers a monostable circuit, thus generating pulses of 8.5ns.

collected over most of the epi-layer thickness, they also tend to quickly drift upwards toward the avalanching junction, where an accurately timed response is generated.

A photomicrograph of a test chip designed for SPAD characterization purposes is shown in Fig. 3. The test chip comprises an array of 5×3 SPADs and three quenching/readout circuits. Only the inner three SPADs are connected as depicted in the inset of Fig. 3. The schematics of the quenching and readout circuits are shown in Fig. 4. SPAD quenching and recharge is performed passively by means of high-resistivity polysilicon resistors R_Q of 300kΩ, typically. Upon photon detections, negative voltage pulses with amplitude of approximately V_E = VAPD – V_{BD} are generated at the SPAD cathode, where V_{BD} is the SPAD breakdown voltage, VAPD is a positive bias voltage, and V_E is the SPAD excess bias. These pulses are then capacitively coupled via a metal fringe capacitor (C_C) of 5fF to the input of a CMOS inverter that acts as a comparator. The inverter input is biased at VCPLG by a thick-oxide PMOS transistor with a constant gate bias VG.

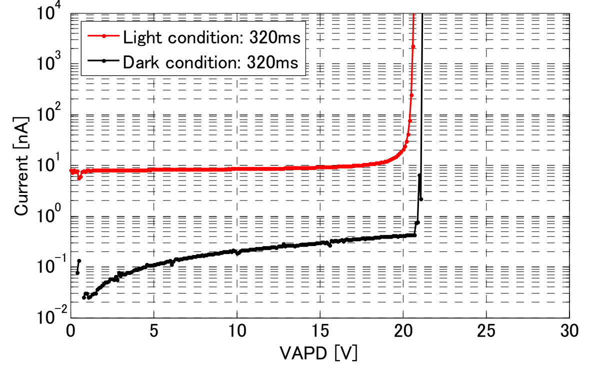

Fig. 5. Static SPAD current as a function of the reverse bias voltage. Current measurements were carried out under dark and light conditions with an integration time of 320ms.

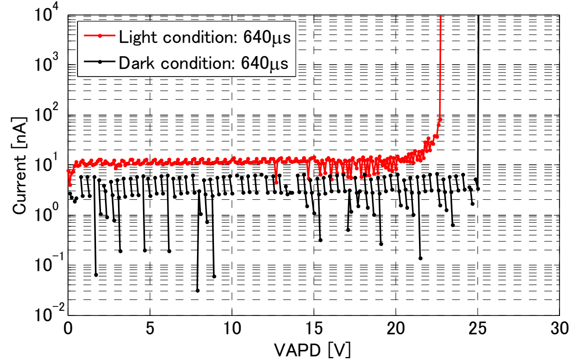

Fig. 6. Static current as a function of reverse bias with an integration time of 640μs. This figure shows how the SPAD bias may be maintained well above V_{BD} in dark conditions, thus validating its Geiger-mode operation capability.

The inverter is designed with thick-oxide transistors and it is powered by the core 1.8V supply voltage in this process. Positive pulses at the inverter output are converted to rectangular pulses of approximately 8.5ns by means of a D-flipflop-based monostable circuit, as shown in Fig. 4. This readout circuit imposes a minimum dead time of approximately 17ns, regardless of the actual SPAD recharge time.

III. Experimental Results

The static current/voltage characteristics of the proposed SPAD were measured using a semiconductor parameter analyzer and are plotted in Fig. 5 and Fig. 6, for two integration times. The measured V_{BD} was 20.5V. In Fig. 6, since the current integration time of the semiconductor parameter analyzer was set to 640μs, the figure also confirms that the SPAD bias (VAPD) may be maintained well above V_{BD} in dark conditions, thus validating its Geiger-mode operation capability.

In order to accurately measure FF, we devised and implemented the microscope-based setup shown in Fig. 7. The setup relies on the fact that all the light coming out of a Dirac-like point source placed in the focal plane of the camera port is focused onto a point on the sample surface. It allows, therefore, XY mapping of the photon counting rate of a SPAD at any desired optical wavelength with high spatial resolution. The micrometric resolution of the proposed setup was experimentally confirmed, as depicted in Fig. 8. A map of the photon response of a SPAD with a resolution of 0.5×0.5μm^2 was performed with V_E at 5V and

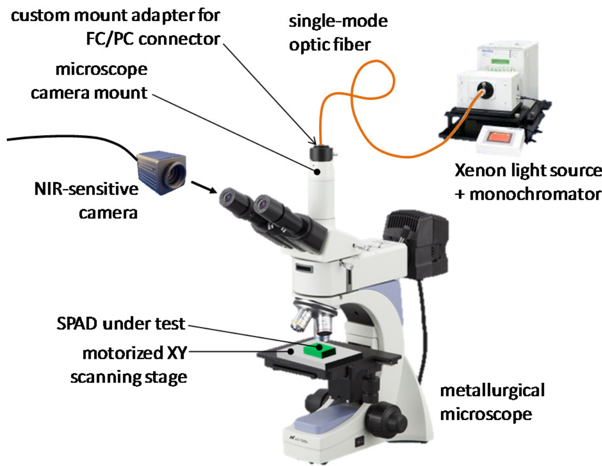

Fig. 7. Proposed optical setup used for high-resolution XY mapping of the photon response of SPADs at any desired optical wavelength.

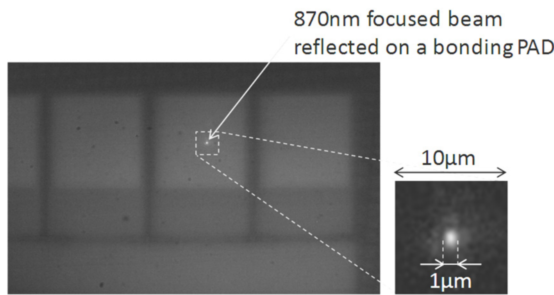

Fig. 8. Image captured using a NIR-sensitive camera mounted on one of the microscope's eyepieces (see Fig. 7). The spot size of the excitation signal at 870nm was confirmed to be approximately 1μm FWHM. This result was also corroborated by an alternative measurement technique.

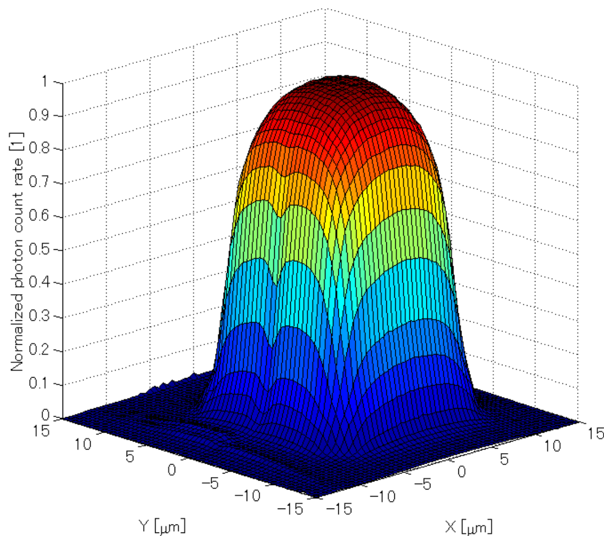

Fig. 9. Normalized photon counting rate map under excitation at 870nm scanned across an area of 30×30 μm^2, fully encompassing the 25×25μm^2 SPAD cell. The X and Y scanning resolution is 0.5μm. This result yields a fill factor of 33.1% FWHM at 870nm.

optical excitation at 870nm. The resulting photon counting rate map was normalized and is plotted in Fig. 9. This result yields an experimentally validated FF of 33.1% FWHM at 870nm. Furthermore, using a calibrated optical setup based on an integrating sphere and a reference photodiode, along with the measured FF, we accurately measured the SPAD

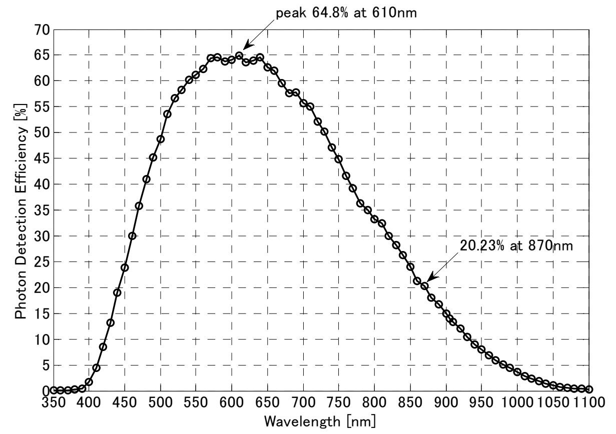

Fig. 10. Photon detection efficiency as a function of signal wavelength at an excess bias of 5V.

PDE as a function of signal wavelength. The PDE with V_E at 5V is plotted in Fig. 10. The SPAD exhibits a flat PDE of approximately 64% between 570nm and 640nm, while achieving 24% and 20.2% at 850nm and 870nm, respectively. To the best of our knowledge, this is the highest PDE achieved for a SPAD in CMOS under similar V_E bias conditions.

The dark count rates (DCR) of 18 SPAD samples from six test chips were measured at room temperature. Fig. 11 shows the measured DCR as a function of V_E. The mean and median values of the DCR among all the 18 samples is plotted as a function of V_E in Fig. 12. With the exception of one device, the obtained DCR were in line with the state-of-the-art for these relatively large SPADs. As indicated in Fig. 11, half of the measured samples exhibited a DCR below 100 counts per second (cps) with a high V_E of 5V, i.e. at 24% of excess bias with respect to V_{BD}. Taking into account the SPAD active area of 207 μm^2, the median DCR density among the 18 samples was 0.6 cps/μm^2 at room temperature with V_E at 5V. The mean DCR density was 7.6 cps/μm^2 in the same conditions due to the large variability among the measured samples, as depicted in Fig. 11.

Additional parasitic false detections in SPADs are caused by afterpulsing effects, i.e. the generation of parasitic false pulses that are correlated in time with actual photon detections. The afterpulsing probability was evaluated by performing an autocorrelation on a train of successive photon detections over 2s when the detector was illuminated by an uncorrelated light source, acquired with a resolution of 2ns, similarly to [6]. The leading 1μs of the resulting normalized autocorrelation with V_E at 5V is shown in Fig. 13 for three values of R_Q. In the inset of Fig. 13, the initial 80ns of the autocorrelation curves are plotted. The computed dead times and afterpulsing probabilities are indicated in the inset for each value of quenching resistor. These results reveal the typical trade-off between afterpulsing probability and dead time. The worst-case afterpulsing probability was 1.63% when targeting the shortest dead time of 17.9ns (R_Q of 200kΩ). For the device with a R_Q of 300kΩ, the afterpulsing probability and dead time were 0.35% and 25.4ns, respectively.

The timing response of the SPAD with V_E at 5V to a 635nm laser diode emitting 100ps pulses is shown in Fig. 14. This measurement response yields an overall timing jitter of 161ps FWHM when applying a quadratic correction to the laser pulse width.

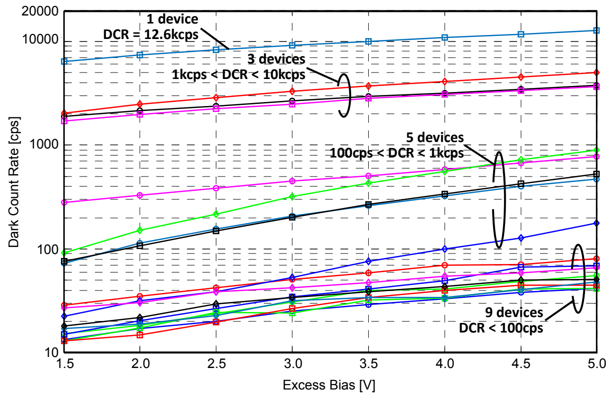

Fig. 11. Measured dark count rates as a function of excess bias for 18 SPAD samples.

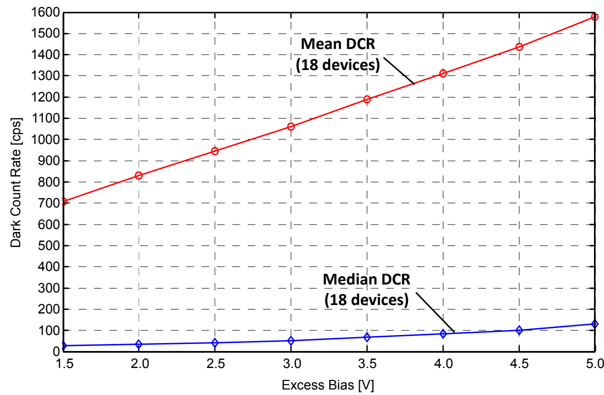

Fig. 12. Mean and median dark count rates as a function of excess bias for the 18 SPAD samples of Fig. 11.

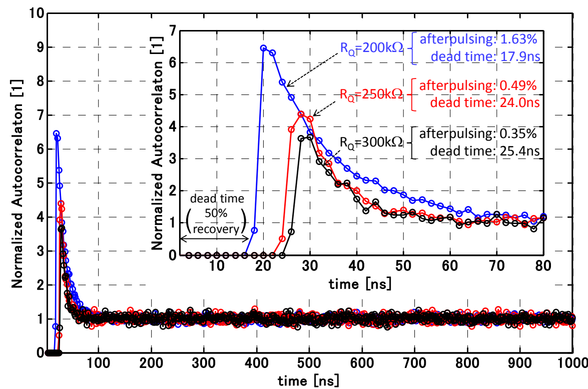

Fig. 13. Measured autocorrelation of the output voltage waveform of three samples with different quenching resistors under uncorrelated illumination with V_E at 5V. The acquired waveform duration was 2s with a resolution of 2ns. In the inset, the initial 80ns of the autocorrelation curves are plotted. The computed dead times and afterpulsing probabilities are indicated in the inset for each value of quenching resistor.

IV. Conclusion

We have introduced a new SPAD structure by adding two custom layers to an existing 0.18µm CMOS process. The proposed SPAD has been designed to feature a relatively low breakdown voltage of approximately 20V.

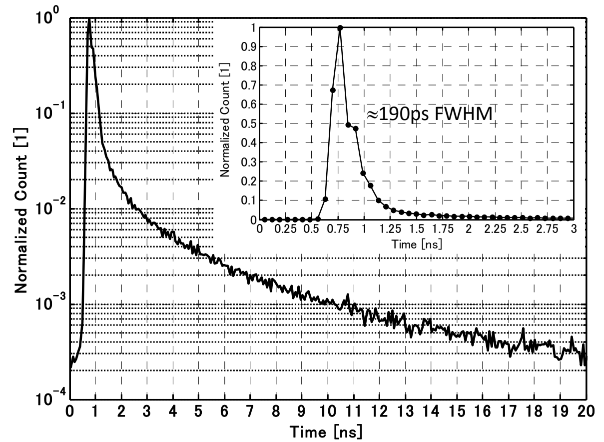

Fig. 14. SPAD timing response to a 635nm laser diode emitting optical pulses of approximately 100ps at 40MHz. This measurement response yields an overall timing jitter of 161ps FWHM when applying a quadratic correction to the laser pulse width.

The doping concentrations of the custom layers have been optimized to achieve high avalanche gain, yet obtaining the p-type layer fully depleted when the device is biased to operate in Geiger mode. Experimental evaluation of the proposed SPAD revealed photon detection efficiencies of 64.8% and 20.2% at 610nm and 870nm, respectively. To the best of our knowledge, this is the highest PDE achieved for a SPAD in CMOS under similar excess bias conditions, i.e. at 5V. Sensitivity with respect to the state-of-the-art has also been improved through fill factor optimization. Further SPAD characterization has been carried out in terms of dark count rate, afterpulsing probability, and timing jitter, all with the highest excess bias of 5V.

Acknowledgment

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