Characterization of Single-Photon Avalanche Diodes in Standard 140-nm SOI CMOS Technology

Myung-Jae Lee, Pengfei Sun, and Edoardo Charbon

***Abstract*—We report on the characterization of single-photon avalanche diodes (SPADs) fabricated in standard 140-nm silicon on insulator (SOI) complementary metal-oxide-semiconductor (CMOS) technology. As a methodology for SPAD optimization, a test structure array, called SPAD farm, was realized with several junctions, guard-ring structures, dimensions, etc. In this paper, characterization results of the most promising SOI CMOS SPAD are compared with state-of-the-art results reported in the literature.**

***Index Terms*—Avalanche photodiode (APD), backside illumination (BSI), CMOS, silicon, silicon on insulator (SOI), single-photon avalanche diode (SPAD), standard SOI CMOS technology.**

I. Introduction

PHOTON counting is one of the leading fields of research in image sensor technology. Monolithic solid-state complementary metal-oxide-semiconductor (CMOS) technologies for the fabrication of single-photon avalanche diodes (SPADs) have paved the way to image sensors optimized for many photon-counting applications, where single-photon sensitivity and time-of-arrival detection are critical [1]–[4]. For a conventional SPAD, monolithically integrated with readout circuitry, however, the fill factor of the image sensor is severely limited by the circuitry as well as its guard-ring structures and contacts. To address this limitation, backside illumination (BSI) is a promising option, while silicon on insulator (SOI) CMOS technology has been proposed as a possible solution to easily realize BSI SPADs because of the ease of stopping backside etching via the buried oxide (BOX) layer. To the best of our knowledge, no SPAD has yet to be demonstrated in standard deep-submicron SOI CMOS technology.

In order to fabricate, characterize, and optimize SPADs in a standard SOI CMOS technology, a test structure array, called SPAD farm, was realized with several junctions, guard-ring structures, dimensions, etc. After checking performance of all SOI CMOS SPADs, in this paper, we present the most promising structure, whereas we report full characterization results, including current-voltage characteristics, avalanche breakdown voltage, breakdown voltage variability with temperature and process, light emission, photon detection probability (PDP), dark count rate (DCR), and timing jitter. In addition, PDP and DCR are compared with the literature.

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II. Test Structure Array and Device Description

Fig. 1 shows a layout of the SPAD farm fabricated in the standard 140-nm SOI CMOS technology of interest; it includes a total of 94 different SPADs. Measurements

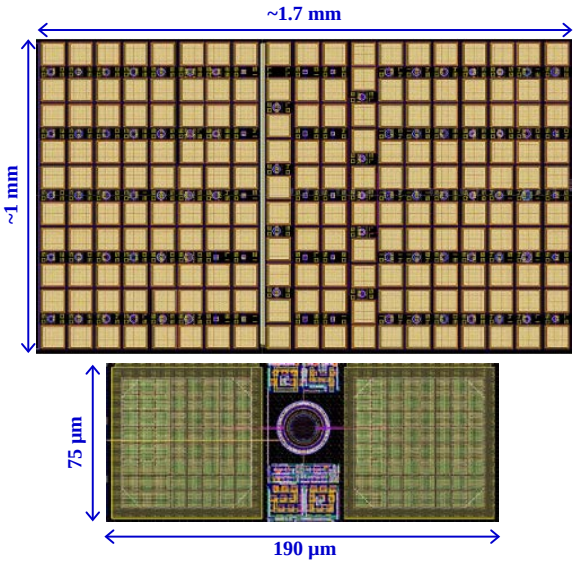

Fig. 1. Layout of the fabricated SOI CMOS SPAD farm.

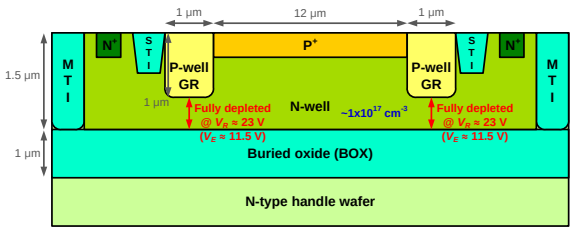

Fig. 2. Cross section of the fabricated SOI CMOS SPAD.

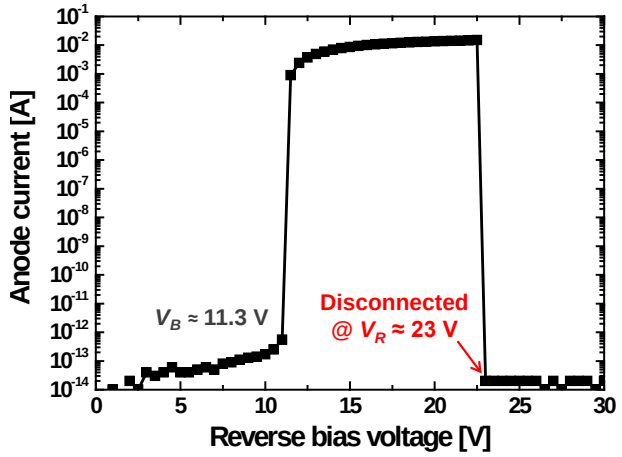

Fig. 3. Steady-state current-voltage characteristics of the SOI CMOS SPAD under dark condition at room temperature to check the avalanche breakdown voltage and the excess bias voltage limitation by fully-depleted N-well below the GR structure.

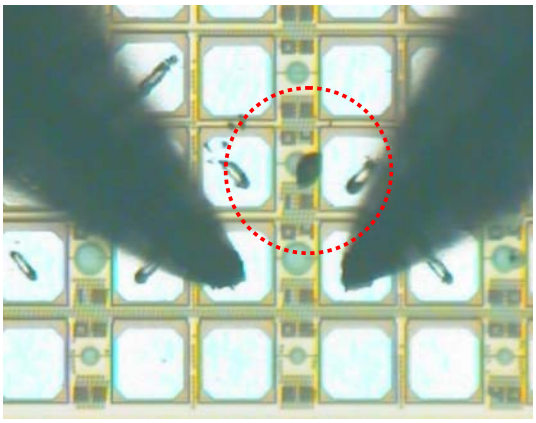

Fig. 4. Micrograph of the fabricated SOI CMOS SPAD after disconnection.

were conducted to check functionality and DCR was measured with on-wafer probing at room temperature. Most of SOI CMOS SPADs are saturated at very small excess bias because of numerous defects at the BOX to silicon interface, as well as band-to-band tunneling caused by high doping concentrations in the 140-nm CMOS technology. However, we have also found several structures operating well in Geiger mode; a cross section of the most promising SOI CMOS SPAD is shown in Fig. 2. The SPAD is based on the P^+/N-well junction with the 1-μm width P-well guard ring. The diameter of the active area is 12 μm, and the N-well and guard-ring depths are about 1.5 and 1 μm, respectively.

III. Characterization Results and Discussions

The SOI CMOS SPAD was wire-bonded on a printed circuit board (PCB), and a 20-kΩ quenching resistor was used for the characterization. Fig. 3 shows the current-voltage curve of the SPAD; its breakdown voltage is about 11.3 V at room temperature. In addition, it is clearly seen that the SPAD could not operate above about 23 V, because the N-well bias from the N^+ contacts is

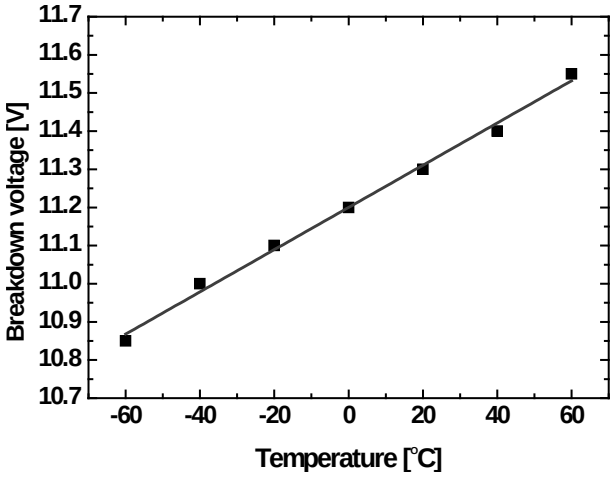

Fig. 5. Measured breakdown voltage of the fabricated SOI CMOS SPAD as a function of temperature.

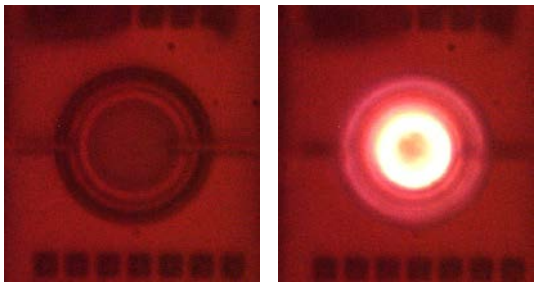

Fig. 6. Micrograph of the fabricated SOI CMOS SPAD and light emission test result.

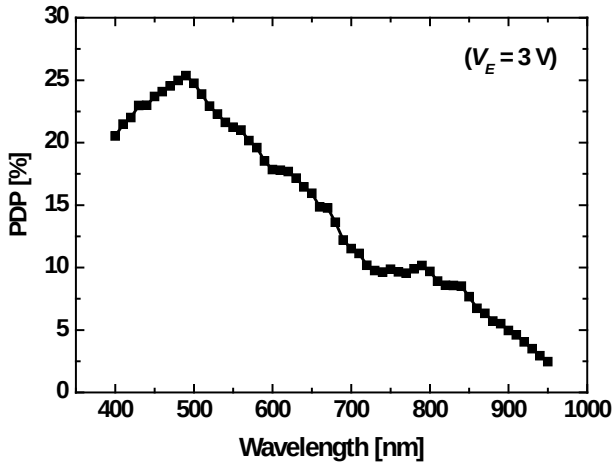

Fig. 7. PDP of the SOI CMOS SPAD as a function of the wavelength at room temperature.

disconnected by the fully-depleted N-well below the P-well guard ring due to the BOX layer. The SPAD shown in Fig. 4 has undergone this process, resulting in its destruction; this indicates that the excess bias voltage in SOI CMOS technology is limited by the BOX layer. The proposed SPAD can operate in Geiger mode with the excess bias voltage upto 11.5 V. Fig. 5 plots the SPAD breakdown voltage at various temperatures and Fig. 6 shows a micrograph of the SPAD with the result of the light emission test at an excess bias voltage of 3 V.

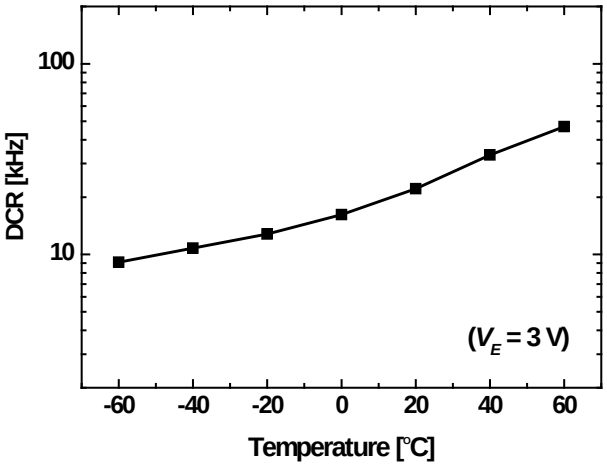

Fig. 8. DCR of the SOI CMOS SPAD as a function of temperature.

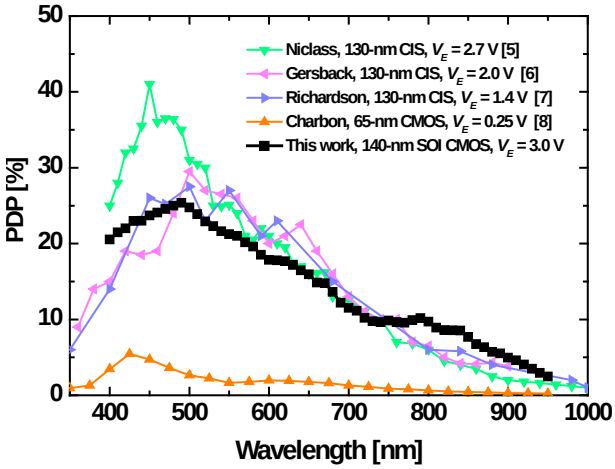

Fig. 10. SPAD PDP performance comparison.

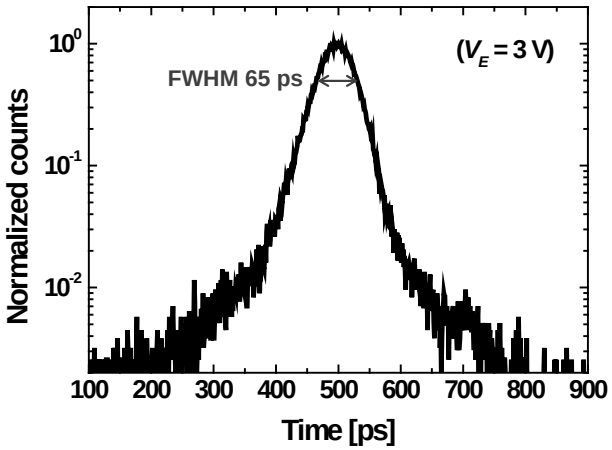

Fig. 9. Timing jitter performance of the SOI CMOS SPAD at room temperature using a 405-nm wavelength laser.

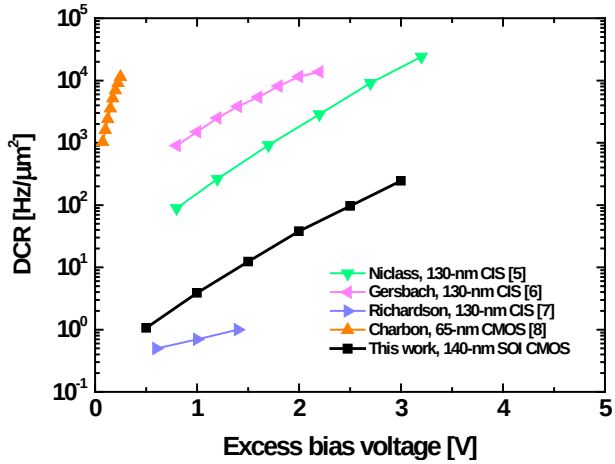

Fig. 11. SPAD DCR performance comparison.

TABLE I
PERFORMANCE SUMMARY FOR THE SOI CMOS SPAD

Performance	Min.	Typ.	Max.	Unit	Comments
SPAD diameter		12		μm	Circular shape
Avalanche breakdown voltage	11.2	11.3	11.4	V	Inter-chip variation at 25 °C
Excess bias voltage			11.5	V	Limited by BOX layer
Avalanche breakdown voltage	10.85		11.55	V	Temp = -60~60 °C
PDP	2.5		25.4	%	λ = 400~950 nm V_E = 3 V
DCR	9.1		46.9	kHz	Temp = -60~60 °C V_E = 3 V
Timing jitter		65		ps	FWHM at 405 nm V_E = 3 V

Fig. 7 shows measured PDP performance of the SPAD at the excess bias voltage of 3 V, achieving a maximum PDP of over 25 % at 490 nm. In addition, the SOI SPAD shows enhanced PDP characteristics at long wavelengths above about 750 nm thanks to the reflection of the light by the interface between silicon and BOX layers.

Fig. 8 plots the SPAD DCR characteristics at various temperatures. With the excess bias voltage of 3 V, the DCR is about 22.1 kHz at 20 °C, and it is reduced to 9.1 kHz by decreasing temperature to -60 °C. The weak dependence of the DCR on temperature implies that it is dominated by band-to-band tunneling due to the relatively higher doping concentration of the N-well in this SOI CMOS technology.

Fig. 9 summarizes the timing jitter performance of the SPAD at the excess bias voltage of 3 V, measured using the time-correlated single-photon counting (TCSPC) technique. It shows a remarkable time resolution of 65 ps (FWHM).

Table I lists the proposed SOI CMOS SPAD characteristics. To compare the proposed device performance to CMOS SPAD performance, substrate-isolated SPADs implemented in a feature size smaller than 150 nm are considered for a fair comparison.

Fig. 10 and 11 present PDP and DCR comparisons with the state-of-the-art CMOS SPADs [5]–[8]. It is clearly observed that the SOI CMOS SPAD achieves comparable PDP performance to conventional CMOS SPADs at short wavelengths and better PDP at the long wavelengths above 750 nm. In addition, it exhibits good DCR performance compared to conventional CMOS SPADs.

IV. Conclusion

This paper reports on the design and characterization of SPADs fabricated in standard SOI CMOS technology. Some SOI CMOS SPADs are saturated with very small excess voltage probably due to numerous defects at the BOX to silicon interface and band-to-band tunneling caused by high doping concentrations of the technology, but we have found several SPADs operate well in Geiger mode with the realized test structure array, SPAD farm. Full SPAD characteristics, such as current-voltage characteristic, breakdown voltage variation, light emission, PDP, DCR, and timing jitter, of the most promising structure are presented and discussed. The performance of the proposed SOI CMOS SPAD is comparable to or better than that of SPADs fabricated in CMOS technologies in the literature.

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