

High-Sensitivity Image Sensor with Stacked Structure comprising Crystalline Selenium Photoconductor, Crystalline OS FET, and CMOS FET

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Abstract

To realize a high-sensitivity CMOS image sensor using avalanche multiplication, we investigate the feasibility of a pixel structure that uses a crystalline selenium-based photoelectric conversion element and a crystalline oxide semiconductor (OS)-based FET. The OS FET is shown to have a withstand voltage of over 20 V, with which the photoelectric conversion element can cause avalanche multiplication. An amorphous selenium-based photoelectric conversion element in which holes are mainly travelling carriers and which is formed on a pixel electrode on a pseudo OS FET/CMOS FET substrate exhibits favorable photoconductivity, indicating compatibility with an OS FET/CMOS FET hybrid process. This shows the potential for realizing an OS/CMOS image sensor using avalanche multiplication in a crystalline selenium-based photoelectric conversion element.

Introduction

A configuration for a CMOS image sensor with a photoelectric conversion element instead of a silicon photodiode has been proposed in [1, 2], incorporating a high-gain avalanche rushing amorphous photoconductor (HARP) stacked onto a transistor with a high withstand voltage through a micro-bump. Unfortunately, this configuration requires a high process cost, and poses problems such as variations in device properties and mechanical stress. Furthermore, a crystalline selenium film has been reported to cause avalanche multiplication and thus have a quantum efficiency greater than 100% with over 20 V bias [3], and an image sensor having a photoelectric conversion element using the crystalline selenium film formed on a CMOS circuit has been proposed [4]. A high-sensitivity CMOS image sensor utilizing avalanche multiplication can be achieved with a hole-readout structure, a lower multiplication voltage, a considerably lower dark current, and a higher multiplication factor.

A crystalline oxide semiconductor (OS), typically c-axis aligned crystalline In-Ga-Zn oxide (CAAC-IGZO), is a wide bandgap semiconductor. An

FET containing the OS exhibits ultra-low off-state current and has a high withstand voltage [5]. Image sensors utilizing these features have been proposed, including an OS FET as a pixel transistor [6–8].

This paper proposes a CMOS image sensor using a crystalline selenium film for a photoelectric conversion element and an OS FET in a pixel. It is shown that the OS FET has a high withstand voltage and that a selenium-based photoelectric conversion element is compatible with the OS FET/CMOS FET hybrid process in terms of electrode structure. Furthermore, this paper examines the feasibility of the avalanche-mode CMOS image sensor with the crystalline selenium film.

Device and Circuit Configurations

A. Device Configuration

Fig. 1 illustrates the configuration of the device proposed in this paper. A pixel electrode, a photoelectric conversion element, and a common electrode are stacked on an OS FET/CMOS FET substrate. We aim for a photoelectric conversion element using a crystalline selenium film. This study will examine the withstand voltage of an OS FET and, as a first step of investigating the feasibility of the novel configuration, process compatibility by evaluating a sample that is a selenium-based photoelectric conversion element shown in Fig. 2.

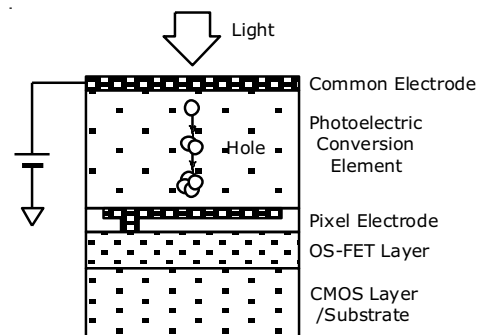


Fig. 1. Device configuration of a stacked structure comprising an avalanche-mode selenium-based photoconductor, a crystalline OS FET, and a CMOS FET.

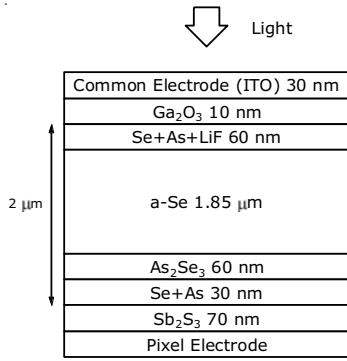


Fig. 2. Configuration of a hole-reading selenium-based photoconductor.

B. Circuit Configuration

Fig. 3 shows a circuit diagram and an operation timing chart of the pixel. The common electrode is positively biased, and a reset voltage is GND. The transistors M_R and M_T required to have high withstand voltages when avalanche multiplication occurs are OS FETs. It should be noted that the use of an OS FET with an ultra-low off-state current for M_R is likely to reduce reset noise. When the amplitude of the signal, T , ranges from GND to VDD, the highest voltage applied to M_A is VDD; thus, as the transistors M_A and M_S do not necessarily have high withstand voltages, Si FETs can also be used, resulting in efficient scaling.

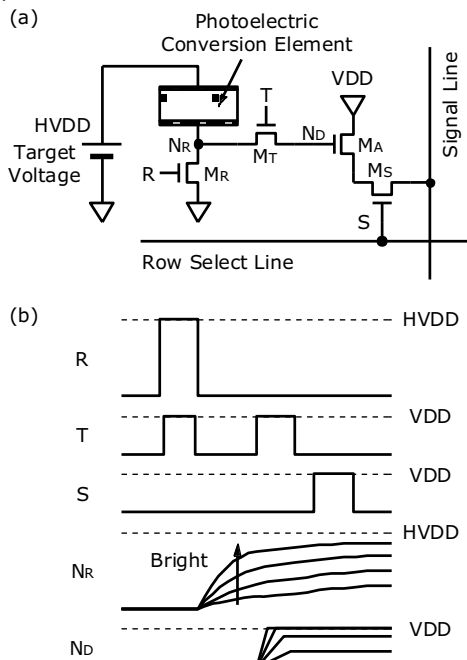


Fig. 3. (a) Circuit diagram and (b) timing chart for a pixel with a stacked structure comprising an avalanche-mode selenium-based photoconductor, a crystalline OS FET, and a CMOS FET.

Fabrication and Measurement

A. Oxide Semiconductor FET

Figs. 4 and 5 are cross-sectional views of the OS (CAAC-IGZO) FET. Fig. 6 shows the static characteristics of the CAAC-IGZO FET, and Figs. 7 to 9 represent its measured withstand voltage. Here the CAAC-IGZO FET has a channel length L of $0.35 \mu\text{m}$, a channel width W of $0.8 \mu\text{m}$, and an equivalent oxide thickness of the gate insulating film of 20 nm (with a physical thickness of 31 nm). As the CAAC-IGZO FET contains a wide bandgap semiconductor ($> 3.0 \text{ eV}$), its drain breakdown voltage depends on the thickness of the gate insulating film, rather than the junction breakdown voltage. Moreover, short-channel effects are unlikely to occur in the OS FET [5]; therefore, the CAAC-IGZO FET easily obtains normally off characteristics while increasing the drain breakdown voltage using a thick gate insulating film. The measurement results demonstrate that the CAAC-IGZO FET withstands bias exceeding 20 V necessary for a crystalline selenium film to cause avalanche multiplication [3]. Note that a failure mode of the CAAC-IGZO FET is dielectric breakdown.

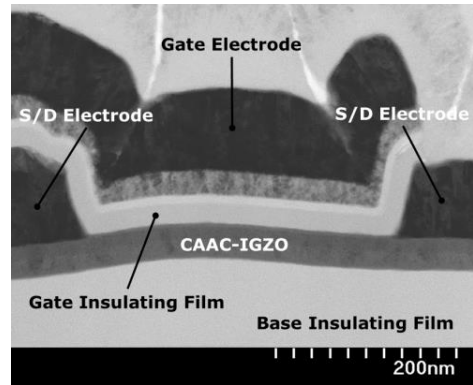


Fig. 4. Cross-sectional STEM image of a CAAC-IGZO FET in the channel length direction.

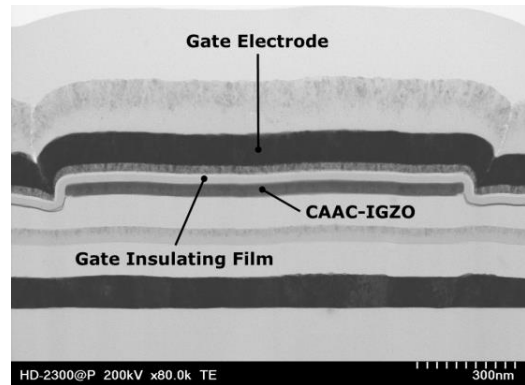


Fig. 5. Cross-sectional STEM image of the CAAC-IGZO FET in the channel width direction.

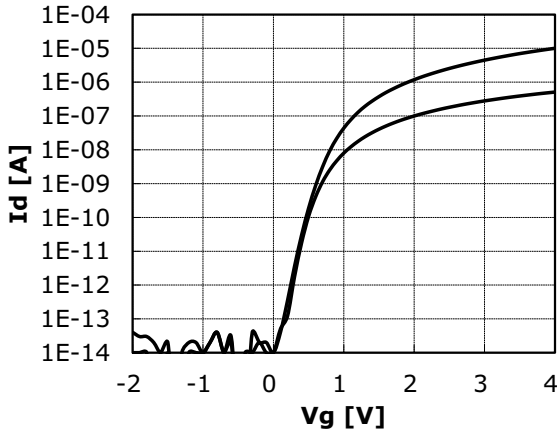


Fig. 6. Transfer characteristics of a CAAC-IGZO FET with $L/W = 0.35 \mu\text{m}/0.8 \mu\text{m}$ and $T_{\text{ox}} = 31 \text{ nm}$ ($\text{EOT} = 20 \text{ nm}$) at drain voltage $V_{\text{d}} = 0.1$ and 3.3 V . The measurement limit of the semiconductor parameter analyzer is 10^{-13} A .

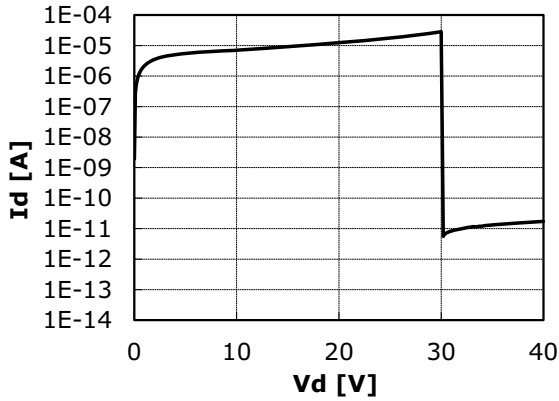


Fig. 7. Measured drain breakdown voltage of the CAAC-IGZO FET with $L/W = 0.35 \mu\text{m}/0.8 \mu\text{m}$ and $T_{\text{ox}} = 31 \text{ nm}$ ($\text{EOT} = 20 \text{ nm}$) at $V_{\text{g}} = 3 \text{ V}$ and $V_{\text{s}} = 0 \text{ V}$. The CAAC-IGZO FET has a drain breakdown voltage of approximately 30 V .

B. Photoconductor Fabrication

The CAAC-IGZO FET and the pixel electrode are connected through a contact hole formed in an interlayer film on the OS FET/CMOS FET substrate [5]. To examine process compatibility, a photoelectric conversion element is formed on a substrate provided with the uppermost wire layer of the OS FET/CMOS FET substrate and the pixel electrode (a substrate with a simplified structure). The pixel electrode is formed of Mo, W, or indium tin oxide (ITO). Fig. 10 shows a chip micrograph of the sample with an ITO pixel electrode.

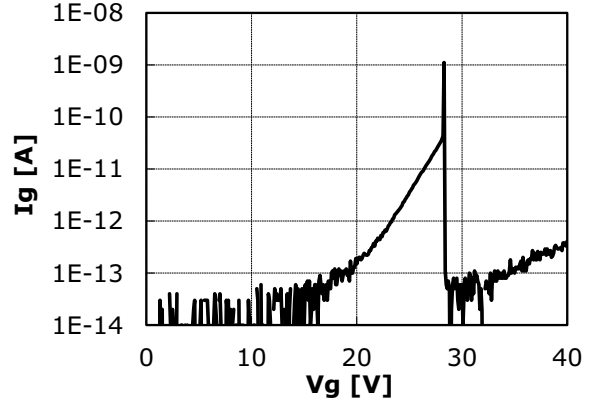


Fig. 8. Measured positive gate breakdown voltage of the CAAC-IGZO FET with $L/W = 0.35 \mu\text{m}/0.8 \mu\text{m}$ and $T_{\text{ox}} = 31 \text{ nm}$ ($\text{EOT} = 20 \text{ nm}$) at $V_{\text{s}} = V_{\text{d}} = 0 \text{ V}$. The CAAC-IGZO FET has a gate breakdown voltage close to 30 V .

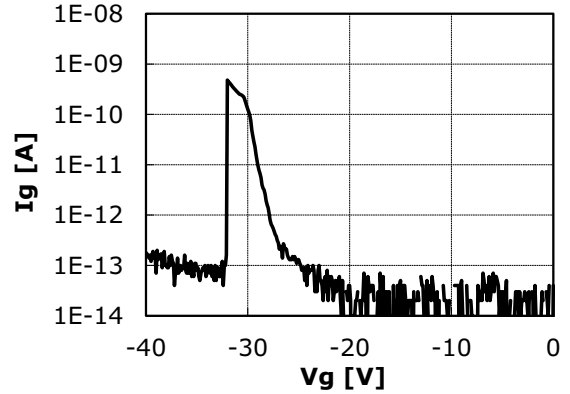


Fig. 9. Measured negative gate breakdown voltage of the CAAC-IGZO FET with $L/W = 0.35 \mu\text{m}/0.8 \mu\text{m}$ and $T_{\text{ox}} = 31 \text{ nm}$ ($\text{EOT} = 20 \text{ nm}$) at $V_{\text{s}} = V_{\text{d}} = 0 \text{ V}$. The CAAC-IGZO FET has a gate breakdown voltage more than -30 V .

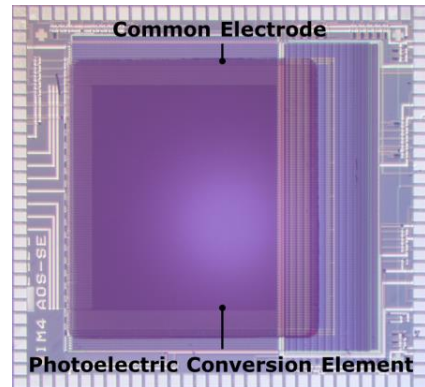


Fig. 10. Sample chip micrograph. A hole-reading selenium-based photoconductor is formed on a pseudo OS FET/CMOS FET hybrid chip.

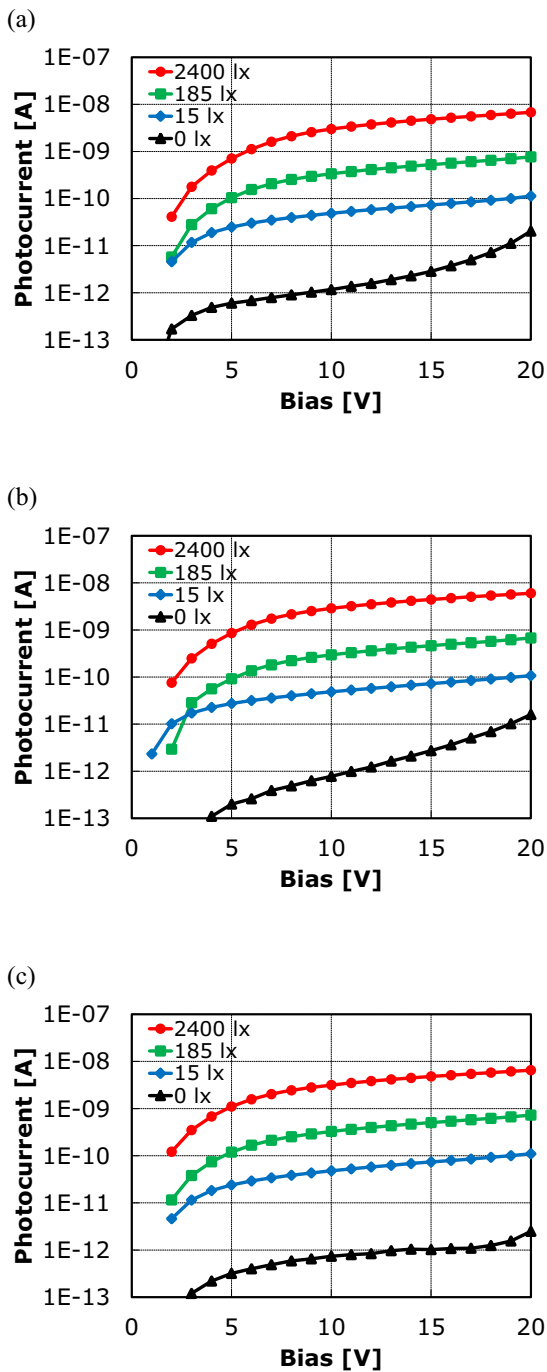


Fig. 11. Photoconductivity of a selenium-based photoconductor of a sample with (a) Mo pixel electrode, (b) W pixel electrode, and (c) ITO pixel electrode.

C. Photoconductor Measurement

Fig. 11 shows the photocurrent properties of the various photoelectric conversion elements. Although the elements have slightly different photoelectric characteristics depending on the electrode materials (e.g., work function or surface roughness), a hole-blocking layer (Ga_2O_3) works effectively and reduces dark current. These characteristics are substantially equivalent to those of a similar element formed on a glass substrate. It is thus observed that the selenium-based photoelectric conversion element is formed effectively on the OS FET/CMOS FET substrate, thereby indicating process compatibility. This shows that avalanche multiplication in a crystalline selenium photoelectric conversion element will be feasible.

Conclusion

This study has demonstrated that the OS (CAAC-IGZO) FET has a high withstand voltage and that a selenium-based photoelectric conversion element is compatible with an OS FET/CMOS FET hybrid process in terms of electrode structure. These results may promise the achievement of a CMOS image sensor with a photoelectric conversion element using a crystalline selenium film, which causes avalanche multiplication and has the quantum efficiency over 100%, showing much higher sensitivity than a conventional one.

References

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