A low-noise, P-type, vertically-pinned and back-side-illuminated pixel structure for image sensor applications

B. Mamdy[1,2] ; F. Roy[1] ; N. Ahmed[1,2] ; G.N. Lu[2]

[1]STMicroelectronics, 850 rue J. Monnet BP16, 38926 Crolles cedex, France

Tel: +33 4 38 92 31 67 - E-mail: bastien.mamdy@st.com

[2]Institut des Nanotechnologies de Lyon (INL), Université Claude Bernard Lyon 1 - Bat. Léon Brillouin

43, boulevard du 11 Novembre 1918 – 69622 Villeurbanne Cedex - France

***Abstract*-We propose a P-type back-side-illuminated (BSI) pixel. It was implemented in a shared 2T architecture at 1.4µm pitch. The pixel employs a hole-collection, vertically-pinned deep photodiode and other PMOS components. It has a full well capacity over 7000h+ and a conversion factor of 134µV/h+. Noise analysis on the PMOS source follower (SF) shows much lower trapping noise than the NMOS counterpart. The proposed P-type pixel may thus allow better low-noise achievement for image sensor application.**

***Index Terms*- CMOS image sensor, hole collection, vertical pinning, back-side illumination, PMOS source follower, deep photodiode**

Introduction

In the past decade conventional CMOS image sensors have evolved impressively through the introduction of many performance-improving techniques and structures, such as back-side illumination (BSI) and improved pixel-to-pixel isolation for ever smaller pixel pitch. Noticeably, despite all these transformations, the vast majority of image sensors remain based on electron collection photodiode and N-type readout architecture. However there have been reported studies showing that hole-based pixels could present some advantages over N-type counterparts [1] [2] [3].

P-type pixel developments involve major changes in fabrication process and require much effort on process integration and optimization. But this will also offer possibilities to further develop new and improved image sensors by choosing N or P-type components according to targeted applications.

In this paper, we propose a P-type, BSI pixel structure comprising a hole-collection, vertically-pinned photodiode and PMOS readout components. It integrates oxide-filled deep trench isolation (DTI) between pixels. The 3µm-deep DTI suppresses electrical crosstalk and plays a role of waveguide inside the silicon to limit optical crosstalk and improve angular response [4]. By adopting a pitch of 1.4µm and a shared 2T-architecture the pixel was designed in a combined 65 and 95nm technology. Figure 1 shows the pixel layout. The design is voluntarily very similar to the 1.4µm N-type pixel presented in [5] so as to compare both structures.

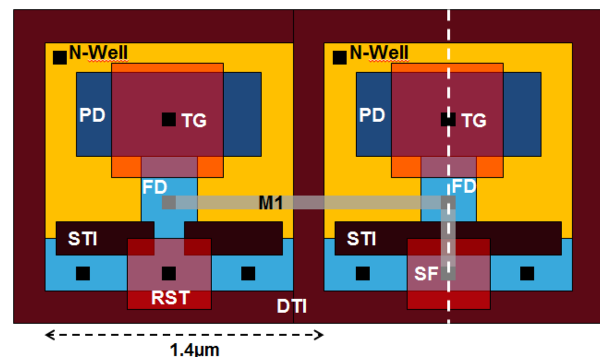

Figure 1: Simplified layout of P-type pixel implemented in 1.4µm-pitch, shared 2T architecture

In this 2T architecture, the line selection is performed by blocking the SF thanks to the reset transistor drain voltage; it therefore removes the need for a dedicated line selection transistor and further saves some space on the layout. Finally, the use of a triple access reset transistor minimizes the number of metallic interconnections and maximizes the conversion factor (CVF).

Hole-collection vertically-pinned photodiode…

The proposed P-type pixel is implemented in a 3µm-thick silicon layer grown on SOI substrate. At 1.4µm pitch, the aspect ratio is over 2. With vertical pinning of the photodiode, the full well capacity (FWC) is no longer limited by the pixel pitch but by its volume. The photodiode's volume is optimized by extending its depth over the entire volume of the pixel. This structure is

similar to the one reported in [5], which showed large full well capacity and good quantum efficiency. But unlike the N-type counterpart the hole collection photodiode was fabricated by carefully adjusting the boron concentration during the epitaxy to control the amount of charges stored in the bulk of the pixel. N-type ion implantations were employed to passivate the deep trench isolation as well as to pin the bottom-part of the photodiode and maintain it fully depleted.

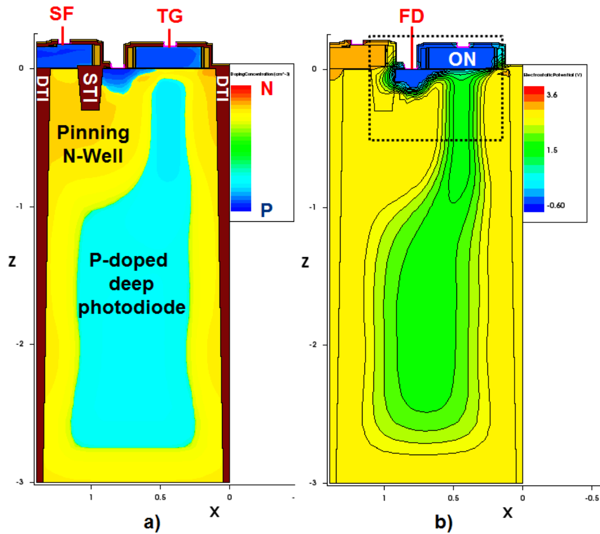

Figure 2: Cross-sections of the P-type, 1.4µm-pitch pixel, showing: a) volume of photodiode; b) electrostatic potentials with iso-potentials when TG (transfer gate) is ON.

The doping profile at the photodiode was then engineered by several ion implantations so as to generate a gradual electrostatic potential shift going from the bulk towards the floating diffusion node and thus to facilitate the transfer of holes while avoiding lag. In addition, shallow N-type implantations were used to pin the potential of the top of the photodiode.

Transfer-gate structure

The physical structure of the transfer gate (TG) should be implemented with process optimization to ensure pixel operation. On the one hand, when TG is off, a good potential barrier is necessary between the floating diffusion node and the photodiode in order to reach maximum FWC and prevent leakage of charges. On the other hand, when TG is on, all the charges should be transferred from the photodiode to the floating diffusion node.

Figure 3 shows measured Id(Vgs) on a test transistor structure similar to TG. It is off when Vgs = 1V. The bulk-source voltage Vbs is related to the filling of the photodiode. For Vbs = 0V, which corresponds to the case where the photodiode is full, the structure exhibits a noticeable current leakage. It sets a limit to FWC. Structures with optimized implantation do not show this current leakage and the photodiode can therefore reach full saturation.

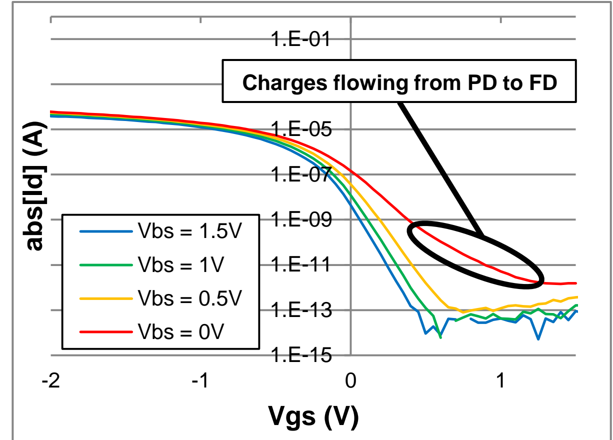

Figure 3: Id(Vgs) of a test structure similar to TG, with variation of Vbs corresponding to photodiode's filling.

Figure 4 shows two cases of charges transfer by 3D-TCAD simulation. In the case of Figure 4a where two potential barriers remain in the transfer path, the transfer is only partial, leading to image lag. It is needed to obtain 100% transfer as shown in Figure 4b. To this end, we employed shallow ion implants of opposite types to optimize the structure.

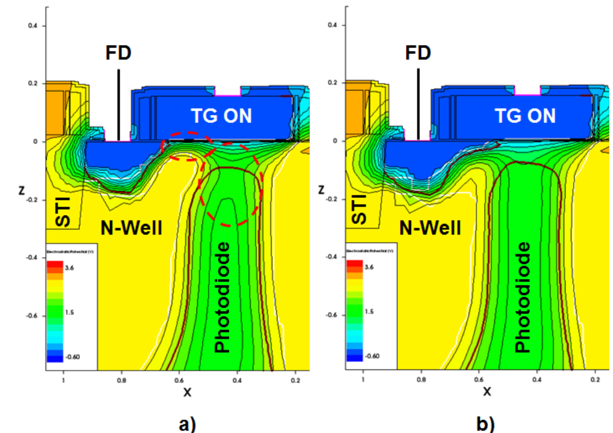

Figure 4: 3D-TCAD simulation of the TG structure showing electrostatic potential profile: a) prior to process optimization; b) after optimization.

Noise of PMOS source follower

The PMOS SF is implemented between STI and DTI. It has two main noise sources: thermal noise and trapping noise. Figure 5 shows

the observed PMOS SF output variations resulting from these two noise sources. After correlated double sampling most of the trapping noise is filtered out [6] [7]. The remaining noise can be evaluated using a statistical method to process measured data from the sensors in standard operating condition and without illumination. The resultant noise distribution has a characteristic thermal noise peak with a trapping noise tail.

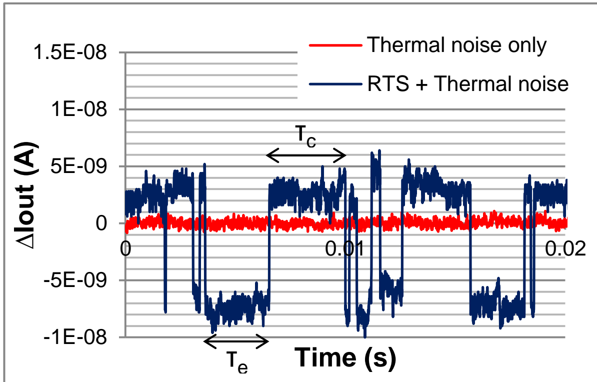

Figure 5: Output signal of a P-type SF presenting thermal noise (red) and RTS noise (blue).

Figure 6 plots noise distributions of both PMOS and NMOS having the same size and at the same bias current level. The thermal noise peak for both types is almost the same in height and in position, but P-type SF exhibits a much lower RTS tail than the N-type case.

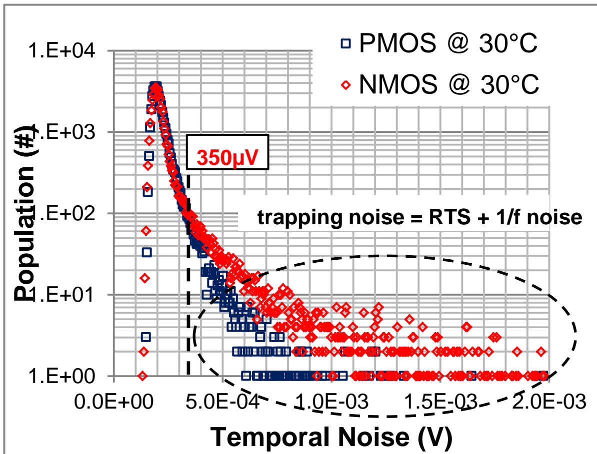

Figure 6: Statistical noise distributions of PMOS and NMOS as SF, in the same operating conditions: |Vgs| = 0.9V, |Vgb| = 2.5V, |Ids| = 2µA, at 30°C.

Assuming that RTS only accounts for noise with levels over 350µV, its average contribution to the total temporal noise is decreased by a factor of three for P-type SF compared with N-type one (see figure 7). These results are in agreement with studies presented in [3] and [8].

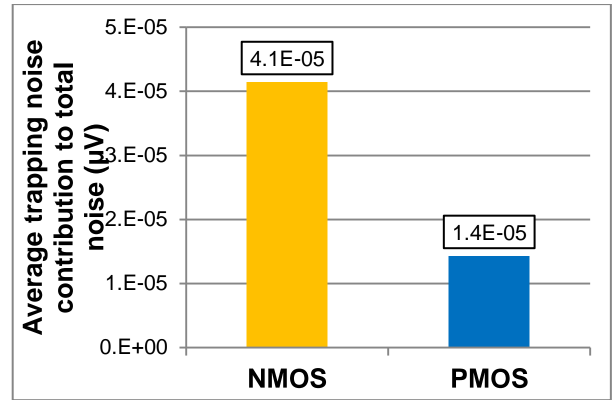

Figure 7: Comparison of average trapping noise between NMOS and PMOS in the same operating conditions: |Vgs| = 0.9V, |Vgb| = 2.5V, |Ids| = 2µA, at 30°C.

Fig. 8 shows bias and sizing impacts on the SF's noise. At high current density (|Ids| = 4µA), no significant difference in noise distribution is observed for different sizes. However, for |Ids| below 1µA the shift of the distribution peak indicates a thermal noise dependence on L/W.

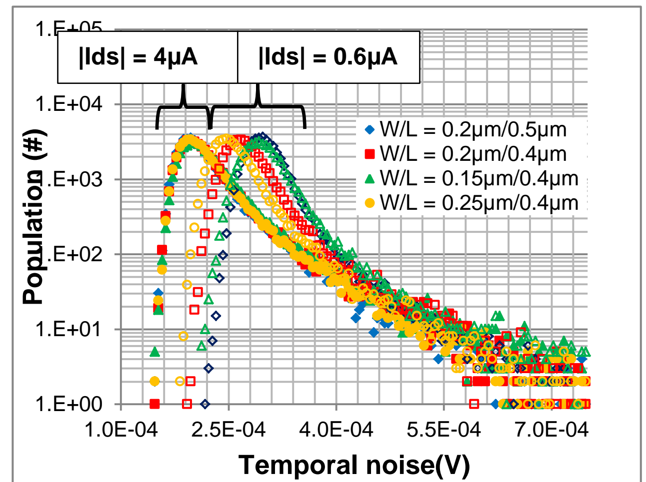

Figure 8: Statistical noise distributions of PMOS SF of different sizes in the operation conditions: Vgs = -0.9V, Ids = -4µA (full) or -0.6µA (hollow), at 30°C.

This is because its noise power density is inversely proportional to the transconductance (gm) of the transistor. At higher current, when gm reaches its maximum value, the minimal thermal noise is observed and size variations do not matter anymore. It should be noted that regardless of the current density, no significant impact is observed on the trapping noise tail from the geometrical variations.

Pixel characteristics

P-type pixel arrays with design variations were fabricated and tested (see Figure 9).

Figure 9: Picture taken with one P-type sensor for testing. The sensor integrates fifteen different pixel design variations each having more than 200000 pixels.

Electro-optical characterizations gave a conversion factor of $134\mu V/h^+$ and a FWC over $7000h^+$. These results are comparable with the N-type pixel. The average temporal noise of the P-type SF is around 195µV at room temperature, compared to 224µV for the N-type counterpart. Other tests are under way. Table 1 compares the obtained characteristics between the two types of pixels.

Table 1: Comparison of characteristics between the P-type pixel and the N-type one

Parameter	**P-type**	**N-type**
Pitch	1.4µm	1.4µm
BSI	Yes	Yes
CVF	$134\mu V/h^+$	$149\mu V/e^-$
Full well capacity (FWC)	$>7000h^+$	$7000e^-$
SF temporal noise (average)	195µV	224µV
Trapping noise contribution to SF temporal noise	14µV	41µV

Conclusion

We have proposed a P-type BSI pixel and implemented in a shared 2T architecture. The implementation includes process optimization of hole-collection and vertically-pinned photodiode as well as transfer gate. Test results on the 1.4µm-pitch pixel show a full well capacity exceeding $7000h^+$ and a conversion factor of $134\mu V/h^+$. PMOS source follower has a much lower trapping noise than the NMOS counterpart. The use of P-type pixel components may improve performances of CMOS image sensors, such as low-noise achievement.

Acknowledgement

The authors would like to thank the entire process integration imager team at STMicroelectronics as well as the Design, TCAD, Front-End Manufacturing and Electrical Characterization groups for their dedicated support and invaluable help.

Reference

[1] E. Stevens, H. Komori, H. Doan, H. Fujita, J. Kyan, C. Parks, G. Shi, C. Tivarus and J. Wu, "Low Crosstalk and Low-Dark-Current CMOS Image Sensor Technology Using a Hole-Based Detector," in *IEEE ISSCC*, 2008.

[2] S. Place, J.-P. Carrere, S. Allegret, P. Magnan, V. Goiffon and F. Roy, "Rad Tolerant CMOS Image Sensor Based on Hole Collection 4T Pixel Pinned Photodiode," *IEEE Trans. on Nucl. Sc.,* vol. 59, no. 6, pp. 2888-2893, 2012.

[3] J. Tower, J. Janesick, T. Senko, P. Levine, M. Grygon, J. Andrews, J. Zhu, T. Vogelsong, G. Yang, S. Huang, C. Sun and B. Mansoorian, "BSI Low Light Level CMOS Image Sensor Employing P-type Pixel," in *IISW*, 2013.

[4] A. Tournier, F. Leverd, L. Favennec, C. Perrot, L. Pinzelli, M. Gatefait, N. Cherault, D. Jeanjean, J.-P. Carrere, F. Hirigoyen, L. Grant and F. Roy, "Pixel-to-pixel Isolation by Deep Trench Technology: Application to CMOS Image Sensors," in *IISW*, Hokkaido, JAPAN, 2011.

[5] J. Michelot, F. Roy, J. Prima, C. Augier, F. Barbier, S. Ricq, P. Boulenc, Z. Essa, L. Pinzelli, H. Leininger, M. Gatefait and J.-E. Broquin, "Back Illuminated Vertically Pinned Photodiode with in Depth Charge Storage," in *IISW*, Hokkaido, 2011.

[6] P. Martin-Gonthier and P. Magnan, "RTS Noise Impact in CMOS Image Sensors Readout Circuit," in *16th IEEE ICECS 2009*, Hammamet, 2010.

[7] K. Findlater, J. M. Vaillant, D. J. Baxter, C. Augier, D. Herault, R. K. Hendernson, J. Hurwitz, L. A. Grant and J.-M. Volle, "Source follower noise limitations in CMOS active pixel Sensors," *Detectors and Associated Signal Processing. Proceedings of the SPIE.,* vol. 5251, pp. 187-195, 2004.

[8] K. Abe, S. Shigetoshi, K. Rihito, W. Shunichi, M. Naoto, T. Akinobu, O. Tadahiro, K. Yutaka and S. Katsuhiko, "Analysis of Source Follower Random Telegraph Signal Using nMOS and pMOS Array TEG," in *IISW*, Ogunquit, 2007.