A 0.4 e⁻$_{rms}$ Temporal Readout Noise 7.5 µm Pitch and a 66% Fill Factor Pixel for Low Light CMOS Image Sensors

Assim Boukhayma[1,2], Arnaud Peizerat[1] and Christian Enz[2]

[1] CEA-LETI, Grenoble, France
[2] ICLAB, EPFL, Switzerland

assim.boukhayma@epfl.ch, *arnaud.peizerat@cea.fr*, *Christian.enz@epfl.ch*

Abstract

This paper explores a new way to reduce the readout noise for CMOS image sensors by using a typical 4T pixel embedding a PMOS source follower with reduced oxide thickness and gate dimensions. This approach is confirmed by a test chip designed in a 180 nm CIS CMOS process, and embedding small arrays of the proposed new pixels together with state-of-the-art 4T pixels for comparison. The new pixels feature a pitch of 7.5 µm and a fill factor of 66%. A 0.4 e⁻$_{rms}$ input-referred noise and a 185 µV/e⁻ conversion gain are obtained. Compared to state-of-the-art pixels, also present onto the test chip, the RMS noise is divided by more than 2 and the conversion gain is multiplied by 2.2.

I. Introduction

During the last few years, it has been shown that the temporal noise of CIS readout chains can be reduced slightly below the 1 e⁻$_{rms}$ barrier using circuit techniques, namely, high column amplification and correlated multiple sampling (CMS), combined with device optimization like in-pixel buried channel source follower [1] or in-pixel open-loop gain based on a PMOS transistor [2]. These achievements were obtained at the cost of a large pixel pitch and a lower fill factor. It is known that the 1/f noise originating from the in-pixel source follower becomes the dominant noise source when the thermal noise is reduced using high column amplification or CMS [3]. This work explores a new way to further reduce the 1/f noise originating from the in-pixel source follower. The proposed pixel based on the latter achieves a noise reduction of more than 50% with a reasonable pixel pitch of 7.5 µm and a fill factor of 66%.

II. The new noise reduction technique

It has been shown that buried channel transistors feature lower 1/f noise compared to surface channel transistors. This is due to the fact that the 1/f noise is a result of the process of trapping and de-trapping at the silicon silicon-oxide interface. It is also known that the gate oxide thickness reduction comes with a higher electrical field density and hence a better control of the gate over the channel. Thus, gate oxide reduction is also expected to reduce 1/f noise. In order to combine the two noise reduction mechanisms, this work presents a new low noise CIS pixel based on a PMOS source follower transistor with a reduced gate oxide thickness.

CIS process flows use thick oxide to support high voltages needed to achieve acceptable voltage swings, to reduce leakage currents and for difficulties to downscale pinned photodiodes. In order to overcome these limitations, in this work, only the source follower transistor gate thickness is reduced. Fig. 1 shows the circuit schematic of the proposed pixel together with a

conventional pixel. The PMOS source follower is biased to keep the voltage difference between all its four terminals below 1.8 V while keeping the output voltage swing of the pixel over 1.5 V. The new pixel is integrated in a 180 nm CIS process. It features a 7.5 µm pitch and a 66% fill factor. The new pixel is combined with high column amplification as shown in Fig. 1 in order to reduce thermal noise.

III.   Test description

In order to evaluate the impact of the proposed noise reduction technique, the classical NMOS source follower reference pixel shown in Fig. 1 (a), embedding a source follower dedicated for low light CIS and already optimized for low noise by the foundry, has been integrated in the same chip together with the new proposed pixel shown in Fig. 1 (b). The 1×5 mm^2 test chip is designed in a 180 nm CIS process. The pixels are made of 4 transistors and a standard pinned photo diode. The reference pixel features a pitch of 6.5 µm. A micrograph of the test chip is presented in Fig. 2. The chip includes a total of 24 pixels of new and reference pixels. Each pixel is surrounded by 8 dummy pixels for proper characterization and each pixel is connected to its own column amplifier offering an adjustable gain between 8 and 64 in order to verify the impact of column gain on noise. The column amplifiers also limit the bandwidth of the readout chain to 265 kHz.

In order to measure the input referred noise, the conversion gain of the overall readout chain is first measured at low column gain using the photon shot noise. The conversion gain at high column gain is obtained after measuring the ratio between high and low gain. This ratio is measured by closing the reset switch (RST) and using the reset voltage (V_{RST}) as an input (Fig. 1). Then, the RMS read noise is measured at the output of the readout chain using an external 14 bits ADC. The noise is then referred to the input using the measured readout chain conversion gain.

IV.   Measurement results

The conversion gain is measured using the photon shot noise property. Fig. 3 (a) shows, for both the new and reference pixels, the plot of the variance as a function of the mean value of the signal voltage at the output of the readout chains for different amounts of received photons. The points obtained for both pixels are well aligned. The conversion gain is obtained by estimating the slopes of both curves. The new pixel features a conversion gain of 185 µV/e$^-$ compared to 85 µV/e$^-$ for the reference pixel. The output noise is then measured for all the 24 readout chains of 7 different chips using a 14-bits ADC with a CDS of 3 µs and a column amplifier bandwidth limited to 265 kHz. Fig. 4 shows the histograms of the measured input-referred noise obtained with all the new and reference pixels (84 each) with a column level gain set to 64. The new pixel features an average input-referred noise below 0.4 e$^-_{rms}$, compared to 0.9 e$^-_{rms}$ for the reference pixel. In addition, the histograms show that the standard deviation of the measured noise for the proposed pixel is three times less than the reference pixel. Fig. 3 (b) shows the impact of the column gain on the measured input-referred noise.

As expected, the reference pixel used for comparison and already optimized by the foundry for low noise shows a state-of-the-art performance. But the new proposed pixel features a very promising result of 50% noise reduction and 2.2 times higher conversion gain compared to the reference pixel integrated on the same chip for the same 1.5 µA pixel bias current.

The test results presented in this paper are summarized in Table I and compared to other sub-electron rms pixels integrated in similar 180 nm CIS processes [1] [2]. The new proposed pixel offers significantly lower noise with a smaller pixel pitch and higher fill factor.

V. Conclusion

A new pixel, featuring a pitch of 7.5 µm and 66% fill factor, has been designed to explore a new way to further reduce the temporal read noise. It is based on a standard 4T pixel embedding a PMOS source follower with reduce oxide thickness. The proposed pixel is designed with a 180 nm CIS process and integrated on the same chip with a conventional 4T pixel with a source follower already optimized for low noise. The test measurements show that the new pixel features an input-referred noise of less than 0.4 e$^-$$_{rms}$ for a column gain of 64 without using multiple sampling, and a conversion gain of 185 µV/e$^-$. Compared to the reference pixel integrated on the same chip, the new pixel shows a noise reduction of more than 2 and a pixel conversion gain increase of more than 2.

References

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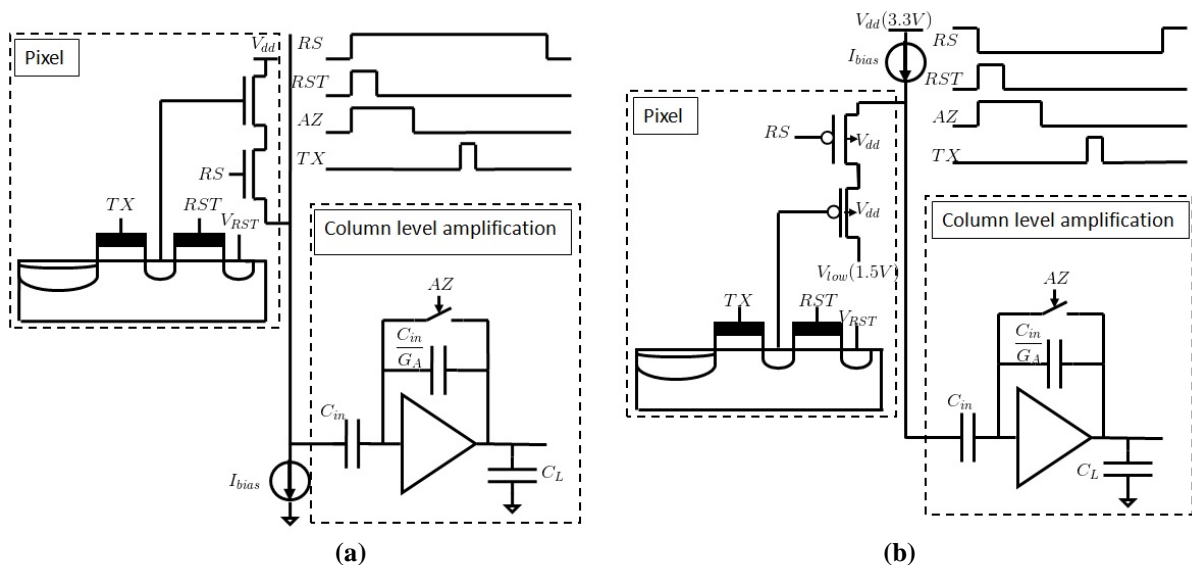
(a)   **(b)**

Figure 1 Schematics of the CIS readout chains based on the reference pixel (a) and on the new pixel (b)

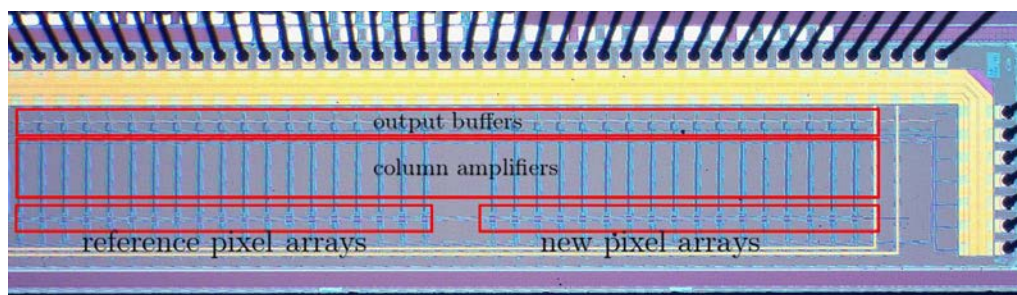

Figure 2 Test chip micrograph

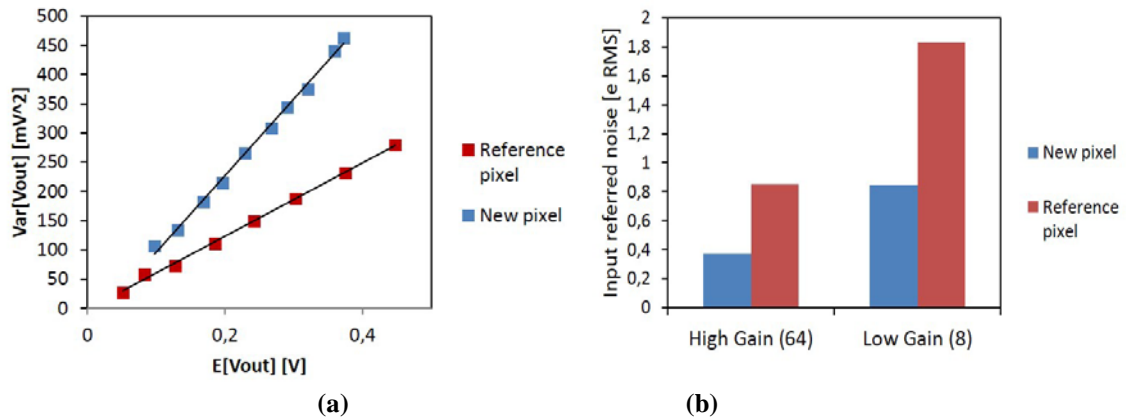(a)   (b)

**Figure 3 Measurement of the overall conversion gain with a column level amplification of 8 (a)
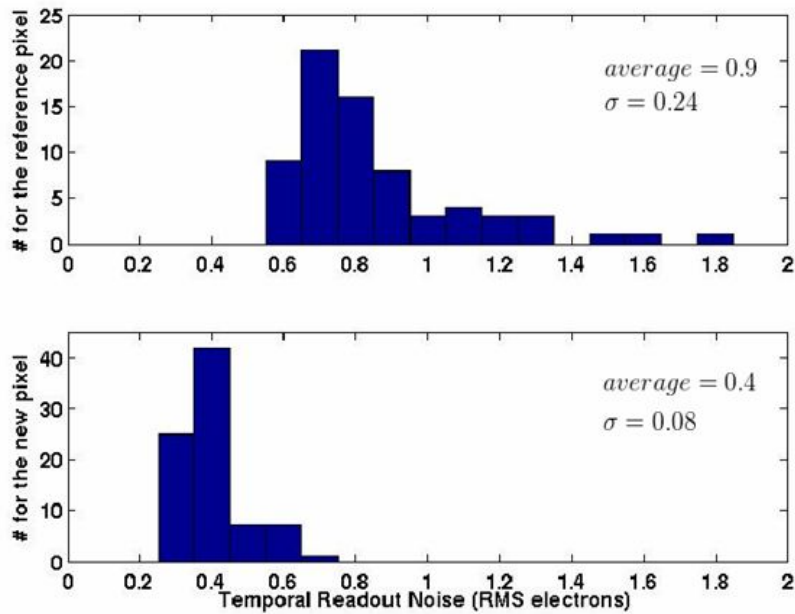and the input referred noise for high and low column gain (b)**

**Figure.4 Histograms of input referred noise of readout chains based on the reference pixel and the new
pixels for a column gain of 64**

Table I Comparative table with recently reported low light CIS all integrated in 180 nm CMOS processes dedicated forCIS

Technique	Noise [e⁻$_{rms}$]	Conversion gain [μV/e⁻]	Pixel pitch [μm]	Fill factor [%]	Reference
PMOS common source pixel amplifier	0.86	300	11	50	[2]
Buried channel NMOS source follower, column gain and CMS	0.7	45	10	33	[1]
Optimized PMOS source follower and column amplification	**0.4**	**185**	**7.5**	**66**	**This work**