CMOS image sensor reaching 0.34 e^-_{RMS} read noise by inversion-accumulation cycling

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Abstract

This work presents the design and evaluation of a 0.18 µm technology 16*16 pixels prototype CMOS image sensor with a measured read noise below 0.34 e^-_{RMS}. This result is obtained by the combination of severe oversampling and inversion-accumulation cycling.

Design Concepts and Operation Principle

Except for photon shot noise (PSN), almost all image sensor noise sources can be cancelled, calibrated or reduced arbitrarily. In a very well calibrated camera system, in the dark and at low temperature, source follower 1/f noise turns out to be the hardest to cancel and eventually becomes the dominant remaining noise source.

In [1], we proposed and demonstrated a technique to cancel also this MOSFET 1/f noise contribution. The method is essentially based on:

→ Removing the time-correlation of the 1/f noise by cycling repeatedly the MOSFET between accumulation and inversion, during one readout moment.

→ Oversampling the pixel's signal when the MOSFET is in inversion.

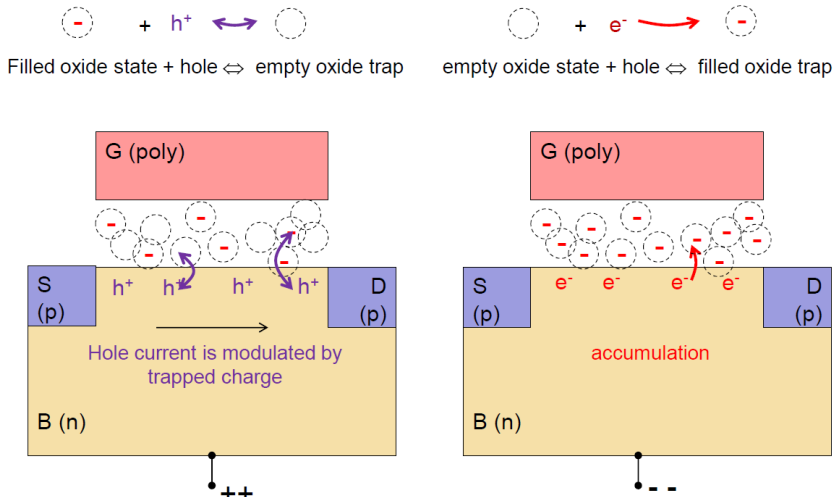

Figure 1 pMOSFET 1/f noise

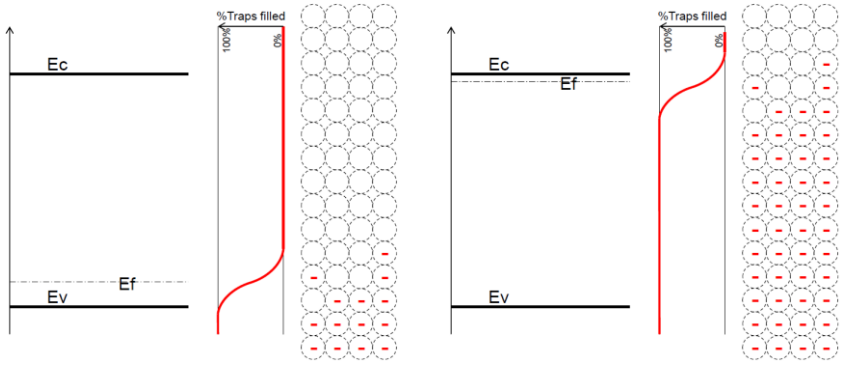

Figure 2 Fermi statistics of interface states

Based on the McWorther model for 1/f noise, the 1/f noise is caused by carries transitions between interface states (traps at Si/SiO_2 interface) and silicon conduction band (inversion layer). [2] The time constants of those transitions vary from less than nano second to days, the long correlation time is responsible for the 1/f spectrum. As consecutive samples are strongly correlated, oversampling does not help.

When MOSFET is biased to accumulation state, for a pMOSFET, its Fermi level is higher than interface state. All traps are quickly filled with electrons and lose their long term memory. And when the pMOSFET comes back to inversion, traps' memories are erased and correlation time is reset to zero and spectrum of the read noise between different

cycling becomes “white”. [3, 4] The principle is shown in Figure 1 and Figure 2.
As far as the samples are uncorrelated, the voltage read noise can be arbitrarily reduced by increasing the number of samples.

Measurement Setup

The schematic of pixel and readout circuit is presented in Figure 3. The imager (ZPS2) layout and chip on CoB are shown in Figure 4.

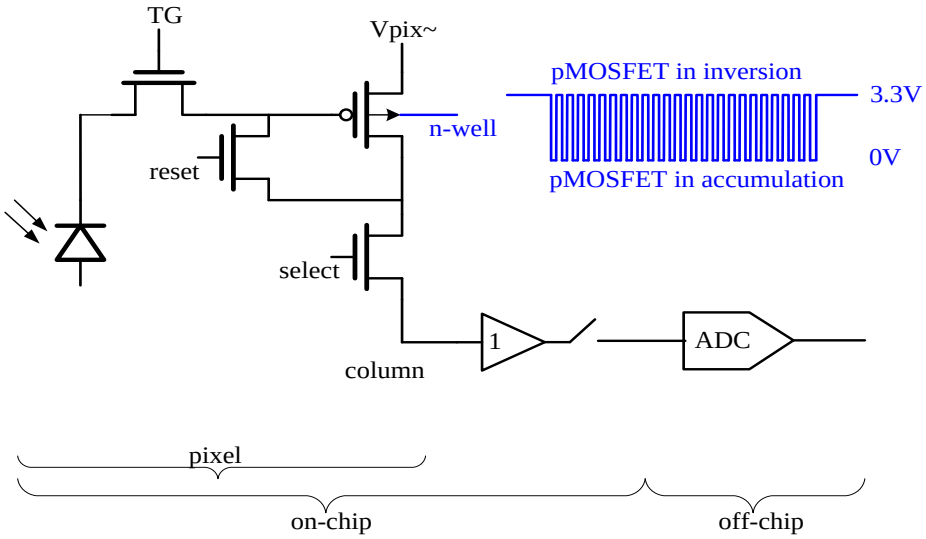

Figure 3 schematic of pixel and readout circuit

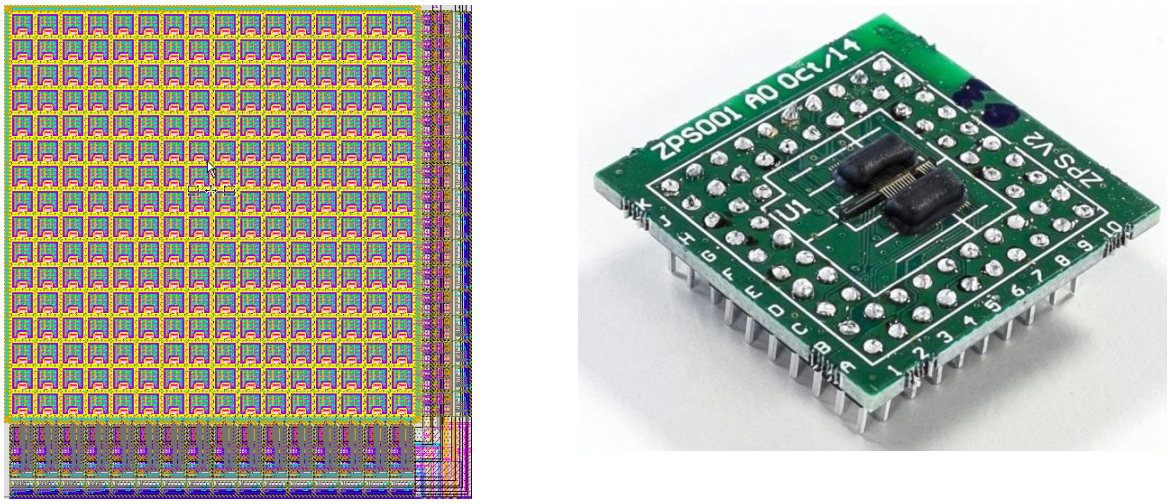

Figure 4 ZPS2 imager core layout (left) and IC on its CoB package (right)

ZPS2 key features and nominal operation conditions:

Technology	180nm CMOS, 3.3V option	Operation temperature	27°C→-40°C
Pixels	16x16	Sample frequency	50kHz
Pitch	25µm	Illumination condition	Dark
Pixel type	4T CTIA with pMOSFET	Accumulation time/Inversion time	16
Interface	Direct analog	CDS	digital
N-well amplitude	Between 0V and 3.3V	#oversamples or #cycles	1 to 1600
CVF	392-402 µV/e- Between -40°C and +27°C +/-3% +/-1%	Acquisition system	Caeleste in-house

Results and Interpretation

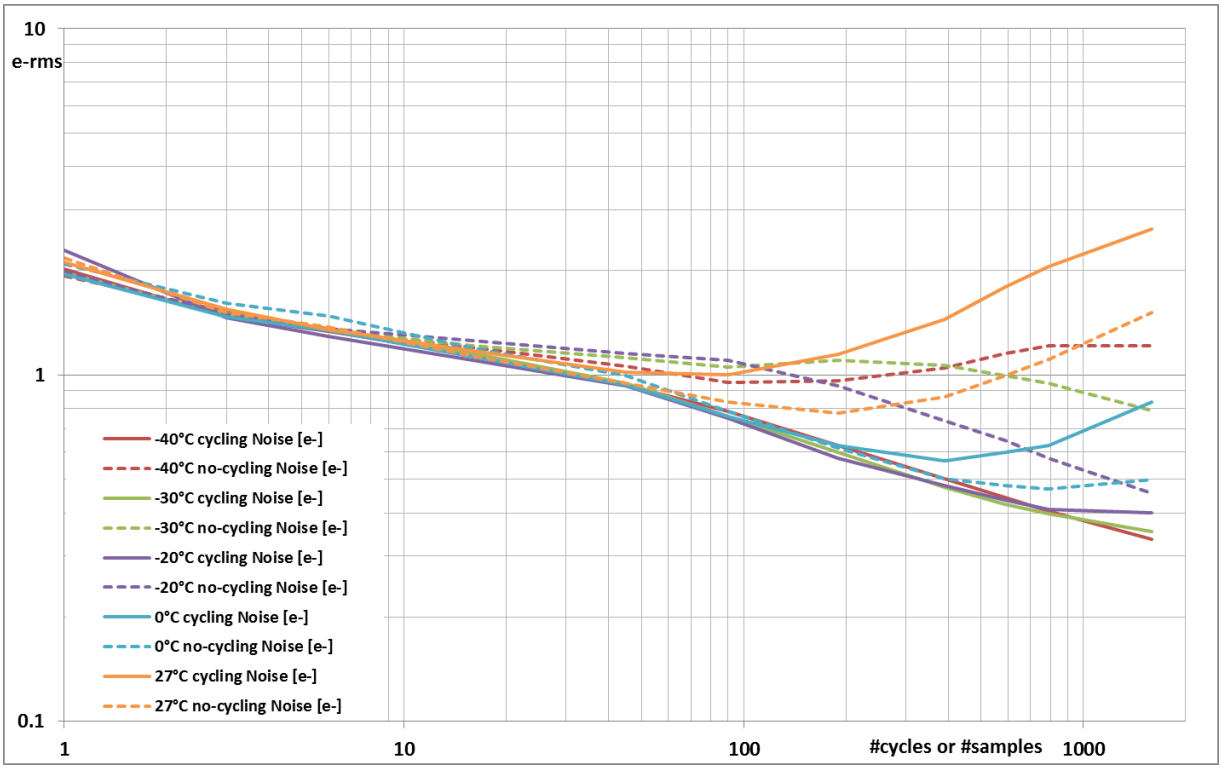

Figure 5 Read noise as function of #cycles or #samples at different temperature

At room temperature, the read noise decreases when the sample number goes from 1 to about 50. Clearly oversampling decreases the white noise, yet when going above this number the time between reset level and signal level acquisitions grows, increasing thus also the FD's integrated dark current and making DCSN the dominant noise source. The situation improves considerably at lower temperature. At -40°C, cycling with 1600 samples, the read noise touches $0.33e^-_{RMS}$; we did not exploit even lower temperature an even high number of samples.

The difference between cycling and no cycling is obvious, especially where the impact of DCSN is suppressed by cooling.

One sees in this graph especially at 27°C and 0°C, cycling adds an extra noise that seems to increase with #cycles as would DCSN do. We have no explanation for that. It may point to other correlated RTS-like or 1/f like noise sources as suggested in [4]? At very low temperature this effect is probably shifted sufficiently of the right edge of the graph.

The limit of "Photon Counting" Accuracy

In Figure 6, a *hypothetical* series of 50 consecutive readings of a pixel signal with a 0.25 $electrons_{RMS}$ read noise is shown. As an exercise of thought we re-sample all readings by rounding to the nearest integer number of electrons, and then re-calculate the effective read noise. We can do that as a Monte Carlo experiment for a range of hypothetical read noise levels, as in Figure 7. We see that, when the initial read noise is sufficiently below 0.28 noise e^-_{RMS}, the re-sampled read noise becomes quickly lower than that original value. In practice: it becomes possible to really see steps in the signal, which steps correspond to a signal difference of 1 electron.

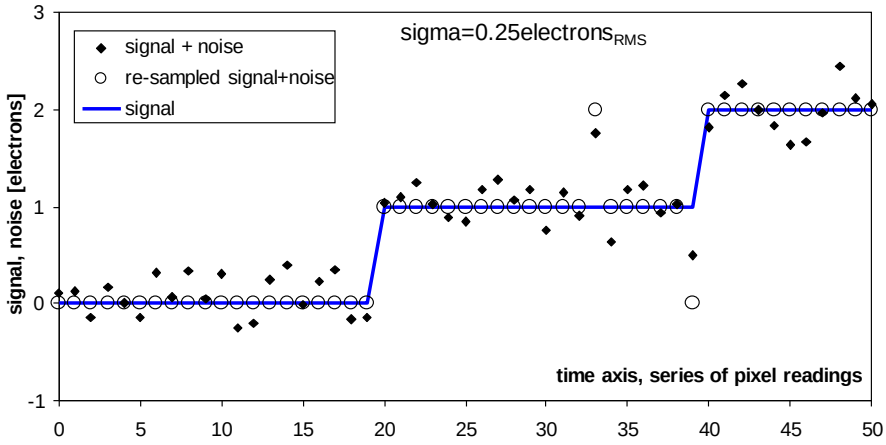

Figure 6 signal + synthetic read noise sequence, re-sampled to the nearest integer #e-

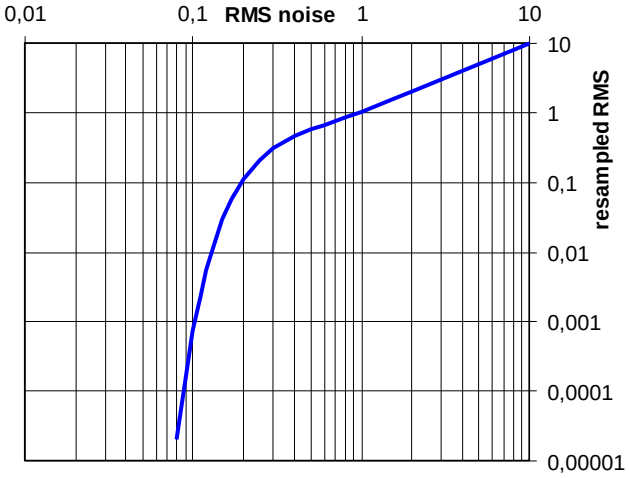

Figure 7 Monte Carlo experiments synthetic raw noise magnitude varied between 0.01 and 10 e^-_{RMS}. Plotted raw noise [e^-_{RMS}] vs. resampled noise [e^-_{RMS}].

Below 0.28 e^-_{RMS}, the resampled noise starts becoming lower than the raw noise.

Conclusions

There is a clear effect of the inversion-accumulation cycling on the noise. Part of that is due to the oversampling, cancelling all contributors except 1/f noise, part of it is due to the cycling presumed to uncorrelate the 1/f noise, making it subject to oversampling. Depending on the operation temperature, the useful number of oversamples is limited, likely by the contribution of DCSN.

It is interesting to observe, and not properly explained, that the cycling operation itself has also an effect that looks like the effect of an increased DCSN.

This effect and the observation that the improvements factor is finite may lead us to conclude from physics standpoint that the McWorther model for 1/f noise is incomplete. It looks as if a simple capture&emission of carriers in interface states, with or without mobility fluctuation, is not the full story behind 1/f noise.

Still further improvements may be reached such as adjusting the circuit parasitics so that a deeper accumulation can be reached; in the measurements setup to reach a high number of cycles and a lower temperature; and from technology standpoint migrating to thinner oxide MOSFETs known to have a priori a lower 1/f noise.

References

[1] B. Dierickx, N. Ahmed, B. Dupont, "A 0.5 noise electrons$_{RMS}$ CMOS pixel," Workshop on "CMOS detectors for high performance applications", Toulouse, Dec, 6, 2011.

[2] M. J. Kirton and M. J. Uren, "Noise in solid-state microstructures: A new perspective on individual defects, interface states and low-frequency (1/f) noise," Adv. Phys., vol. 38, no. 4, pp. 367–468, 1989 .

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[4] B. Dierickx and E. Simoen, "The decrease of 'random telegraph signal' noise in metal-oxide-semiconductor field-effect transistors when cycled from inversion to accumulation," J. Appl. Phys., vol. 71, no. 4, pp. 2028–2029, Feb. 15, 1992.