High Performance 1.3MPix HDR Automotive Image Sensor

Tarek Lulé[1,4], Christophe Mandier[1], Arnaud Glais[1], Gregory Roffet[1], Roger Monteith[2], Benoit Deschamps[1] , Didier Herault[3]

1: STMicroelectronics, Imaging Division, 12 rue Jules Horowitz, B.P.217, F-38019 Grenoble, France
2: STMicroelectronics, Imaging Division, 33 Pinkhill, Edinburgh, EH12 7BF UK
3: STMicroelectronics, Crolles, To be Completed
4: Phone: +33 476 58 59 35, Email: tarek.lule@st.com

Abstract

A novel pixel and image sensor for automotive applications is present. By combining process advancements from consumer application with automotive technology and design, the optimal high dynamic range 1.3MPixel automotive image sensor is realized. It achieves very good low light performance due to very high conversion gain and low noise readout. Selectable triple High/Medium/Low conversion gains are realized without compromising floating diffusion capacitance. The image sensor architecture is tuned for high dynamic range automotive requirements.

Introduction

Automotive applications of CMOS image sensors are rapidly growing in the coming years [1]. While the bulk of CMOS imagers are optimized for very high resolution, price sensitive consumer expectations, very high performance niche applications are served by expensive, bulky application specific image sensors. The automotive requirements lie somewhere in between these two worlds: uncontrolled external environment imposes very high dynamic range capability while excellent low light performance is a must for night driving, driving for relatively large pixels. On the other hand, moderate resolutions are sufficient for displaying as well as machine vision usage, and allow keeping the price down. Very low power consumption is also important due to very high possible ambient temperatures and the self-heating of the camera body.

Pixel Design

In order to be more flexible to handle extreme situations such as very strong day light and very low night time drive, the pixel has been equipped with a novel 5T pixel circuitry as shown in Figure 1. This 3.75um pixel design provides three different conversion gains depending on the signal drives. While M1, M4, M5 operate as normal TG and SF, the reset circuitry uses two Transistors in series M2, M3, the common diffusion of those being connected between pairs of pixels.

In high conversion gain mode, M3 is permanently on, and M2 serves as normal reset transistor. In this mode, the extra circuitry does not load the floating diffusion with additional Drain(-Gate) capacitances achieving a very high conversion gain of 160uV/el suitable for lowest light scenes. In the low conversion gain mode, both M2s are permanently on, while the M3s serve as reset transistor. With this small effort, conversion gain plummets to 28uV/el providing ~40ke full well – ideal for high light and flickering light sources. A medium conversion gain mode is possible by activating only the one M2 of the pixel being read while still using any of the M3s for reset.

The described pixel is realized in our 65/90nm FSI technology, where a minimum pixel-level illumination to achieve an SNR=1 has been squeezed down to ~1mlx at 6500K illumination and 30msec integration due to thanks to the very high conversion gain. The green QE peaks at respectable 63% for a FSI technology (see Figure 3). The near infrared QE is boosted to >20% at 850nm though a deeper EPI. This is important for machine vision applications, as e.g. the forward

facing camera used for advanced driving assistance. Dark currents measured as low as only 70e/sec at 60ºC junction temperature allow an operation of up to 105ºC junction temperature in daylight situations, where integration times can be chosen shorter (ref. Figure 4). Another key advantage of the pixel design and technology are the extreme large acceptance angles, horizontally and vertically (Figure 5 and Figure 6 respectively), due to the very low optical stack. This allows for very large F-Number lenses without any penalty in SNR even at the edge of the field [2].

Imager Architecture (Figure 8)

Pixel readout is accelerated through the dual vertical readout lines per column, allowing reading two exposures at once. Further, four 10b single slope ADCs per Column, two on top and bottom each (cf Figure 8), provide further acceleration at lower power consumption compared to previously presented architectures using the same triple exposure HDR approach [3]. Referring to Figure 7, first the two rows containing the medium and short exposures are addressed simultaneously. Their signal and reset values are sampled through a S&H stage (SH1, SH2) while the two top ADCs are auto-zeroed (AZtop). Since medium and short exposures are used at high light, their kTC noise has no impact on image quality. Subsequently the row containing the long exposure is addressed, and the two bottom ADC auto-zero (AZbot) performed on the reset value. This signal is read out continuously for lower noise, while the single slope ramp is launched to convert all 4 ADCs at once. One of the two bottom ADCs has a built-in gain of 4x, which allows the two 10b data to be combined to deliver 12b data for the long exposure.

Very high, 132dB, dynamic range is achieved through the combination of the high native pixel dynamic range of 72dB with triple exposure as used many times before. Intermediate storage of up to 128 lines are provided to realign the long with medium and short exposure data. A critical element in this architecture is the intelligence put into the merge of the three exposed images. A wide choice of merge modes is implemented in this sensor, which can be configured to provide the optimum image at different lighting situations. A 32 segment PWL provides smooth compression of the 22bit HDR signal into a 12b output word. The compression can be tuned for example such that no missing codes occur up to the saturation level. Or alternatively it can be used as a tone-mapping stage for direct machine vision processing of the resulting compressed image. Parallel and dual lane CSI2 interfaces are both supported since they are the most wide spread interfaces in automotive companion chips. The sum of all these features explains the large gate count and digital area of the sensor system.

Automotive Safety Features

With increasing impact of the camera system on driving safety, the need for additional safety support elements has become mandatory in the camera system. The image sensor supports the stringent safety requirements through a list of safety features such as analogue and digital ASIL stimulus pixels.

Figure 2 shows the approach we chose to provide an analogue test stimulus: a resistor ladder creates a ramp voltage left to right and right to left respectively. The voltages are sampled by the equivalent pixel circuits and read out through the same ADC architecture chain. The resulting signal ramps are sent out as trailing data appended to the visible image data.
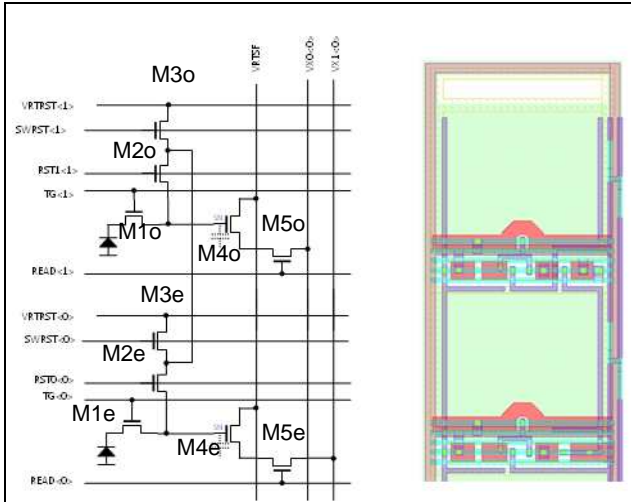
Figure 1, 5T Pixel design and layout providing triple conversion gain and dual VX readout
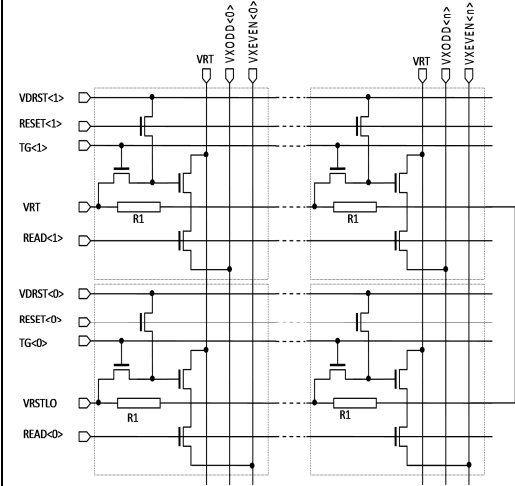

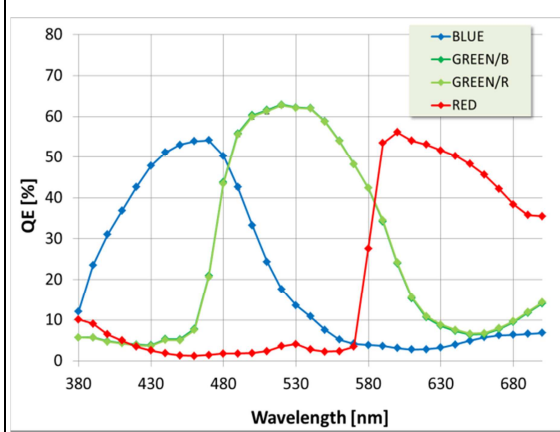Figure 2, Two Rows of Analogue Stimulus Pixels for Real Time Self Testing

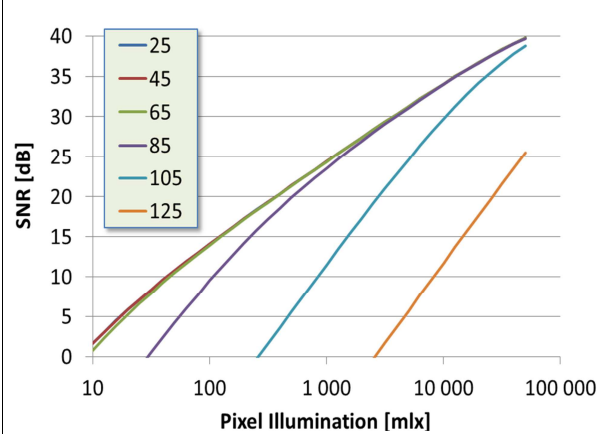Figure 3, Quantum Efficiency RGB Pixels

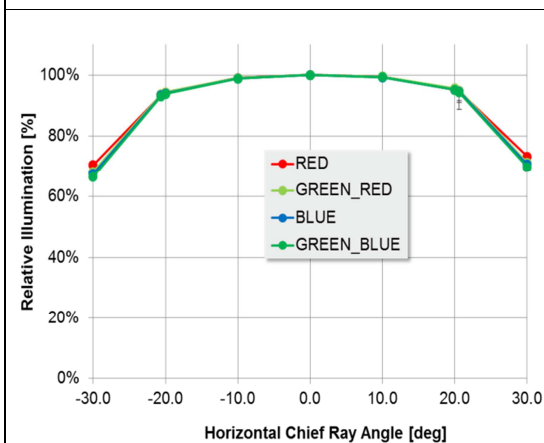Figure 4, SNR Curves versus Pixel Illumination at different Junction Temperatures

Figure 5, Relative Illumination versus Horizontal Tilt of Chief Ray Angle (No Radial Shift)
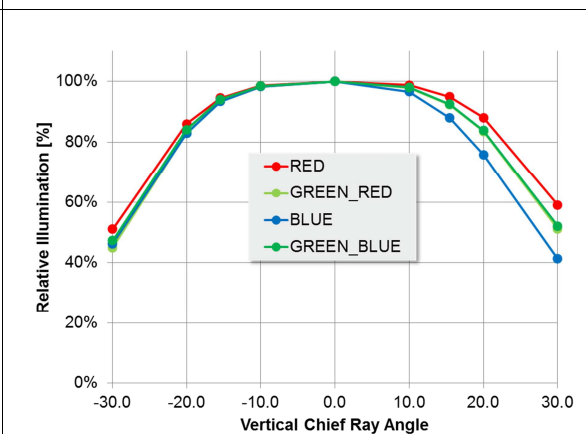

Figure 6, Relative Illumination versus Vertical Tilt of Chief Ray Angle (No Radial Shift)
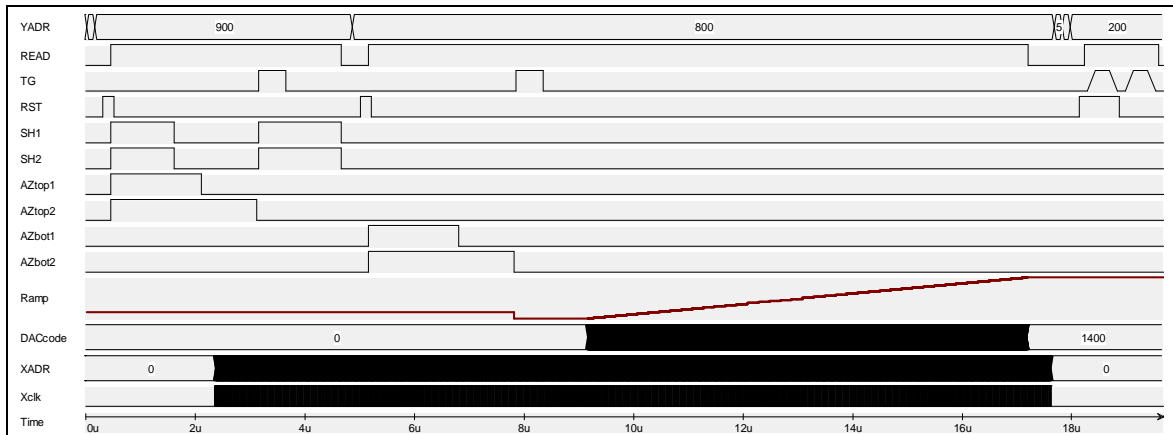
Figure 7, Timing to Operate Four Top and Bottom ADCs to convert 3 Integration Times at once
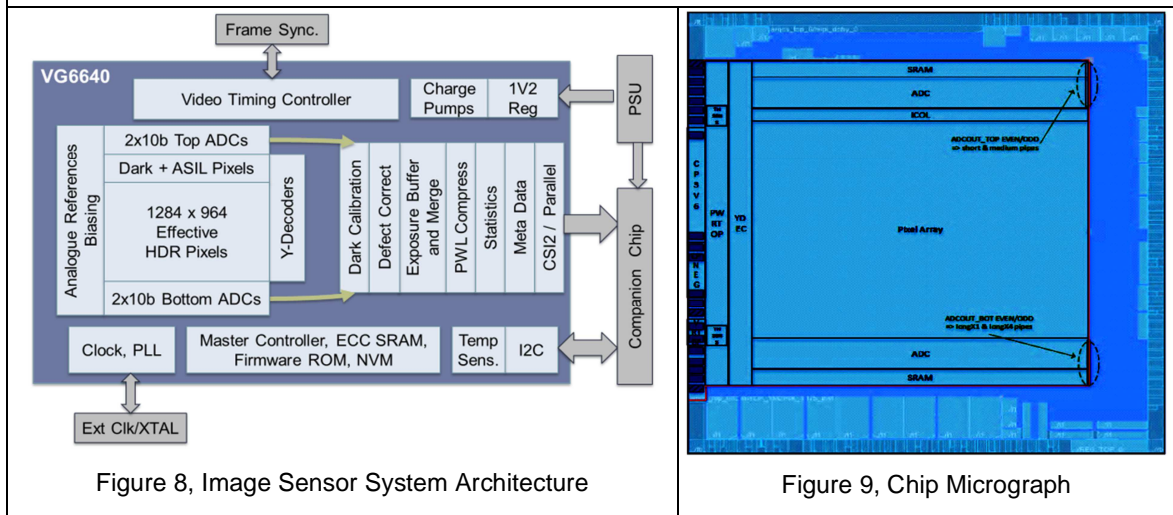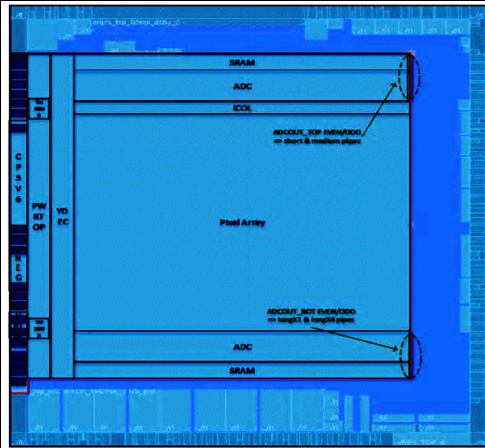

Figure 8, Image Sensor System Architecture

Figure 9, Chip Micrograph

Parameter	High Conversion Gain	Low Conversion Gain
Maximum Full Well	6 ke-	40 ke-
Read Noise (AG=1)	2.0e-	7e-
Read Noise (AG=4)	1.5e-	7e-
Maximum SNR	37 dB	43 dB
PRNU	0.6%	
Peak QE 550nm	63%	
Dark Current @ 60ºC	70aA	
Pixel Size	3.75um	
Full Resolution	1304 x 990 Pixels	
Gate Count	1.08 Mio Gates	
Chip Size	7194 x 7842 = 56.4 mm^2	
Maximum Frame Rate	45 fps	
Power Consumption	390mW @ 30fps	

Figure 10, Image Sensor Performance Characteristics

[1] See For example "CMOS IMAGE SENSOR 2015" market analysis by Yole, http://www.yole.fr/CIS_2015.aspx

[2] A. Johannesson, and H. Eliasson, "Image sensor performance from a security camera perspective", 2013 INTERNATIONAL IMAGE SENSOR WORKSHOP, Snowbird Resort, USA, June, 2013

[3] J. Solhusvik et al., „A 1280x960 3.75um pixel CMOS imager with Triple Exposure HDR", Workshop on CCDs and AIS, Bruges, Belgium, June 1999