A 120dB DR and 5µm pixel pitch imager based on local integration time adaptation

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In order to preserve details in both very dark and very bright parts of the image, numerous imaging applications, e.g. automotive or video-surveillance, require the acquisition of High Dynamic Range (HDR) images, i.e. typically above 100dB. “Bracketing”, i.e. the successive acquisition of several Low Dynamic Range (LDR) images with different exposure times, is one way to circumvent this issue when using a conventional LDR sensor, which has a typical DR of 60dB. This widespread technique shows good results at the cost of a great reduction in the acquisition speed, a larger memory requirement and a higher power consumption. Hence a strong demand arises for HDR image sensors whose intrinsic dynamic is above 100dB along with an unmitigated frame rate. The Dynamic Range (DR) is defined as the ratio of the maximum acceptable signal, i.e. the signal just before saturation, over the minimum detectable signal, i.e. the noise floor. The noise floor has been widely improved to the point that the best equivalent input noise is now below one electron [1]. On the opposite, state of the art architectures that extend the DR upper part, i.e. accepting still higher light levels, suffer from limitations such as adding circuitry to the pixel like in [2,3] or requiring the readout circuitry to be faster like in [4, 5] or undergoing a large SNR dip as described in [6]. Our new HDR architecture is intended to add the HDR feature to an imager without any modifications in its specifications (speed, noise floor, pixel scheme, etc…). Using a classic 0.18µm process, this architecture has been implemented in an 800x512 proof-of-concept imager with a 5µm pixel pitch and features a 120dB DR. Mapping this architecture on a 3D-IC technology, in a next step, will bring fully optimized capabilities.

Figure 1 shows the fabricated 2D-IC architecture as well as the targeted 3D-IC one. The dark blue blocks, further referred to as “primary” image sensor blocks, are common to both architectures and could be part of any image sensor. The light blue blocks are added to provide the HDR feature to this primary image sensor. Without changing the pixel architecture (3T or 4T), the technique consists in dividing the pixel array into pixel blocks (32x32 pixel blocks for the 2D-IC architecture while 8x8 pixel blocks for the 3D-IC architecture), each having its own self adjusted integration time. The respective integration times are evaluated from one image to the next as follows. The pixels are fed with specific reset signals (for the 3T case, used in this work) or with specific transfer signals (4T case). According to the ADC outputs, the integration time of a pixel block is computed in the EXP block and represented by a 4 bit word. Then these 4 bits are sent to the corresponding Reset Element (rexel) that generates a reset signal RST_Tint specific to each block. Finally the pixel receives the RST_HDR signal that corresponds to the previously evaluated integration time. This process does not modify the frame rate or the pixel architecture of the primary image sensor. Hence, the pixel value is coded as a floating point number: the mantissas (MANT) are readout from the ADCs and the exponents (EXP) are readout from rexels.
Figure 2, the pixel block is composed of 32x32 pixels. As the imager acquisition mode is the rolling shutter mode, all pixel rows have the same integration time within their block but different input signals, row to row time shifted. This shift is already generated for the “primary” signals that are common to each row of the whole matrix, i.e. Row Select (RS) and Reset (RST). This delay also has to be implemented for signals that are specific to each pixel block: RST_Tint, coming from the corresponding rexel, represents

the additional reset portion needed to generate RST_HDR1. This RST_Tint is then delayed in order to generate RST_HDR2 and so on until the last pixel row of the block. Thus additional circuitry per pixel block is needed in order to perform the time shifting of RST_Tint. The interest of a 3D-IC version lies in implementing this additional circuitry on the second layer. To be compliant with the 3D architecture, a minimum of two dead pixels (i.e. not sensitive to light) per pixel row are required in the 2D proof of concept architecture. They are layout in a diagonal way so as to embed two switches and a dynamic shift register whose clock, named RST_CK, is common to the whole matrix.

As shown in Figure 3, each pixel block is associated with its own rexel, whose goal is to generate the signal RST_Tint corresponding to the 4bit signal EXP. A 4 bit SRAM first stores the EXP value. Then a 4 bit down-counter is loaded with the EXP value. This value is decremented at each rising edge of the signal CK_LOG. When the down counter output equals zero, then the rising edge of RST_CK causes RST_Tint to fall, meaning the pixel starts integrating. As illustrated on Figure 3, two successive time interval between 3 consecutive rising edges of CK_LOG are in ratio of 2, so as to obtain eleven possible integration time values proportional to $\{1/2^0,1/2^1,\ldots,1/2^{EXP},\ldots,1/2^{10}\}$. An example of an integration time of $Tframe/2^2$ is given on figure 3. Due to the rolling shutter mode, one CK_LOG is generated and undergoes a 32 pixel row shift from one rexel row to the next. The use of 11 different integration times ranging from 20µs to 20.5ms in a single frame extends the DR by +60dB.

From a PSNR criterion, the optimal integration time per pixel block is obtained when the maximum value among the 32x32 pixels equals the highest code before saturation, i.e. above the mid code 512 and less than the saturation code 1023. Figure 4 shows the algorithm used for the determination of the pixel block integration time. First, the pixel block maximum is retrieved while, in parallel, previous exponents are transferred from the related rexel row to the EXP blocks. Secondly, if saturation is reached, the next integration time will be the shortest one corresponding to EXP=10. If not saturating, a counter gives the number K of consecutives MSBs whose values equal zero. K indicates that the new integration time can be doubled K times. This is equivalent to subtracting K from the previous EXP in order to obtain the updated EXP. The process completes with the return of updated EXPs to their corresponding rexels. As this algorithm runs during row selection time, frequencies at stake are low, allowing serial processing, which saves silicon area.

An 800x512 image sensor with 5µm pixel pitch has been fabricated using a 0.18µm 1P4M process. The image sensor can be operated in the conventional LDR mode or the HDR mode that extends the DR by +60dB. Three images of the same scene (whose DR exceeds 120dB) are given in Figure 5, the first one in the conventional LDR mode, the second one in the HDR mode and the third one after a basic FPN blind reconstruction algorithm. On this second image are superimposed the exponents of the pixel blocks. These exponents, as expected, span from 0 to 10 in order to avoid saturation inside a pixel block. On the third image, block artifacts appear but will be removed after a more sophisticated image processing. Table 1 compares our circuit to the state of the art and stresses the preserving in the pixel architecture and in the readout timing. Hence, our DR extension technique can add the HDR feature to any imager without mitigating any other performance. For example, it can be used for a global shutter imager or a low noise imager to better fit the needs of very demanding applications. The chip micrograph of Figure 6 shows that, with respect to the pixel array, the additional circuitry represents only 6% for the rexels and 3% for the EXP blocks. Once implemented using a 0.18µm 3D-IC technology and a BSI imager, this architecture will easily accept pixel blocks of 8x8 pixels without the inconvenience of dead pixels inside the matrix. A more advanced technology node for the 2^{nd} layer of a 3D-IC imager would reduce even more the block size.

References

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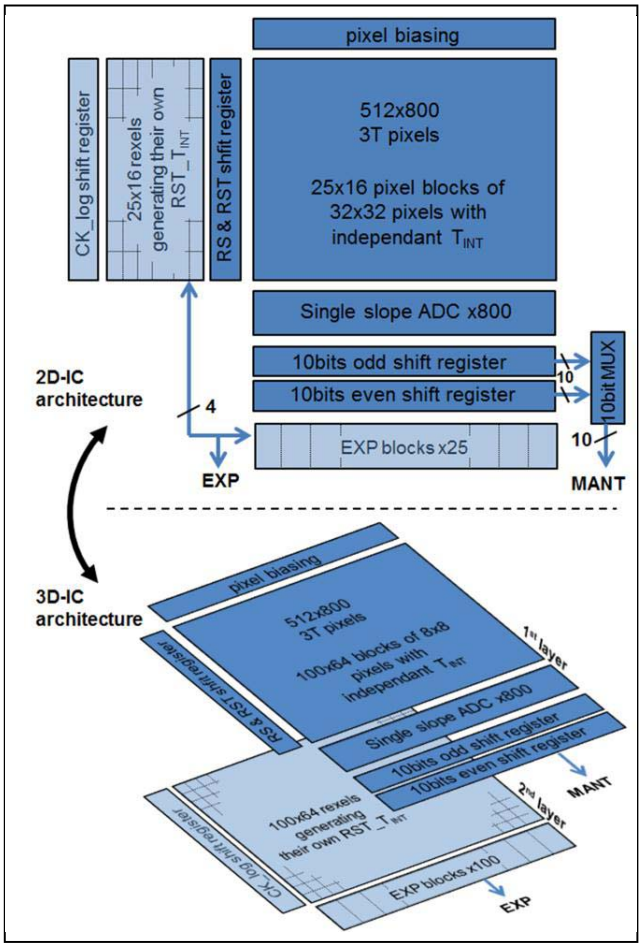

Fig. 1 Overall block diagram of the chip for 2 different architectures (the 2D one has been fabricated and the 3D one has just been studied). The dark blue blocks, further referred to as "primary" image sensor blocks, are common to both architectures and could be part of any image sensor. The light blue blocks are added to provide the HDR feature to this primary image sensor

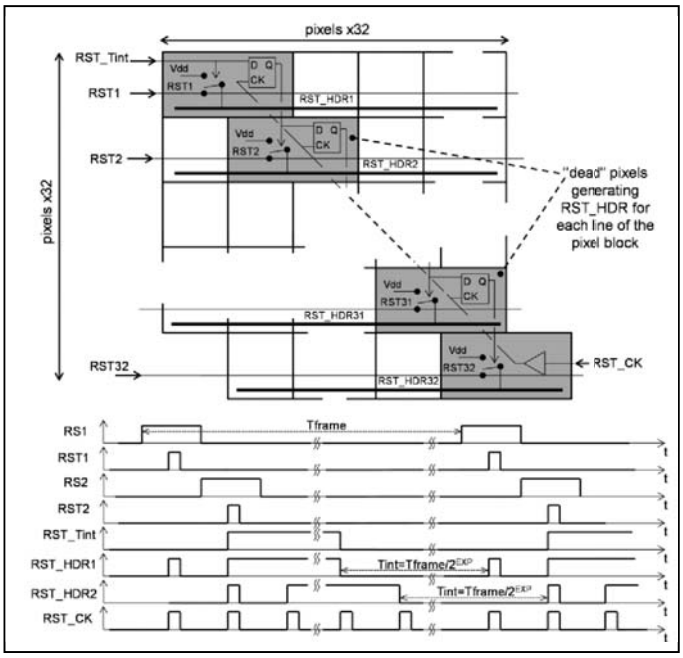

Fig. 2 Block diagram of the "pixel block" and associated timing diagrams

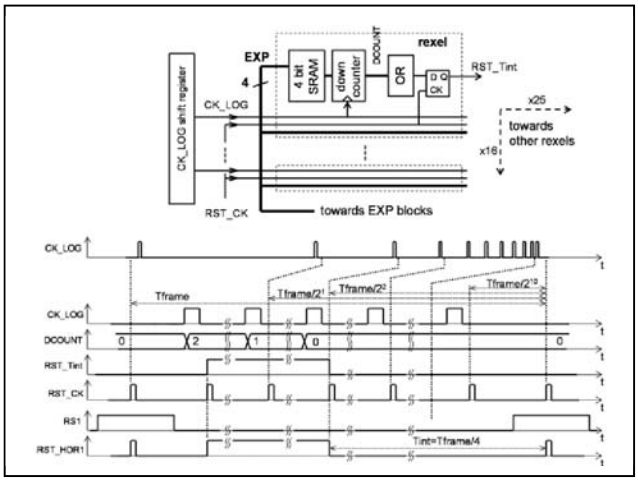

Fig. 3 Block diagram of the "rexel" and associated timing diagrams

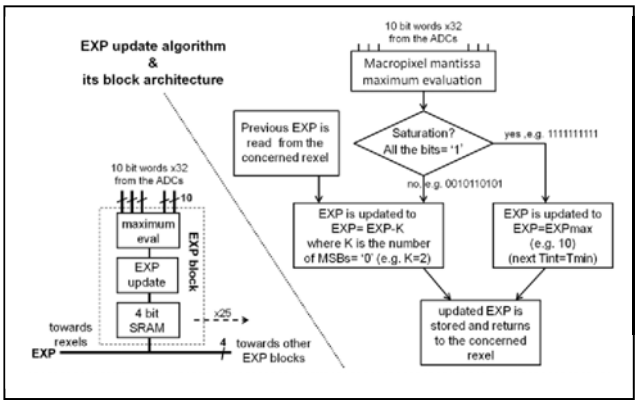

Fig. 4 block diagram of the "EXP block" and its associated algorithm

	This work	[4]	[3]	[2]	[5]
Technology node	0.18µm	?	0.35µm	0.18µm	?
Pixel size (µmxµm)	5x5	3.75x3.75	7.5x7.5	14x14	7.5x7.5
HDR technique	Local Tint adaptation	Triple exposure	LOFIC	Time to saturation	Dual diodes Dual shutters
Total DR	120dB	106dB	100dB	132dB	92dB
HDR granularity	32x32 pixels	1 pixel	1 pixel	1 pixel	1 pixel
Pixel modification due to DR extension	No, 3T pixel (and can work with 4T pixel)	No, 4T pixel	Yes, 4T pixel + additionnal capacitance	Yes, digital pixel	Yes, 5T pixel +3 additionnal transistors
Readout modification due to DR extension	no	3x faster	2x faster	Digital readout	2x faster

Table 1 Comparative table with other HDR sensors

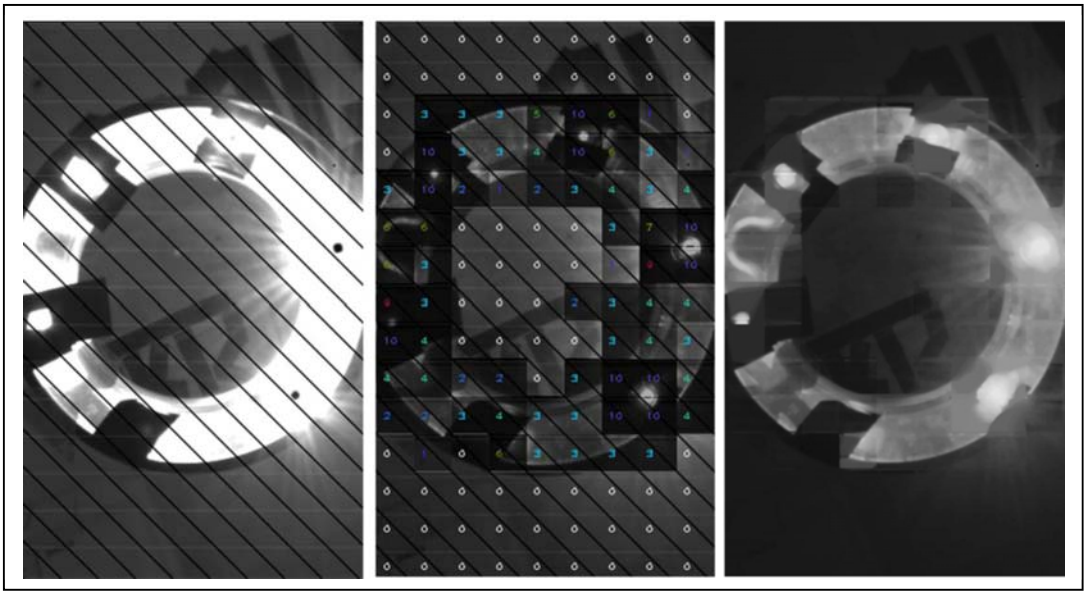

Fig. 5 Three cropped-images of the same scene (an LED lamp). On the left, the image of the mantissas is taken without activating the HDR mode (all blocks have the same EXP or the same integration time). In the middle, the image of the mantissas is taken with activating the HDR mode (each block has its own EXP that is superimposed to the image for understanding purposes). On the right, the reconstructed HDR image.

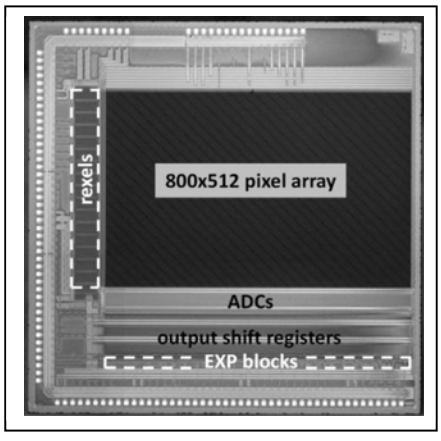

Fig. 6 Fabricated chip using a 0.18µm CMOS process