A 1 Megapixel HDR Image Sensor SoC with Highly Parallel Mixed-Signal Processing

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***Abstract*—This work aims to develop a universal and flexibly programmable image sensor SoC for a variety of industrial image acquisition and processing applications. It is comprised of an array of 1024×1024 pixel cells with a pitch of 8.75 µm and features linear/logarithmic characteristics. In logarithmic mode, dynamic range exceeds 120 dB. The fully programmable, column-parallel, mixed-signal data path from charge-based pixel readout and analogue processing via multi-slope analogue-to-digital conversion to the full custom digital 8-bit ALU allows for data processing with more than 100 GOps.**

***Index Terms*—image sensor, vision-system-on-chip, VSoC, dynamic range, linear-logarithmic response, ASIP**

I. Introduction

Since the early CMOS image sensor designs, several efforts have been made to perform image processing and feature extraction as close as possible to the photo detector, and to achieve high processing speeds by exploiting the potentials of massive parallelism. In [1], an overview of different approaches to vision-system-on-chip (VSoC) is presented. It is noticeable that only a few sensors are manufactured in large quantities and thus exhibit high user acceptance. Notable examples are the sensors in computer mice [2] or dedicated sensors for laser light section systems [3].

For the most part, this is because of low fill factors and hence low sensitivity, their resolution being much lower than conventional image sensor's, and usually a complex external control or programming. Undeniably, in general very high processing speeds and the resulting data reduction to overcome the bottleneck of the external interface, speak in favor of these sensors.

The presented VSoC shall combine the advantages of programmable processing complex image algorithms at high speed with a high fill factor. Moreover, dynamic range is significantly increased using a lin-log transfer characteristic. Combining these features, the vision-system-on-chip can be used for a variety of applications and can be tailored to new applications using software.

II. Pixel cell design

In Figure 1, the fundamental circuit diagram of the pixel cell is depicted. It contains a photo FET T_{Ph} as photodetector [4] and a current memory (SI) cell for information storage. In [5], the pixel cell and the concept of charge-based signal processing and analog/digital conversion were presented for the first time.

The operating point of the pixel cell and thus noise, dynamic range, and power consumption of the sensor matrix can be set by the drain current of T_{Ph}. Values can be digitally set in 31 discrete steps between 65 nA and 2 µA via the integrated bias circuit.

The drain current of T_{Ph}, the value stored in the SI-cell, or the difference of both, is switched by S_{O} to generate current pulses and hence charges at the `IO` terminal. The generated charge is controlled digitally and proportional to the width and number of pulses. Via S_{Res}, the internal node N_{i} can be set to a predefined potential according to the reset potential of the column line. To reset the photo FET to a defined value at the beginning of the integration of photocurrent, the symbolically depicted S_{SetC} is used. D_{SB}, the source-bulk diode of T_{Ph}, is responsible for its logarithmic saturation.

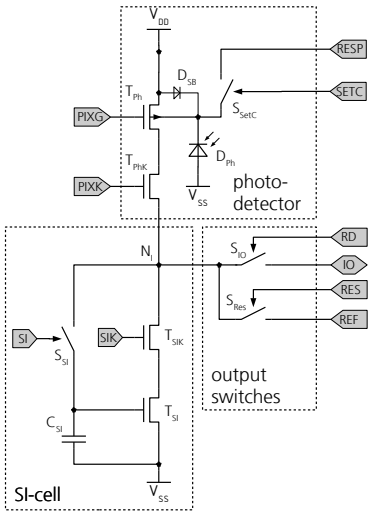

Figure 1. Principle circuit diagram of the pixel cell

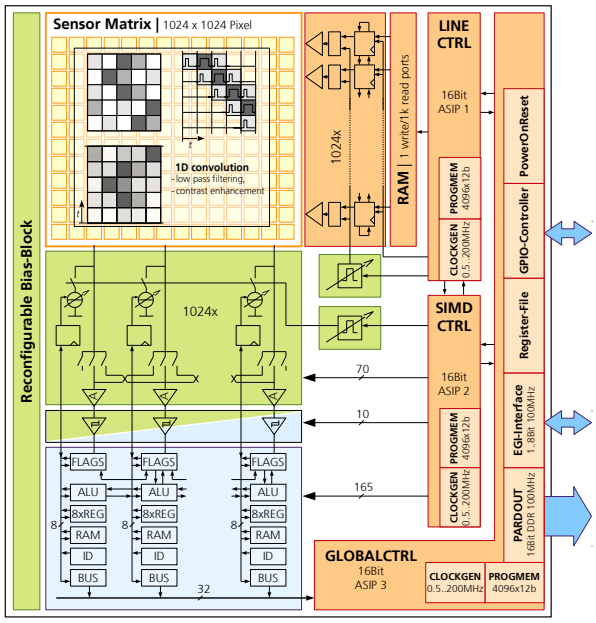

Figure 2. Architecture of the vision system-on-chip.

III. Sensor Design

The architecture of the VSoC is depicted in Figure 2. The focal plane is controlled by the application-specific instruction-set processor ASIP 1 (`Line Ctrl`), in combination with the shift-register unit activating and setting the length of the current pulses. Thus, for example, 1-D convolutions of digital coefficients with the analogue image data of the pixels are possible. All the other pixel operations, such as `RESET`, `EXPOSURE`, `MEM` are controlled in the same way.

The charges are handled column-wise by 1024 mixed-signal processor elements (PE), controlled by ASIP 2 (`SIMD Control`). In the analogue first-stage amplification, storage, inversion and replacement of the charges with the two neighbouring columns can be carried out. Images are digitally converted using charge compensation by current pulses of opposite sign, and comparison of the resulting voltage with an adjustable global reference. The conversion algorithms are implemented in software, controlled by the PE program execution, so that the realization of different slope- as well as SAR-algorithms become possible. By changing the number and size of conversion steps as well as the rate of charge output and comparison operations, it is possible to optimize parameters such as accuracy, resolution and sample rate. The pulse width for the compensation pulses may be chosen in 64 discrete steps between 2 ns and 2 µs. The ADC's comparison operation is the interface to the digital domain, and one of 55 8-bit SIMD instructions implemented in the PE. Other examples are arithmetic (`ADD, SUB`), logical (`NOT, AND, OR, XOR`) and bit operations (`SHL, SHR, ROL, ROR`). In addition to the ALU-register, each PE has seven internal registers for command execution. Moreover, there are sixteen registers used for data storage. Each column has its own ID, which can be used in combination with a look-up table for algorithmic purposes, e.g. the search for the first occurrence of an event in any PE starting from right or left. For each flag in the flag registers of all columns a global logical combination may be determined.

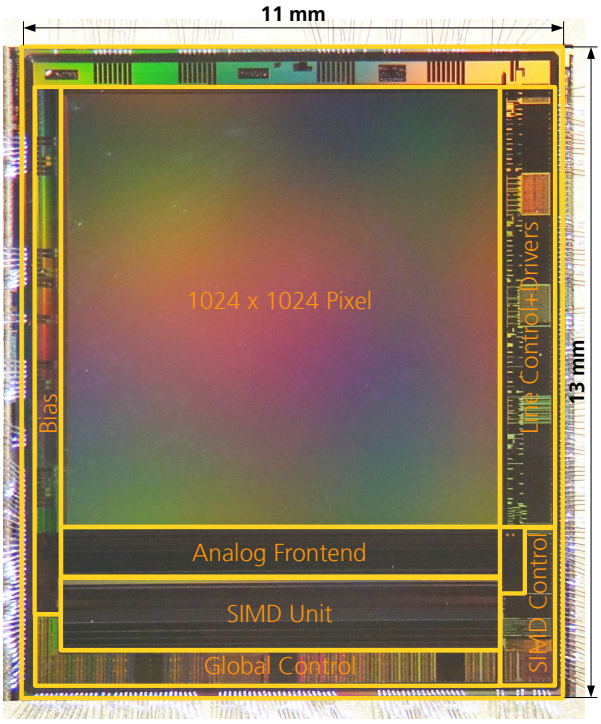

Figure 3. Picture of the vision systen on chip.

Data exchange with the PEs is controlled by ASIP 3 (`Global Control`) and is carried out via a 32-bit data bus, accessible via 16-bit registers in the even and odd columns. The combination of all outputs on the data bus is carried out by a wired-OR. There are three possibilities for data input and output of the SoC: a fast parallel 16-bit DDR-interface running at 100 MHz (`PARDOUT`); a configurable SPI-like interface with 1, 2, 4 or 8 lanes (`EGI`); and a 16-bit `GPIO`, which can be split signal by signal between the three ASIPs. Each of them is clocked individually using a programmable oscillator with frequency range between 500 kHz and 100 MHz. Figure 3 shows a photograph of the chip manufactured in a standard 180nm 1P6M-CMOS technology.

IV. Experimental Results

During measurements, the entire VSoC has been operated at 1.8 V and a medium operating point for the pixel cells was chosen. For this purpose, they were set to a bias current of 1 µA and to VDD for the reset voltage of D_{Ph}. Analogue-to-digital conversion has been performed by appropriately settings the size for one

LSB to resolve the whole dynamic range with 8 Bit. Two increments of the compensation charges, 1 LSB and 4 LSB, have been chosen, resulting in a conversion rate of 200 kHz at a basic clock frequency of 100 MHz.

To estimate the linear-logarithmic transfer function, measurements with irradiation intensities over more than four decades have been performed. The results are depicted in Figure 4. In order to better understand their relationship, the digital value has been plotted depending on the number of impinging photons according to the equation

$$N_{\mathrm{Ph}} = \frac{A_{\mathrm{Pix}}\, E_{\mathrm{e}}\, T_{\mathrm{exp}}\, \lambda}{h\, c} \qquad (1)$$

with the pixel area A_{Pix}, the irradiance E_{e}, the exposure time T_{exp}, the wavelength λ, Planck's constant h and the speed of light c.

In the linear region, all curves are almost exactly superimposed. With increasing irradiance, logarithmic mode starts at higher digital levels and higher number of photons which results in a dependence of an equivalent full-well capacitance from impinging light. The logarithmic operation's lower threshold is determined by the dark current (dashed line). Due to its influence, the linear region exhibits higher gains at very small irradiance values (E_{e}= 100 nW/cm²).

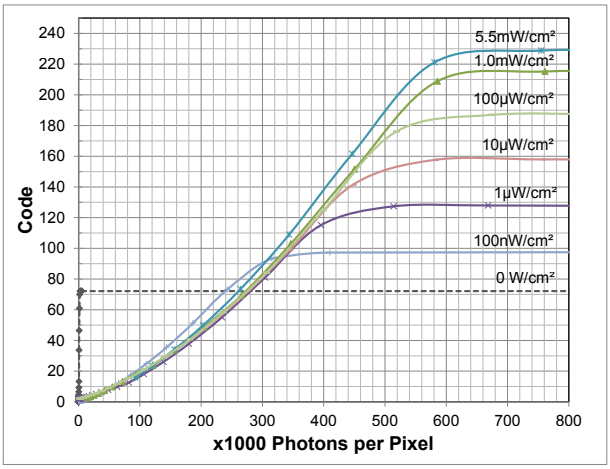

Figure 4. Linear-logarithmic characteristics at different illumination levels.

Figure 5 shows the transfer function in the logarithmic operation at $\lambda = 527\,\mathrm{nm}$ with a marker for the sensitivity of 40 nW/cm² and a dynamic range of 120 dB. Further measurements have been performed, but no deviation from the logarithmic behavior was observed.

Figure 6 depicts a family of curves with the digital value depending on the irradiance at different integration times. This graph can be used to optimize the sensor control for the operation in linear and logarithmic mode through the choice of an appropriate combination of shutter speed and irradiance level. It is possible to determine

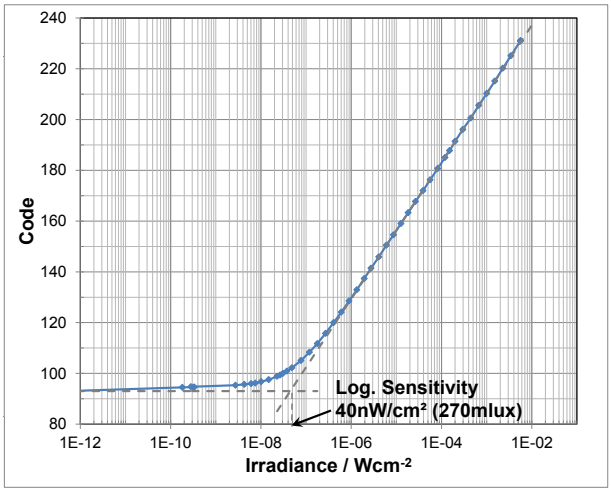

Figure 5. Logarithmic response.

1) the settling time for the logarithmic operation depending on the irradiance level (Example: 100 ms @10 µW/cm²),
2) the required irradiance level for logarithmic operation at a given frame rate (Example: 100 µW/cm² @ 100 fps), or
3) the lowest limit of the irradiance in linear mode for a given integration time (Example: 100 nW/cm² @ 100 ms.

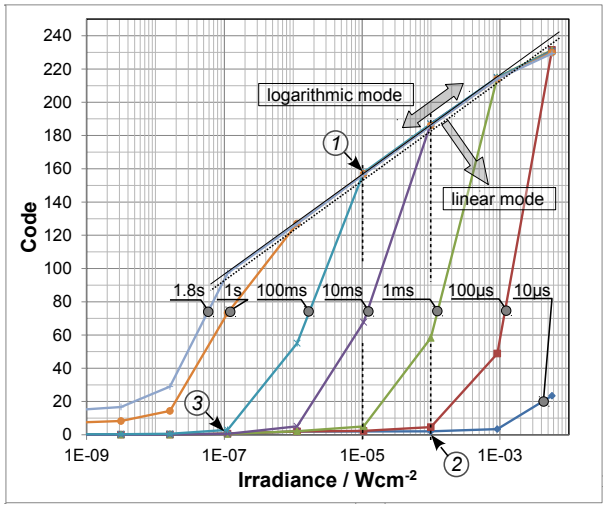

Figure 6. Family of curves for the optimization of lin/log operation.

Figure 7 shows the image of a natural scene with high dynamic range captured by the VSoC.

V. Conclusion

A vision-system-on-chip with linear-logarithmic pixel cells, column-parallel charge-based mixed-domain signal processing and the possibility to freely program image processing and output mechanisms has been

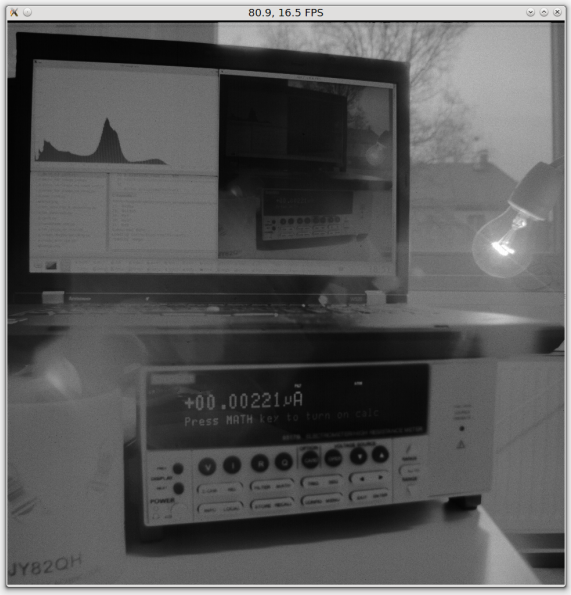

Figure 7. Linear-logarithmic image taken by the image-sensor SoC

Table I
SPECIFICATION OF THE VISION SYSTEM-ON-CHIP.

Sensor matrix	Resolution	1024×1024 Pixel
	Pixel size	8.75 µm×8.75 µm
	Fill factor	50 %
	FPN (uncorrected)	<1.3 %
	Equivalent full well capacity	43 ke (no light) .. >100 ke (5mW/cm²)
	Dynamic range	>120 dB
	Log sensitivity	40 nW/cm² (0.27 lux)
	Dark current	6200 e/s
	Log SNR	49.9 dB
ADC and control	Exposure time	1 µs .. 20 s
	Greyscale resolution	1 .. 12 Bit
	SNR	57.8 dB @200 kHz
Processing	Clock frequency	500 kHz .. 100 MHz
	ASIP memory	3 × 4 k words
	SIMD instructions	55 (8-bit ALU)
	SIMD memory	1024 × 24 × 8 Bit
	GPIO	8 + 8
	Dout	16 @ 100 MHz DDR
VSoC	Technology	180 nm, 1P6M CMOS
	Analog supply	1.8 V
	Digital supply	1.8 V
	Analog power	67 mW @ 15 fps
	Digital power	133 mW @ 15fps

developed. It has been characterized, and has a dynamic range of 120 dB and a sensitivity of 40 nW/cm² For analogue-to-digital conversion, a method with compensation charges of various sizes has been implemented in software for the ASIPs and SIMD unit. It exhibits an SNR of 57.8 dB in the medium at a conversion rate of 200 kHz. Currently software for high-speed laser light section measurement, and for texture-based optical presence-detection are being ported to the VSoC.

ACKNOWLEDGMENT

The authors gratefully acknowledge the ENLIGHT project (http://www.enlight-project.eu/), funded by ENIAC and the German Federal Ministry of Education and Research, for the financial support.

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