A High Speed 1 MPix Sensor with Floating Storage Gate Pixel

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A new generation of global shutter pixels targets low noise and thus incorporates in-pixel correlated double sampling (CDS) [1-3]. In the last workshop we reported the idea how to build a CDS in-pixel using a single-Poly charge-transfer device in the pixel and the floating gate readout [4]. Based on this concept, we developed a 1 Mpix (1280x864) high speed CMOS sensor for a 3D scanning application.

1. *Pixel with Floating Storage Gate*

The pixel (Fig.1.) has a pinned photodiode PPD, an anti-blooming/shutter gate AB, a transfer gate TX, a storage gate SG, the second transfer gate TX2, a reset gate RST and the source follower SF with ROW enable. The storage gate is connected to the reset switch and to the source follower.

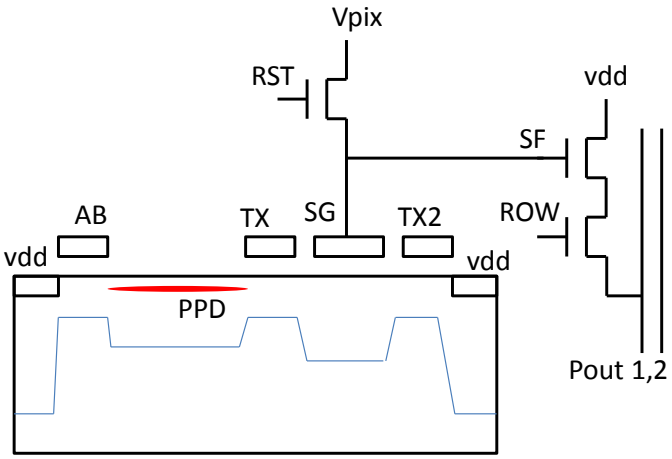

Fig.1. Global shutter pixel with CDS on a floating storage gate.

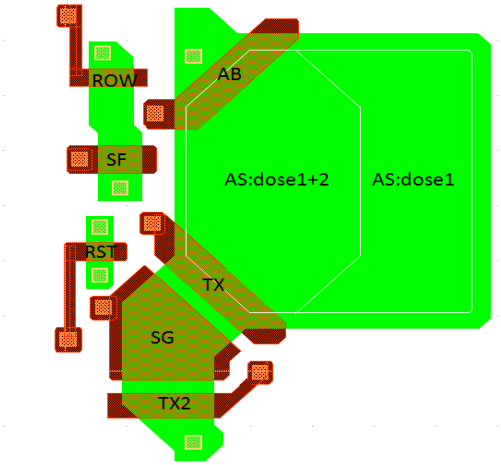

Fig.2. Layout of the pixel.

During the global transfer, charge from photodiode flows to under the storage gate held at Vpix voltage. The readout of the charges is row-by row. To read out the signal corresponding to the accumulated charge, the RST switch is made open, and the first sample of the voltage on the floating gate (with charge) is read out from the pixel. Then the TX2 gate is pulsed High opening the path for the charge into VDD. After charge is removed, the second sample of the voltage at the floating gate (w/o charge) is read out thorough source follower.

The most interesting feature of the floating gate readout is a combination of ***High storage capacity and low readout capacitance.***

The high storage capacity is due to the fact that the charge is stored in the Thin-Oxide Gate-Channel capacitance of the storage gate, with Depletion layer capacitance added in parallel. The small readout capacitance is due to the charge conservation at the floating storage gate. When the mobile charge leaves the storage and goes to VDD, the mirror charge remaining at the gate ionizes the acceptor in the depletion layer under the gate to terminate its electric field line. The depletion layer capacitance is small, so the readout capacitance.

In practice, there is always a parasitic capacitance of RST, SF gates and the metal interconnect added to the readout capacitance, but in a good design, the feature of high storage capacity and low readout capacitance could be preserved.

2. *Column Amp, Column ADC, Digital readout*

The pixel signal is read through the column amplifier into the column ADC. These blocks were described earlier [5] and did not undergo many changes other than fitting the circuits into the given pitch.

To speed-up the readout, there are two vertical readout lines crossing every pixel [6], so the pixel array is read out in pairs of lines (bi-lines). So, there must be 2 ADCs per pixel pitch to read out from 2 rows of pixels simultaneously.

A column AMP before ADC was used to enhance the sensitivity and possibly reach lower readout noise.

The column ADC is of our standard Successive Approximation type, with multi-stage auto-zero comparator, for column FPN reduction [7].

One bi-line of data is stored in the digital memory, serialized and read out.

3. *Fabrication and Measurement Results.*

The sensor was designed and manufactured in UMC 0.18um CMOS sensor process using our custom pixel masks and implants. Pixel pitch was large 13.68um to ensure high sensitivity and to match the pitch of the predecessor. The single Poly charge transfer structure TX-SG-TX2 was made with the gap between Poly gates of 0.24um. The gap was implanted with a low dose of Arsenic to suppress the barrier between the gates. The storage gate has an option to be with a buried channel, this is our default process recipe now. Some details on the process could be found in our pixel paper[4]. Wafers are cut and assembled into either 352-pin uPGA or 344-pin uPGA package. The picture of the assembled sensor is in Fig.5.

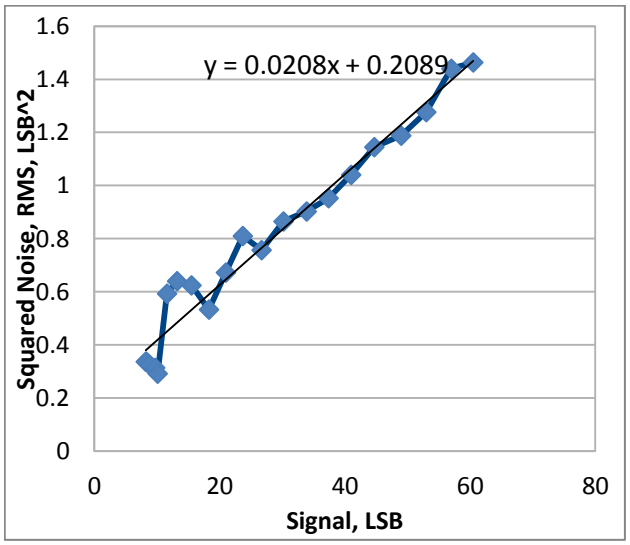

Fig.3. Conversion gain measurements. Gain=1.

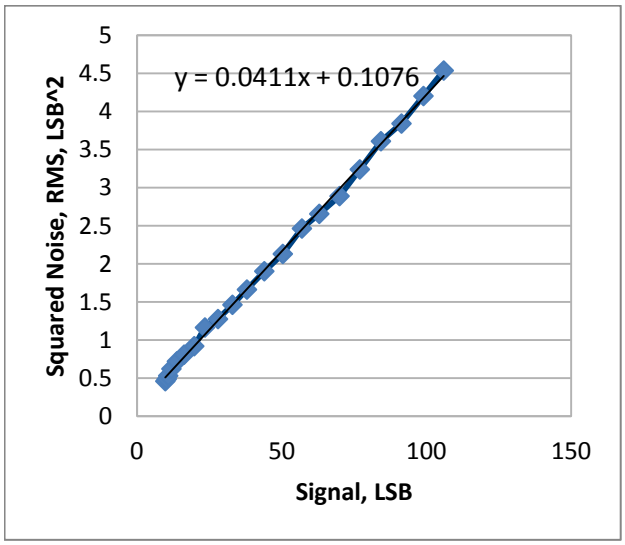

Fig.4. Conversion gain Measurements. Gain=2.

The testing of the sensor was done using a custom camera. Fig.3-4 presents the results of the conversion gain measurements. The test system was limited to 8-b accuracy and the coarse quantization caused an oscillation in the temporal noise measured with the unity gain of the column AMP. The results

were repeated with the Gain=2 to confirm the conversion gain of the pixel to be 75 uV/e-. The noise in dark was a function of the amplifier gain (Fig.6).

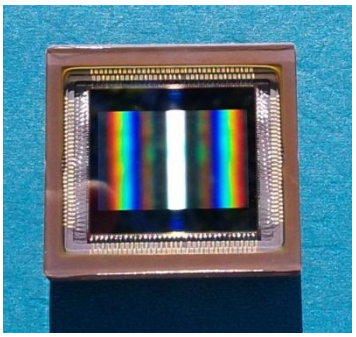

Fig.5. Photograph of the sensor

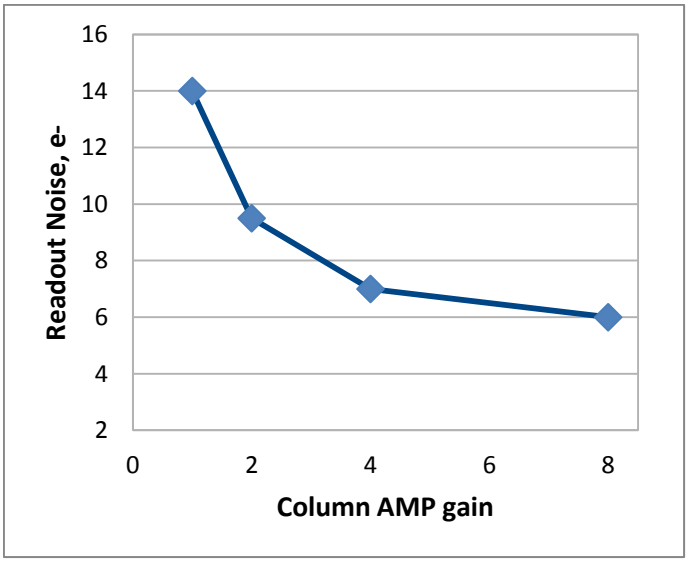

Fig.6. Dark Noise versus column AMP gain.

Pixel-referred RMS of the temporal noise varied in these experiments from 450uV to 1.05mV. The theoretical limit for an ideal column circuit with the storage of ~ 1pf should be of the order of 100uV RMS [8]. We have not identified yet the sources of the extra noise. Based on the observed reduction with the gain, the dominant source must be post-column amplifier. In any case, the noise of 6-14e- for the sensor operating at 3000 Frames/s is a good result, in our opinion.

Temporal noise vs Settling. In our first batch of the sensor, an insufficient time was allocated to the sampling of the reset value from the pixel. The indication of this was a frequency-dependent positive offset added to the signal (+80 mV at 3000 Fps, compared to 1500 Fps). We thought, insufficient settling might affect the accuracy of the CDS, so expected the noise would go down in the second revision of the sensor. The new revision is out, the black level control is good, however the noise reduction is not observed. We observed however the noise increased by ~50% when the sensor clock was raised by 60% above the nominal value. The explanation is the increased DNL of the ADC causing irregular quantization.

Fixed pattern noise in dark over entire frame was 2.5mV rms. The dominant component was the pixel FPN. The first revision of the sensor also has high odd-even row nonuniformity. The vertical readout lines had a different coupling to the pixel readout nodes. By Metal routing redesign and a shielding, this component was reduced from 6 lsb p-p to 1 lsb p-p.

Dark current might be an issue for this type of the pixel, when the sensor operates at low frequency. The average dark current signal of 120 mV/s at 55C was estimated from the DSNU histogram broadening with varying frame rate from 3000 to 300 and to 30 frames/s. No white spots were observed at 3000 Fps, while a single white spot at 300 Fps and a dozen of white spots at 30 Fps. The source of the dark current is the channel under the storage gate. If a low frame rate operation is needed, the easy fix is to employ a burst readout shortly after the global TX transfer preceded with a global TX2 clear of the storages right before the global transfer. There is also a more elegant fix is to problem which is to employ the CCD annealing techniques to passivate the surface states under the gate.

Other measured parameters are summarized in the following table:

Active resolution	1280 x 864 pixels
Pixel	13.7 um pitch 7T shutter pixel with CDS
Full well/ Read Noise	16,000e-/ 14e-
Responsivity	25V/Lux-s @ 550nm
Image Lag	Not detected
Conversion gain	75 uV/e-
DSNU	2.5 mV rms
PRNU	<1.5% rms
Shutter efficiency	99.8%
Frame Rate	>3500 Frames/s @ 1280 x 864
Column Parallel ADC	10b
Data Output	80 LVDS ports @540MHz for 10-b output
Nominal clock rate	133 MHz
Power supply	3.3V Analog, 1.8V digital
Power consumption	2.5W @ 3000Fps full resolution
Package	352-pin uPGA, 36mm; 344-pin uPGA, 30mm

Concluding remarks:

We have proved we can make a practically usable CMOS device out of the concepts popular in early CCDs. A single-Poly charge transfer device is made in 0.18um process with the help of a Gap implant. The 7T pixel has some size limitations, but many high speed applications do not need small pixel. The CMOS sensor process used could not offer dark current of CCDs, but this was not an issue for the high speed application. Also, it is possible to add a Hydrogen annealing to the recipe.

The floating gate amplifier did not find wide usage in CCDs because of a low conversion gain compared to the floating diffusion readout which had become dominant [9]. Yes, we can agree we could not have the record high c.g. in this sensor, but the achieved one is quite acceptable.

We did not fully realize the advantage of the high storage capacity. Moreover, we had to forcefully cut (!) the accumulated charge with opening the anti-blooming path through TX2 gate in order to achieve the full charge transfer. We hope we will find the use of this feature in the future sensors.

References:

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