A Flexible 14-bit Column-Parallel ADC Concept for Application in Wafer-Scale X-ray CMOS Imagers

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Abstract
The use of a column-parallel ADC concept in wafer-scale X-ray CMOS imagers is attractive for reasons of costs and performance. In order to serve an extensive range of imager products, it is mandatory for the ADC architecture to be highly flexible. In this paper we present a 14-bit ADC implementation in a 0.35µm 2P4M CMOS process that meets this requirement. Adaptations of and additions to the basic ADC concept required for application in various X-ray imager variants are described as well.

1. Basic ADC operation

The operating principle of the applied ADC is based on a multi-slope thermometer code search methodology. This architecture was preferred to single-slope, successive approximation or cyclic implementations for reasons of size, speed and power consumption.

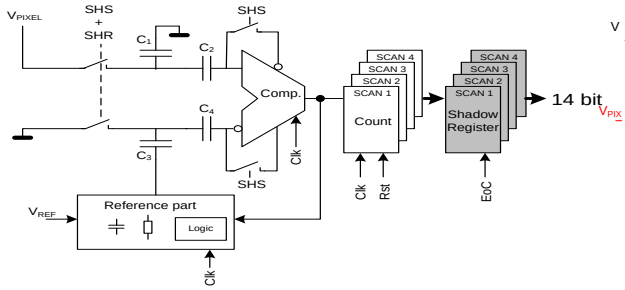

Figure 1 *Basic 14-bit ADC architecture*

The related block diagram is depicted in Figure 1 and consists of the following blocks: a sample and hold circuit, a reference part with a multi tap resistor ladder, a bank of poly-poly capacitors and switches, an offset-compensated low-noise comparator, counters and registers to temporarily store the output data. The first step being the pixel readout and related timing is given in Figure 2.

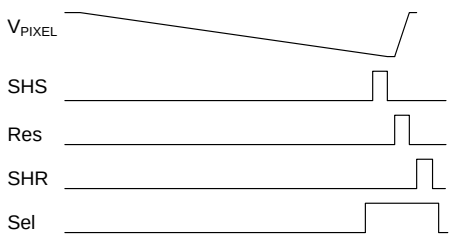

Figure 2 *DDS (Double Delta Sampling) pixel readout timing*

Following pixel reset, the charge integration phase starts and the output of the pixel (V_{PIXEL}) decreases gradually as a result of photon induced electrons. At the end of the integration phase, the column select (Sel) is activated, V_{PIXEL} is sampled and stored under control of the SHS timing signal on capacitors C1 and C2. To compensate for comparator offset the input offset is stored on C2 simultaneously. Immediately after readout of the signal, the pixel is reset once more and consequently this value is sampled under control of the SHR timing signal. Since the signal level of the pixel and comparator offset are already stored on C2, the result of the second sampling action is the subtraction of the pixel signal level and offset from the reset level. To finish the pixel sampling the column is deselected.

For the A-to-D conversion process the reference part generates 4 ramps with accurate reference levels during 4 subsequent scans. From ramp to ramp the step size is decreasing as depicted in Figure 3.

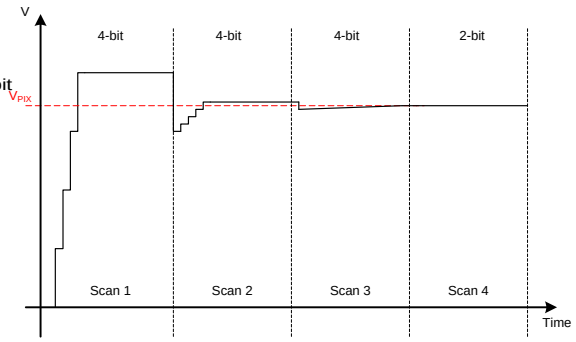

Figure 3 *ADC conversion process*

For this purpose the reference part consists of a bank consisting of 16 x 16 unit poly-poly capacitors and a resistor divider with 16 + 3 taps. The 4 different ramps are then generated by means of the following combinations:
- Ramp 1: groups of 16 unit capacitors with Vref
- Ramp 2: one group of unit capacitors with one of the 16 taps of the divider giving Vref/16 steps
- Ramp 3: unit capacitor and again one of the 16 taps of the divider
- Ramp 4: unit capacitor and the three additional taps between reference ground and the first of the 16 taps giving steps of Vref/64.

The first 4 most significant bits are determined during the first scan and therefore the sampled pixel level is compared with the ramp by use of the low-noise comparator. If the ramp exceeds the stored pixel level, the reference output is decreased by a value equal to the last step. Subsequently, a

next scan with smaller steps is performed to derive the next 4 bits. The conversion is finalized when three scans for 4 bits and one scan (the last) for the 2 least significant bits have been completed. The total 14-bit conversion lasts 5.2µs. Every step corresponds to a count related to the bits weight of the respective scan. The 4+4+4+2 output bits of a single ADC are combined for all the columns in a serial fashion, line and frame sync pulses are added and brought off-chip by means of an LVDS serial interface.

2. Binning implementation

Vertical binning is implemented by averaging the pixel output of two adjacent rows. Since the conversion process for two rows has to be performed simultaneously to increase frame rate, the ADC needs a dual instead of a single input. To realize this dual input the sample and hold part of the basic single input ADC is extended as shown in Figure 4.

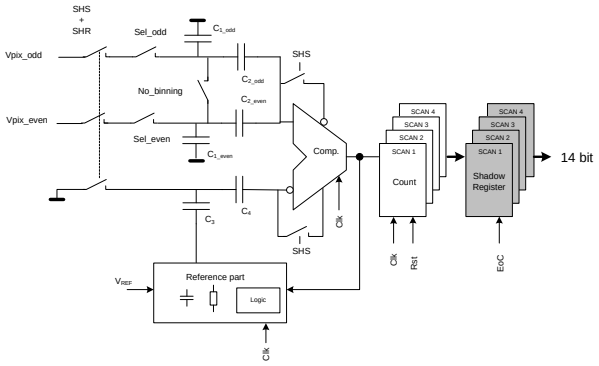

Figure 4 *ADC extensions to enable row binning*

For normal operation the 'No_binning' switch is closed. As a result the capacitors C_{1_odd} is connected in parallel to C_{1_even} and likewise C_{2_odd} and C_{2_even}. Alternately the 'Sel_odd' and 'Sel_even' switches are closed to sample the pixel levels of the odd and the even rows respectively.
For binning operation the 'No_binning' switch is opened and both select switches are closed at the same time. The net result is the intended averaging of both pixel levels. Readout of the pixel array is implemented according Figure 5; one input of a dual input ADC is connected to the even rows and the other to the odd rows.

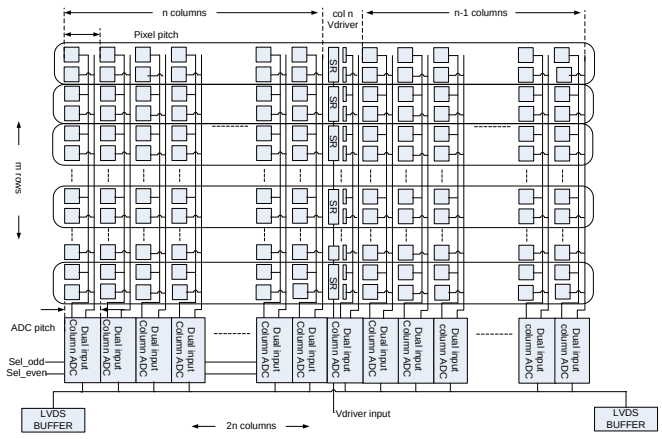

Figure 5 *Row and column arrangement in case of binning*

The rows are readout in pairs under control of the V- (row) driver located in the center column of the pixel array. Both select signals control not only the ADC input switches but also the switches to simultaneously connect the pixel output of two rows to their respective column busses.

In case sensor tiles are vertically butted with a butting distance of one pixel pitch, geometrical image distortion might occur if pair-wise readout for both tiles is done in an identical manner. Assume for instance the gap is ignored, distortion as a result of vertical compression occurs while if the gap is treated as a row pair, the single pitched gap is expanded to a double pitch distance in the resulting image. By implementing a single row shift and activation hereof for one of both sensors solves this issue. The principle is drawn in Figure 6.

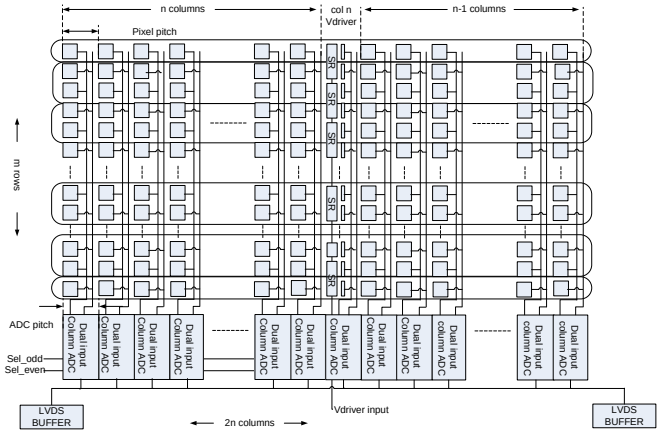

Figure 6 *Row pairs in case of shifted binning*

For one of the tiles (either the top or the bottom one) the row pairs are shifted one row in vertical direction. This results in a single top and bottom row. For these both only one select line is activated, one ADC input is used and hence the pixel output is not averaged. For the top row this implies the output of one row is used for the combination of an active row and the (non-active) gap and distortion as a result of geometrical compression or expansion is avoided.

3. Adaptations to various column widths

The width of a single column ADC is approx 67µm. In case the pixel pitch is e.g. 134µm as indicated in Table 1, two ADCs fit in one pixel pitch. The two ADCs are then both individually connected to a row and conversion of both rows is performed in parallel. In this way the frame rate can be increased considerably.

The ADC width accommodates pixel pitches of 50, 100 and 200µm in the following manner: for the smallest pixel the ADC width is extended to 100µm and a dual input is applied to serve two pixel columns. For pixel pitches of 100µm a dual input ADC is used to read out two vertically adjacent rows. For pitches of 200µm (and 134µm), two ADCs are available for a single column to increase frame rate.

4. CDS vs. DDS readout

Alternative to the DDS pixel readout method described above CDS is a solution to reduce pixel reset noise. On-chip CDS is applied to pixel architectures with a floating diffusion. Readout timing with pixel reset before signal sampling is shown in Figure 7. Compared to DDS, the order of signal and reset value sampling is reversed. The input of the comparator now decreases with decreasing pixel output signal level. The basic ADC implementation is adapted for this readout method by a simple reversal of the top and bottom connections of the resistor ladder in the reference part. Instead of a rising edge, the generated ramp is then in opposite direction (falling edge) corresponding to a decreasing signal level at the input of the comparator.

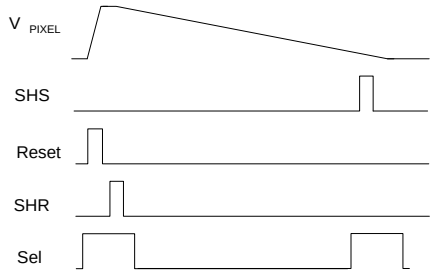

Figure 7 *CDS (Correlated Double Sampling) pixel readout timing*

External CDS for pixels without a floating diffusion is also feasible. This is accomplished by using an artificial reset reference V_{ART} instead of the pixel reset value. This (external) reference source V_{ART} and its connections are shown in Figure 8.

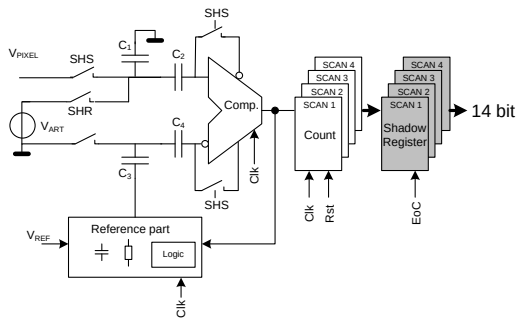

Figure 8 *Adaption for external CDS (DDS readout timing scheme)*

For one net pixel output value two conversions have to take place; the first is the pixel reset value minus this reference voltage V_{ART} and the second the pixel signal level minus the same reference voltage. The first result is temporarily stored externally and subsequently the second is digitally subtracted from the first.

5. DFT implementation

Analog and digital DFT (Design For Test) circuits are implemented for test and validation purposes. These circuits are:

- Artificial pixel
- Buffers for probing internal ADC nodes and
- Programmable generator for various digital test patterns to validate the LVDS interface.

The principle of the artificial pixel is shown in Figure 9. For normal operation the photodiodes of the pixel array are readout by connecting them through the row select switches to the column bus. The artificial pixel can be activated by first disconnecting all the photodiodes and closing the artificial pixel switch. An external voltage can then applied to the column bus. An N-most source follower is used as buffer in the same way as for the photodiode output. The artificial reset reference is used as reset level identical to external CDS operation.

Critical ADC nodes can be probed by closing the related switch and observing the buffered voltage available on the dedicated sensor pad 'Analog Test Out'. Examples of such critical nodes are: the pixel reset voltage, the column bus voltage (both to check settling behavior) and the generated voltage ramp.

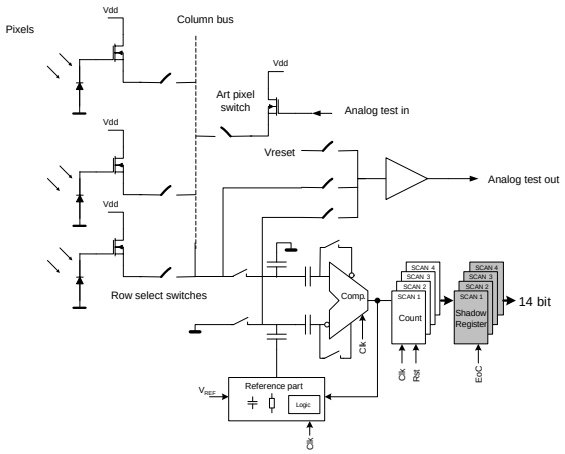

Figure 9 *Analog DFT implementation*

6. Performance summary

Table 1 summarizes the performance of a typical imager with the ADC implementation described in this paper and 134µm pixel pitch.

Technology	0.35µm 2P4M CMOS
Device Dimensions	104 x 142mm^2
Pixel Pitch	134µm x 134µm
Resolution	768 (H) x 1024 (V)
Full Well Capacity	155ke- / 567ke-
Conversion Gain	13µV/e- / 3.5µV/e-
Noise Data Double Sampling	67e- / 148e-
Dynamic Range - DDS mode - External CDS	 67.3dB / 71.7dB 77.5dB
Quantum Efficiency	> 50% @ 500nm
Dark Current @ 60 ^{0}C	60ke- / pix.sec
AD Conversion Depth	14-bit
Max. Data Rate per LVDS output	560Mbps
Frame Rate	100fps
Sensor Power Consumption	1.2W
ADC Clock Frequency	10MHz
#Clock cycles for one conversion	52
Supply Voltages	3.5V (Analog + Digital)
ADC Current Consumption	90µA (3.5V)
LVDS buffer supply	2.7V
ADC Reference Voltage	2.8V

Table1 *Performance summary of one out of the range of X-ray detectors*

Figures 10 and 11 respectively show a sensor tile and a completely assembled detector while Figure 12 depicts an X-ray image of a clinical phantom captured with one of the detectors out of the presented range.

7. Conclusion

In this paper a 14-bit column-parallel ADC for wafer-scale X-ray CMOS imagers is presented. The concept is highly flexible and minor circuit extensions to the basic implementation are sufficient to serve a wide product range of detectors and multiple purposes.

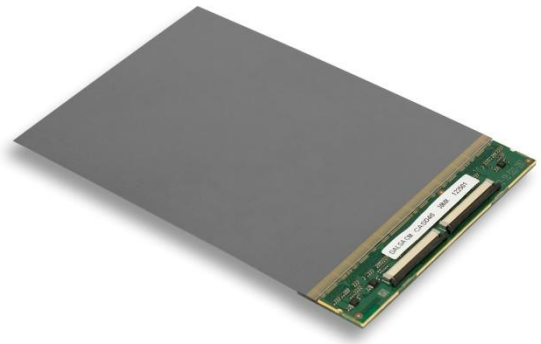

Figure 10 *Photograph of a wafer scale X-ray imager (100µm pixel pitch variant) with the 14-bit column-parallel ADC including tile PCB*

Figure 11 *Photograph of a complete X-ray detector comprising a wafer-scale imager with the 14-bit ADC, scintillator layer for X-ray to visible light conversion and interfacing electronics*

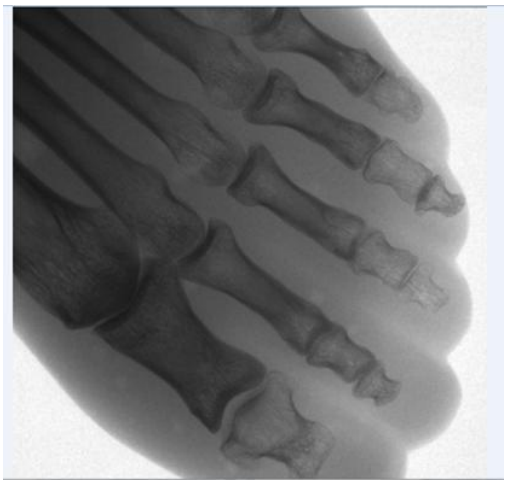

Figure 12 *Image captured with the wafer-scale X-ray detector*

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