A Two Conversions/Sample, Differential Slope Multiple Sampling ADC With Accelerated Counter Architecture

Kazuya Kitamura[1], Albert Theuwissen[2,3]

[1]NHK Science and Technical Research Laboratories, 1-10-11 Kinuta, Setagaya-ku, Tokyo 157-8510, JAPAN

TEL: +81-3-5494-3223 Fax: +81-3-5494-3197 *E-mail: kitamura.k-hi@nhk.or.jp*

[2]Delft University of Technology, Delft, the Netherlands, [3]Harvest Imaging, Bree, Belgium

Introduction

In recent years, the noise performance of CMOS image sensors has improved significantly with the implementation of a multiple sampling architecture [1-3]. In the multiple sampling architecture, the thermal noise of the pixel source follower can be reduced by a factor equal to the square root of the sampling number. The multiple sampling architectures usually employ single slope (SS) ADCs, which have a simple circuit topology, good linearity and noise performance. A low noise level of around 1 electron has been achieved [2,3]. However, one disadvantage of SS-ADCs for multiple sampling is the conversion time which increases exponentially with the number of bits. The noise reduction effect of the multiple sampling was limited by the noise in the frequency domain, i.e., 1/f noise from the pixel source follower, as the sampling time increases [2]. In the meantime, the noise level is still too high to allow a standard CMOS image sensor to perform at an ultra-low light level. To reduce the frequency domain noise, a decrease of the conversion time of the multiple sampling ADC is required. A higher clock frequency of the SS-ADC increases the operation speed, but it requires high power consumption with high thermal noise which also degrades the signal quality. Two-step A/D conversion architecture of SS-ADC has also been proposed [4,5], but they degrade the linearity and hence the image quality.

This paper introduces a differential slope (DS) ADC with a multiple sampling architecture for low noise CMOS image sensors. The DS-ADC achieves half the conversion time of the multiple sampling compared to the SS-ADC at the same clock frequency while preserving the key benefit of the SS-ADC. Employing counter acceleration architecture in the DS-ADC also halves the maximum power consumption of the digital counter.

ADC architecture

The proposed multiple sampling technique of the DS-ADC is described in Fig. 1. The basic concept of the DS-ADC is that two symmetrical reference ramps are used for the A/D conversion. The input signal level is compared with the ramp voltage, and the multiple sampling numbers are given by the number of crossing points. For 4-times multiple sampling, the conventional SS-ADC requires a time series of four ramp waveforms, whereas the DS-ADC only requires a time series of two ramp waveforms. This reduces the conversion time by half.

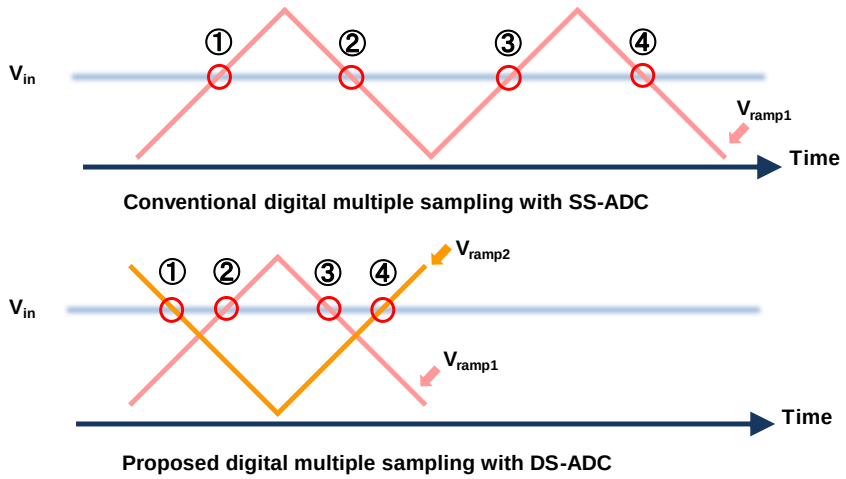

Fig. 1. Proposed DS-ADC technique.

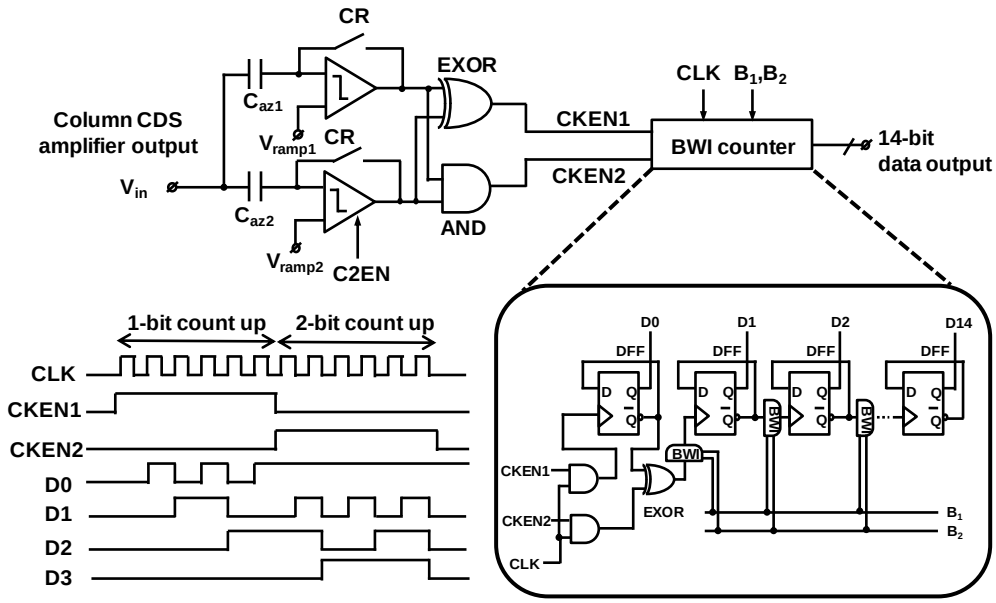

Fig. 2. Simplified column-level DS-ADC circuitry.

Fig. 2 shows the simplified circuitry of the DS-ADC. The DS-ADC consists of two comparators driven by the differential ramp voltages, a logic circuit consisting of AND and EXOR gates, and a 14-bit bit-wise inversion (BWI) counter [3] with a counter acceleration architecture. It is assumed that the input of the DS-ADC is connected to the output of the column gain amplifier which amplifies the analog signal from the pixel. The DS-ADC outputs the 14-bit code which is generated by the multiple times A/D conversion and averaging operation in the BWI counter. Generally, the counter requires the large area in the SS-ADC. To avoid the need for an additional counter for the second comparator, the proposed ADC has simple logic circuits between the comparators and the BWI counter; the outputs of both comparators are connected to the input of the AND and EXOR. The logic output of CKEN1 and CKEN2 in Fig. 2 controls the operation of the BWI counter. The BWI counter with the counter acceleration architecture consists of 14 DFFs, BWI controllers, two ANDs and an EXOR. The input clock is enabled by CKEN1 or CKEN2, and the EXOR is placed between the first DFF and second DFF to select the first DFF output or the input clock.

The operation of the ADC is as follow. The input voltage V_{in} is compared to the ramp voltages using the comparators, and while V_{in} is higher than the ramp voltages, the comparator outputs stay high. When one of the comparators is high,

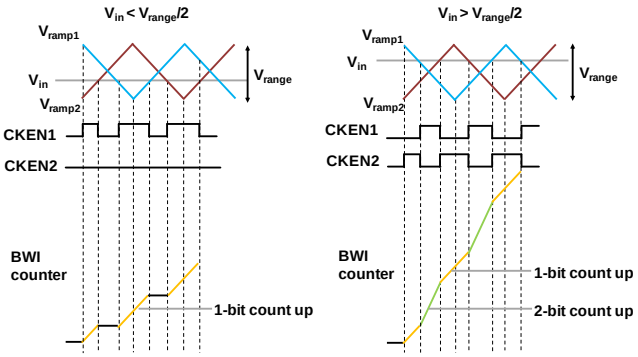

Fig. 3. 1-bit or 2-bit count up operation.

CKEN1 becomes high and the first DFF is driven by the input clock. The BWI counter works normally in 1-bit count up mode. When the outputs of both comparators are high, CKEN2 becomes high, and the second DFF is driven by the input clock. The BWI counter then works in 2-bit count up mode.

Fig. 3 illustrates the operation examples of the DS-ADC in the case of M = 6, where M is the number of the multiple sampling. When V_{in} is smaller than $V_{range}/2$, only CKEN1 operates and 1-bit count up is performed for both ramp waveforms. When V_{in} is larger than $V_{range}/2$, CKEN1 or CKEN2 operates and 1-bit or 2-bit count up is performed. This architecture thus realizes the conversion of two comparators with one counter. The advantage of this architecture is not only the reduced conversion time but also the low power

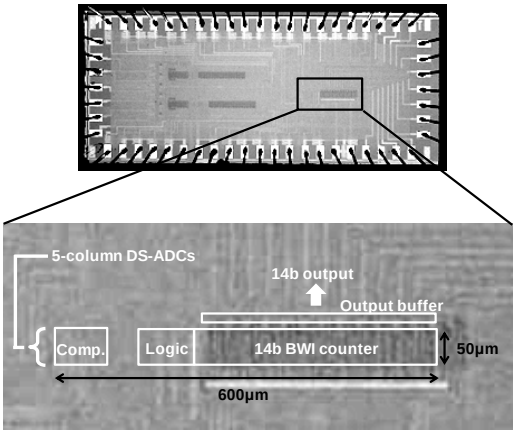

Fig. 4. Die photograph.

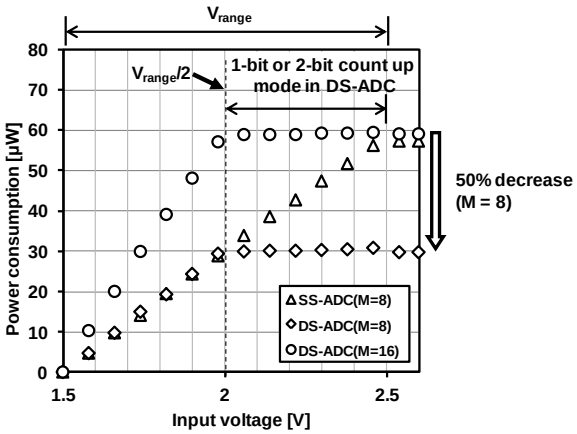

Fig.6. Measured power consumption of BWI counter.

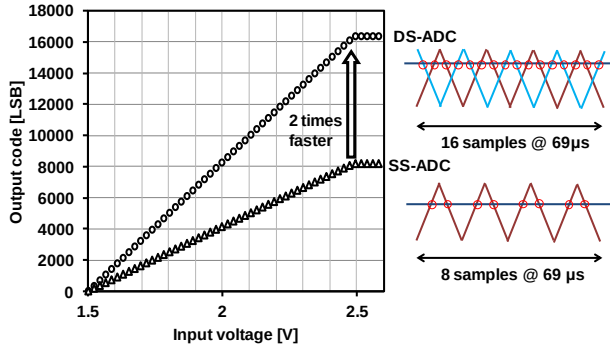

Fig. 5. DS-ADC input–output characteristics.

consumption, because the accelerated operation of the BWI counter is achieved without increasing the clock frequency.

Implementation and experimental results

The DS-ADC arrays with a 10 μm column pitch and a length of 600 μm were fabricated in a 0.18 μm one-polysilicon four-metal CMOS process on the assumption that they can be used for CMOS image sensors. A micrograph of the chip is shown in Fig. 4.

Fig. 5 shows the measured input–output characteristics of the DS-ADC compared with those of the SS-ADC. The DS-ADC operates as an SS-ADC when one of the comparator is disabled by C2EN in Fig. 2. During the measurement, a 120 MHz clock is used to drive the DS- or SS-ADCs in 10-bit mode and the conversion time for both ADCs is set to 69 μs. Compared to that of the SS-ADC, the output code of the DS-ADC is two times larger, meaning that the conversion speed is twice as fast. With the same conversion time, the DS-ADC performs 16-times multiple sampling, whereas the SS-ADC only performs 8-times multiple sampling. The conversion time of the proposed ADC is improved by a factor of two compared to the conventional SS-based multiple sampling ADC [2] at the same clock frequency of 120 MHz.

Fig. 6 shows the measured power consumption characteristics of the BWI counter as a function of the input voltage. Measurements were performed by setting the conversion time to 69 μs in all cases. In the SS-ADC, the power consumption of the counter is proportional to the input voltage. The maximum power consumption of the SS-ADC in 10-bit mode with 8-times multiple sampling is 57.2 μW. In contrast, the power consumption of the accelerated counter in the DS-ADC is flat when the input voltage is larger than $V_{range}/2$. It is because the number of the counter operation is constant during the 1-bit or 2-bit count up operation in the DS-ADC. The maximum power consumption of the DS-ADC in 10-bit mode with 8-times multiple sampling is 29.7 μW and that in 10-bit mode with 16-times multiple sampling is 59.0 μW. At the same sampling number (M = 8), the maximum power consumption of the DS-ADC is half of that of the SS-ADC. The new ADC architecture reduces the total power consumption and makes it easier to implement a large number of parallel ADC channels.

Fig. 7 shows the measured differential nonlinearity (DNL) and integral nonlinearity (INL) of the column parallel DS -ADC. The DNL and INL of the DS-ADC are +0.36/−0.36

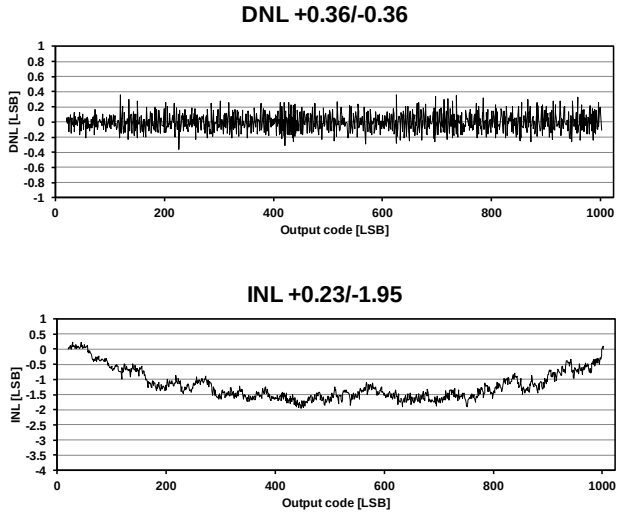

Fig. 7. DNL and INL characteristics.

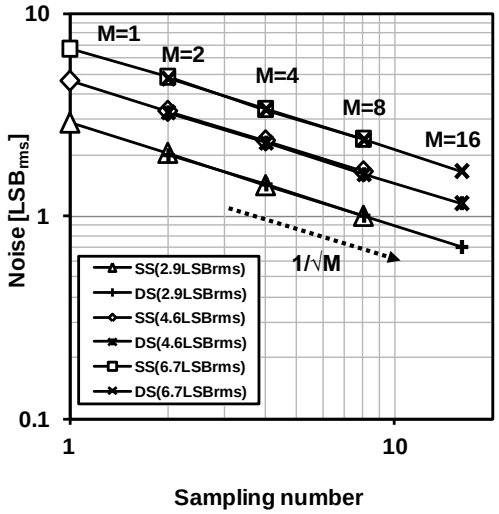

Fig. 8. Measured noise with multi sampling operation of DS- and SS-ADC.

LSB and +0.23/−1.95 LSB, respectively.

Fig. 8 shows the noise reduction effect of the multiple sampling with the DS- and SS-ADCs. A white noise generator is used for the measurement and the RMS noise of the input signal is set to 2.9 LSB_{rms}, 4.6 LSB_{rms} and 6.7 LSB_{rms}. The sampling number M of the DS-ADC is 2, 4, 8 and 16 and that of the SS-ADC is 1, 2, 4 and 8. At the same sampling number, the conversion time of the DS-ADC is half the time of the SS-ADC. Measurements show that the noise is reduced by a factor of square root of the sampling number M, which is consistent with the theory of the multiple sampling, in both DS- and SS-ADC. It is confirmed that the new ADC architecture has the noise reduction effect of the multiple sampling.

Conclusion

The two conversions/sample multiple sampling DS-ADCs with two comparators and the 14-bit accelerated counter were fabricated in a 0.18 μm CMOS process for low noise CMOS image sensors. Measurements show that compared to the SS-ADC, the DS-ADC enables half the conversion time without an increase of the clock frequency while dissipating only half the maximum power of the counter. The new ADC architecture is therefore effective for suppressing the noise in the frequency domain and suitable for use in low noise CMOS image sensors.

References

[1] S. Kawahito, et al., "Noise Reduction Effects of Column-Parallel Correlated Multiple Sampling and Source-Follower Driving Current Switching for CMOS Image Sensors," IEEE Int. Image Sensor Workshop, June 2009.

[2] Y. Chen, et al., "A 0.7e-rms-Temporal-Readout-Noise CMOS Image Sensor for Low-Light-Level Imaging," ISSCC Dig. Tech. Papers, pp. 384–385, Feb. 2012.

[3] Y. Lim, et al., "A 1.1e- Temporal Noise 1/3.2-inch 8Mpixel CMOS Image Sensor Using Pseudo-Multiple Sampling," ISSCC Dig. Tech. Papers, pp. 396–397, Feb. 2010.

[4] M.F. Snoeij, et al., "A CMOS Image Sensor with a Column-Level Multiple-Ramp Single-Slope ADC," ISSCC Dig. Tech. Papers, pp. 506–507, Feb. 2010.

[5] L. Seunghyun, et al., "A High-Speed CMOS Image Sensor with Column-Parallel Two-Step Single-Slope ADCs," IEEE Trans. Electron Devices, vol. 56, pp. 393–398, Mar. 2009.