Stack Chip Technology: A New Direction for CMOS Imagers

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Abstract

Stack chip technologies will drive a new direction for CMOS image sensors (CIS), shifting from pixel scaling to increasingly complicated design features that achieve more diverse image performance.[1-5] In this work, we developed a production ready CIS stack chip technology using a converted 1.1µm, 5 megapixel (MP) BSI product with separated CIS and ASIC masks and processes. Decoupling the ASIC and sensor processes enabled the development of a customized NMOS-pixel process that achieves dark currents (DC) < $4e^-$/s at 60°C, 1.5e^- read noise, and full well capacitance (FWC) > 7000e^-, while maintaining high peak quantum efficiency (QE), low crosstalk (SNR10 = 80 lux) and no blooming. We demonstrated this performance on a 1.1µm and a 1.0µm, 16 MP array-stacked CIS products.

Introduction

The industrial trend in CIS-technology has been a race towards smaller pixels in larger megapixel arrays[1]. The introduction of backside illuminated image sensor (BSI) technology, using standard silicon substrates, into high volume mass production, enabled pixel scaling down to 1.1µm with improved opto-electronic performance[3,4] by moving the color filter array (CFA) closer to the silicon/sensing surface, thereby increasing the QE and angular response. Buried color filter array (BCFA) and backside deep trench isolation (DTI) further improved BSI sensor optical performance[2] for large array formats. Figure 1a is a BCFA schematic showing that the CFA distance to silicon surface is further reduced resulting in improved angular response as shown in Figure 1b. Figure 2a is a schematic of a BSI-CIS with DTI; with tungsten filled backside trench to isolate adjacent pixels from electrical or optical crosstalk. Figure 2b shows the improvement in crosstalk versus incident angle achieved with a backside W-filled DTI. The next significant improvements will come from stacking technology; that is, the separate design and processing of a sensor wafer and ASIC or control wafer that are subsequently bonded together. This technology allows for the development and optimization of a pure CIS process to achieve the best imaging performance independent of the constraints imposed by ASIC or DRAM processing.

Experiment

In this work, an existing 1.1 µm, 5MP BSI CIS design was converted to a stacked chip CIS by separating the sensor and ASIC designs from one mask set into two separate mask sets as illustrated in Figure 3 and Figure 4. Metal layers were re-routed to connect the array row drivers and signal output lines on the sensor wafer to the controllers and ADC on the ASIC wafer, respectively. Alternatively, as shown in Figure 4, sub-arrays within the original 5MP array were created. Each sub-array output signal was connected to the column ADC on the converted ASIC chip, while row drivers remained outside the array and were also connected to the ASIC wafer via local, stacked interconnects. In a custom design, each sub-array would have a dedicated ADC in order to achieve frame rates of 240, 480, or 960 fps for the 256-, 128-, or 64-pixel sub-arrays (respectively) investigated in this work. With such high frame rates, pseudo global shutter performance is achievable at any pixel si**ze**. The sensor and ASIC wafers were processed separately and stacked at the wafer level, similar to standard BSI processing[4], except that the ASIC wafer replaced the BSI carrier wafer. A similar stacking and CIS process was used on two new 16MP stacked CIS products, the OV16850 (1.12**µ**m pixel) and OV16880 (1.0**µ**m pixel). These products also used the BCFA architecture described in Figure 1.

After silicon processing, stacked chip wafers were color processed, wafer-level tested, and then diced and packaged for further optical and electrical characterization. The color filter and micro-lens process for the 16-MP products were optimized for the BCFA process and pixel pitch. After packaging, parts were electrically and optically characterized as well as evaluated for production with reliability stress testing.

Results

The 5MP development vehicle described above was used to optimize the stacking process as well as the CIS process. A high functional yield was achieved with a low deadline yield loss for both stacking designs investigated in this work. Low dark current was achieved with additional annealing steps to reduce implant damage, relieve process induced stress and getter metal impurities. Low noise was achieved with improvements in the gate-oxide quality. A

high full well capacitance with no blooming or lag side-effects was achieved by tailoring implant profiles and thermal budgets to suppress dopant diffusion. These improvements were possible due to the decoupling of the ASIC and sensor processes.

Figure 5 shows a color image from the 1.1µm, 5MP stacked chip test vehicle. The pixel performance of the 16MP 1.12µm pixel product (OV16850) is shown in Figure 5 and Figure 6. High quantum efficiency with low crosstalk is achieved due to the BCFA process as well an optimized back-side optical stack. The improved process described made it possible to achieve a DC of < $4e^-$/s, low read noise of $1.5e^-$, and high FWC of $7500e^-$ without any pixel-to-pixel electrical blooming. This stack chip product completed 1000 hours of reliability stress testing (HTOL, THB, THS, T/C) demonstrating that this is a production ready process. The 1.0µm stacked-chip pixel product achieved a similar pixel performance to the 1.0µm product (data shown in Figure 7).

Summary

A production ready CIS stacking process was demonstrated on a 1.12µm and a 1.0µm CIS with high functional yield that met industry reliability standards. In addition, an accompanying sensor-only process was developed that achieved excellent pixel performance. As discussed above, the stacked chip technology demonstrated in this work will significantly improve CIS imaging. For instance, with continued development, an ADC per pixel will be realized on state-of-the-art pixel sizes, such as 1.0µm, which will result in a low noise sensor with true global-shutter performance. Individual pixels or pixel sub-arrays within larger arrays can be controlled and read out to an ADC, resulting in substantial improvements in frame rate (>10x). Additional memory per pixel can also be added, making global shutter technology and improved HDR performance possible for 1.0µm pixels. With this technology, improved IR imaging and depth ranging is also achievable.

References

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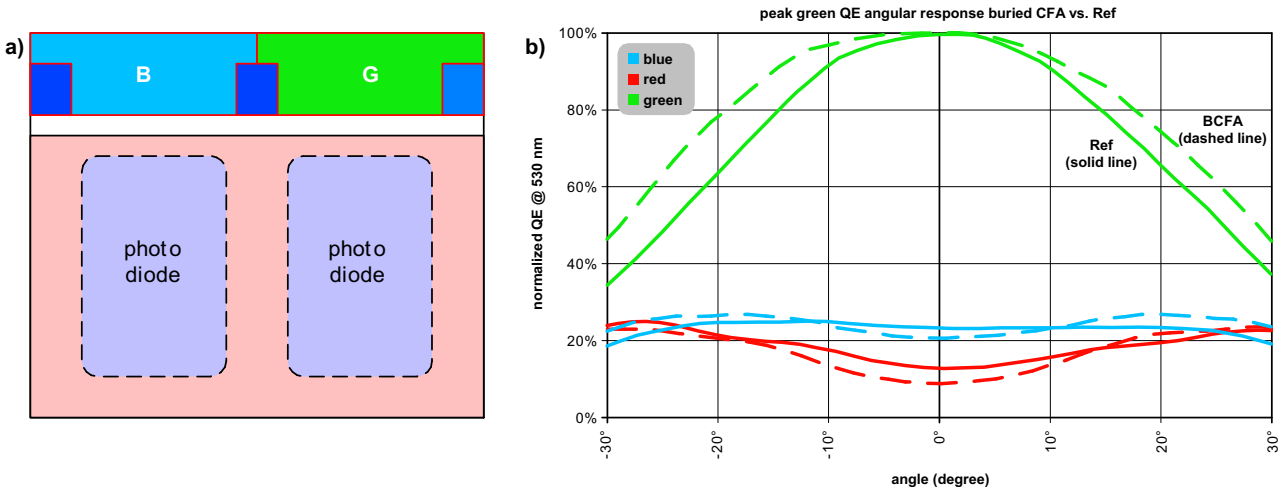


Figure 1 (a) BSI-CSI schematic with BCFA, illustrating how the CFA is closer to the silicon surface between the backside metal grid (b) QE versus incident light angle (530nm), demonstrating BCFA improves angular response. OVT 8MP 1.1µm CIS

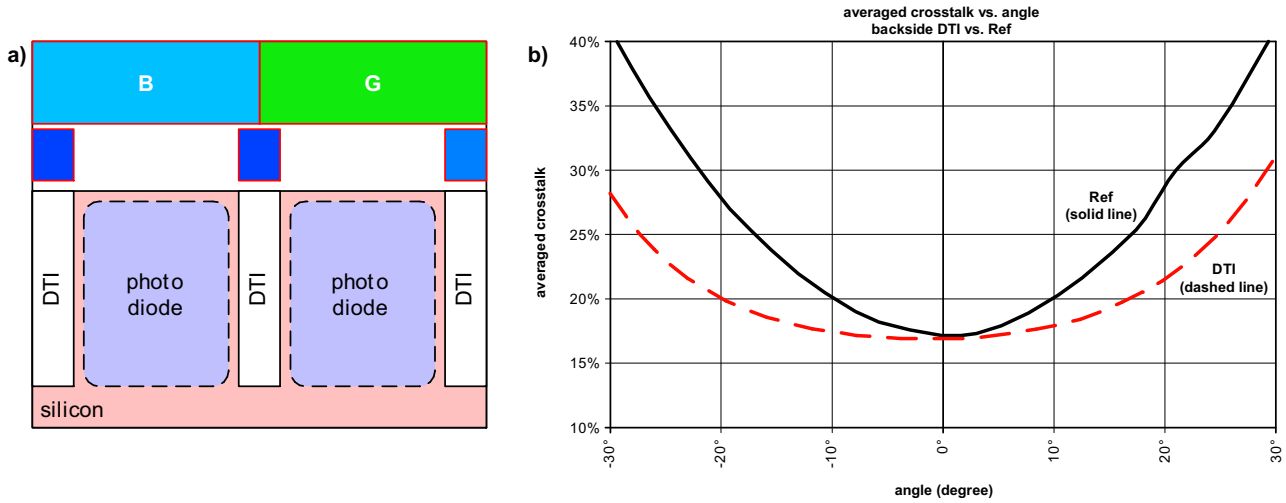


Figure 2 (a) BSI-CIS schematic with backside DTI, illustrating the W-filled trenches between each photodiode (b) average color crosstalk versus incident angle, demonstrating improved angular crosstalk with DTI. OVT 8MP 1.1µm CIS

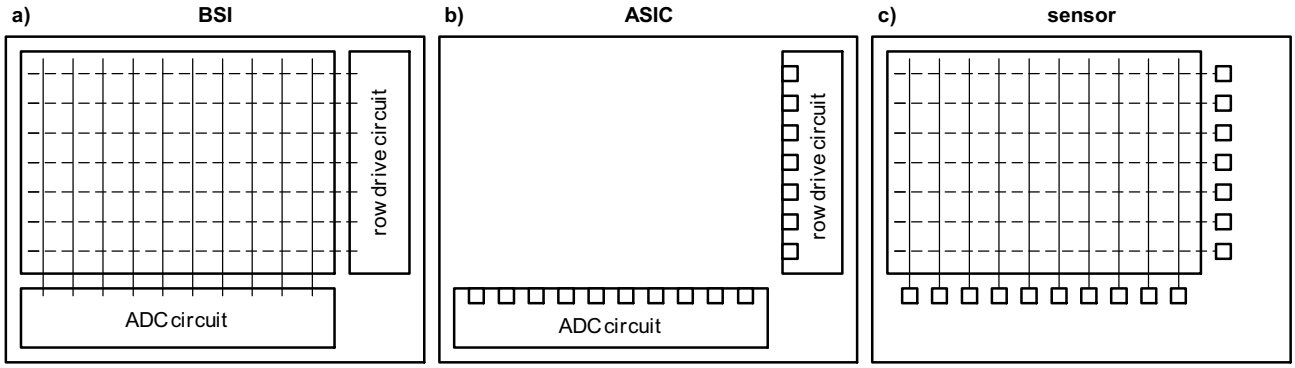


Figure 3 Illustration of mask designs used in this work. The pixel array or all the circuitry from an existing CSI-BSI design (a) was removed to create an ASIC mask (b) or a sensor mask set (c), respectively. Metal lines were re-routed and interconnect pads were added to connected pixel row lines or the output lines on the sensor mask set to the row drivers or ADC on the ASIC mask set.

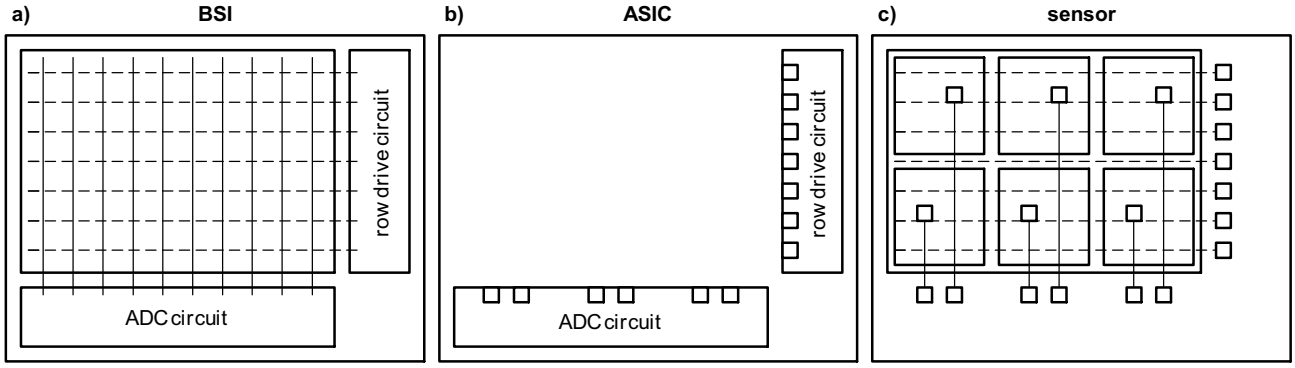
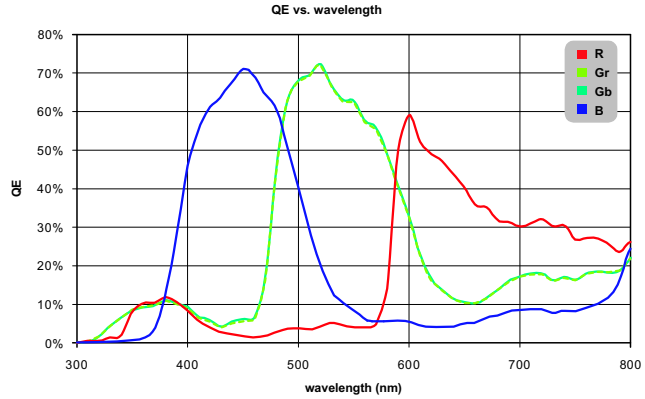


Figure 4. Illustration of alternative mask designs used in this work. The pixel array or all the circuitry from an existing CSI-BSI design (a) was removed to create an ASIC mask set (b) or a sensor mask set (c), respectively. Metal lines were re-routed to form sub-arrays, shown in (c). Local interconnect pads were added to connect the pixel row lines or the output lines on the sensor mask set to the row drivers or ADC on the ASIC mask set.

Figure 5. Color image from 1.1 µm, 5MP array, CIS stack chip (200 lux, 8x gain, 15 fps, f/2.4 lens)

a)

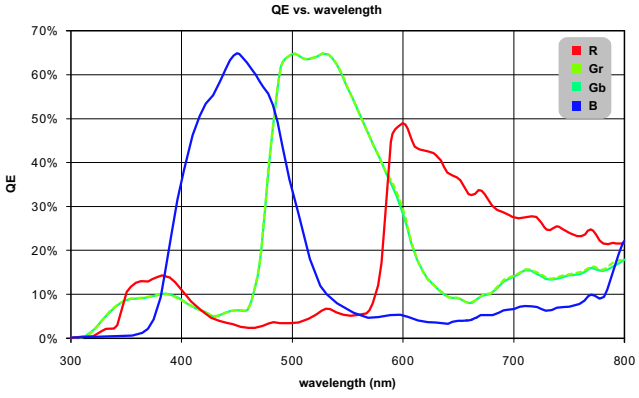


b)

	stacked, BSI chip
pixel size	1.1 µm
PRNU	<0.8%
full well capacity	7500 e^-
max SNR	37.5 dB
sensitivity - G (5100K, 650nm IR)	3800 e^-/Lux.sec
read noise @ 16x gain	1.5 e^-
SNR 10	83 Lux
dynamic range @ 16x gain	73.6 dB
dynamic range @ 1x gain	63.8 dB
dark current @ 60°C	4 e^-/sec
blooming	0%

Figure 6 (a) Quantum efficiency versus wavelength of a 1.12µm stacked, CIS-BSI with BCFA. (b) table of 1.1µm stacked, BSI chip key performance metrics

a)



b)

	stacked, BSI chip
pixel size	1.0 µm
PRNU	<0.8%
full well capacity	6500 e^-
max SNR	36 dB
sensitivity - G (5100K, 650nm IR)	3000 e^-/Lux.sec
read noise @ 16x gain	1.5 e^-
dynamic range @ 16x gain	71.7 Lux
dynamic range @ 1x gain	63.2 dB
dark current @ 60°C	4 e^-/sec
blooming	0%

Figure 7 (a) Quantum efficiency versus wavelength of a 1.0µm stacked, CIS-BSI with BCFA. (b) table of 1.0µm stacked, BSI chip key performance metrics