A 3D stacked CMOS image sensor with 16Mpixel global-shutter mode using 4 million interconnections

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Abstract

We have developed a 16Mpixel 3D stacked global-shutter CMOS image sensor with pixel level interconnections using 4 million micro bumps. The four photodiodes in the unit pixel circuit on the top substrate share one micro-bump interconnection at a 7.6µm pitch. Each signal of the photodiodes is transferred to the corresponding storage node on the bottom substrate via the interconnection to achieve a global shutter function. Those storage nodes on the bottom substrate are not just protected from incident light but also photo generated carriers. The ratio of the parasitic light sensitivity of an in-pixel storage node and the light sensitivity of a photodiode is -180dB with 3.8µm pixel size, which is smaller than our previous work and prevents any artifact by bright moving objects in the scenes for DSC usage.

Introduction

Conventional CMOS image sensors widely used in products currently on the market are mainly equipped with a rolling exposure function. This rolling exposure causes so-called “Jell-o effect” distortion when capturing a moving target. A global-shutter image sensor is ideal for digital cameras if the necessary parasitic light sensitivity (PLS), which is the ratio of the light sensitivity of an in-pixel storage node and the light sensitivity of a photodiode, is satisfied with a light-shielded storage node using the 3D stack as we proposed [1]. 3D stacking technologies have been introduced for image sensors [2-4]. Those interconnection technologies, however, set various restrictions on the numbers of interconnections, less than tens of thousands in the case of a less than 10µm pitch, and on the connection area in order to produce a high resolution global shutter image sensor over 10Mpixels. In this paper, we propose a 16Mpixel 3D stacked CMOS image sensor with 4 million interconnections at a 7.6µm pitch that connect every four pixel on the top substrate to the circuits on the bottom substrate without causing any harm to the pixel characteristics and setting a restriction on the interconnection position and area. The architecture of the sensor consists of a storage node for every photo diode to achieve a 16Mpixel global-shutter mode with a PLS of -180dB.

Image sensor architecture

Fig.1 shows a block diagram of the image sensor.

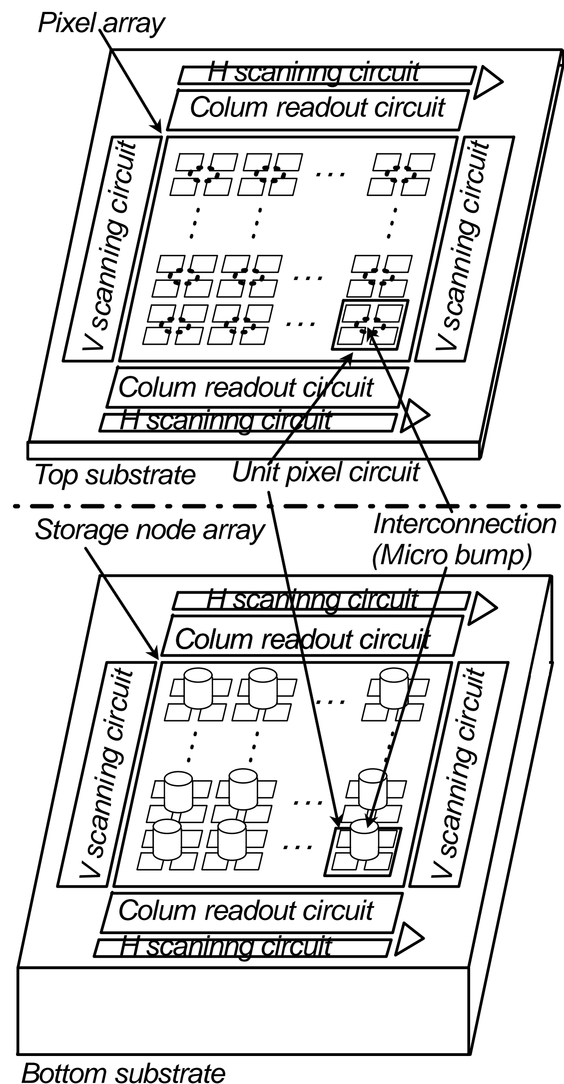

Fig.1: Block diagram of the image sensor

The image sensor comprises two semiconductor substrates bonded by micro bumps. The top substrate comprises a backside illuminated photo diode array, vertical scanning circuit and readout circuit for readout signals from the photodiode array. The bottom substrate comprises a storage node array, vertical scanning circuit and readout circuit for readout signals from the storage node array. The vertical scanning circuit on the top substrate is arrayed on both sides of the pixel array to drive the 16Mpixel array rapidly and globally, and the vertical scanning circuit on the bottom substrate is also arrayed on both sides of the storage node array to reduce the delay of the control signals.

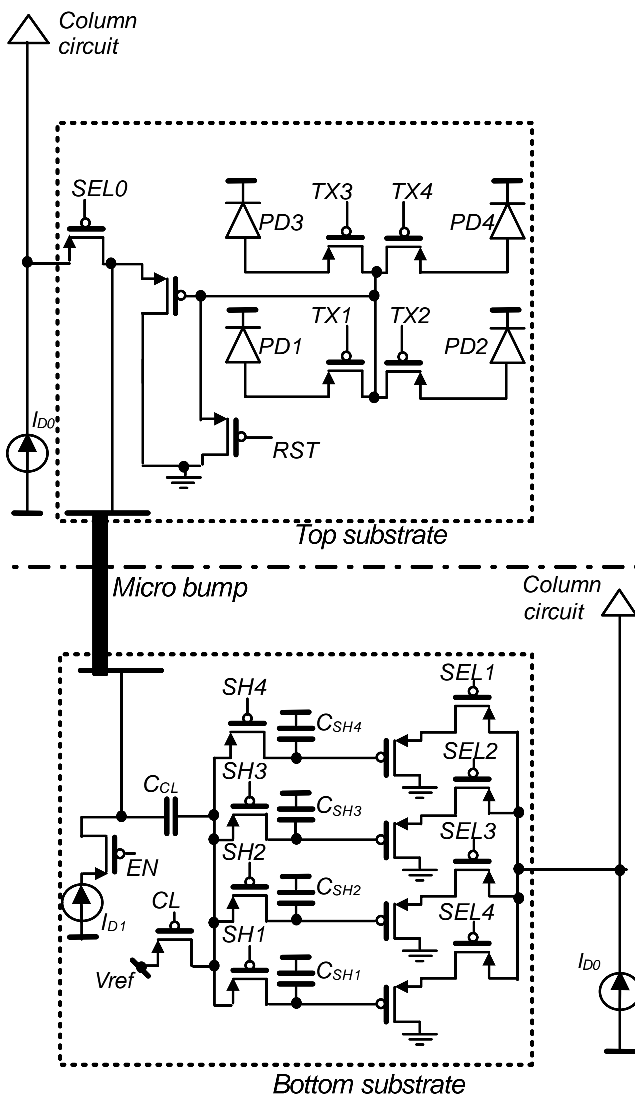

Fig.2: A unit pixel circuit of the image sensor

Fig.2 shows a unit pixel circuit of the image sensor. The unit pixel circuit of the photodiode array on the top substrate comprises four photodiodes (PD1 to PD4), four transfer transistors, one reset transistor, one source-follower transistor and one select transistor. The unit pixel circuit of the storage node array on the bottom substrate consists of one clamp capacitor and four sample hold capacitors. Compared with the former reported storage node array, this circuit is improved by the removal of three clamp transistors, achieving a 3.8μm pixel size for 16Mpixels [1]. One clamp transistor is shared for clamping four sample hold capacitors. The peripheral circuits on each substrate of the image sensor are able to operate independently and perform rolling shutter readout on the top substrate. A micro bump connects a unit pixel circuit of the photodiode array on the top substrate and a unit pixel circuit of the storage node array on the bottom substrate. This means there are 4 million micro bumps in the pixel array area for 16 million effective pixels. All transistors in unit pixel circuits are PMOS transistors.

Device structure

Fig. 3 shows a cross sectional structure of the image sensor. The image sensor consists of two semiconductor substrates bonded by micro bumps at a 7.6μm pitch. The silicon layer of the bottom substrate is light-shielded by interconnection layers on the top substrate and isolated using the 3D device structure. Thus, the storage node array is not just light-shielded but is protected from photo generated carriers. The bump connection was achieved by wafer to wafer bonding.

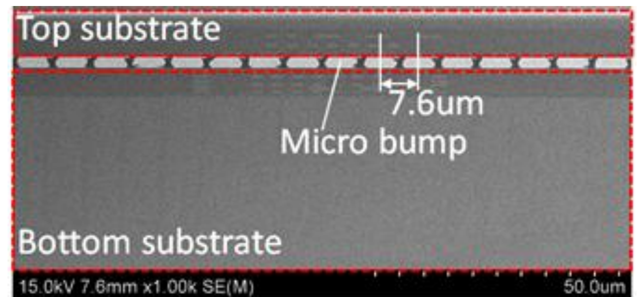

Fig.3: Cross section of the image sensor

Timing diagram

Fig.4 shows a timing diagram of the 16Mpixel global-shutter mode, which is a 4-time frame shutter operation. First, a 4-time frame reset is performed by using TX1, TX2, TX3, TX4 and RST to reset PD1, PD2, PD3 and PD4 sequentially. Second is the 4-time frame transfer operation, which starts from PD1 to

PD4. In PD1, the accumulated signals are sent to Csh1 in the storage node array with a CDS operation just after a predefined exposure time by using TX1, RST, CL, CSH1 and EN. This is also repeated to sample the amplified noise-cancelled signals from photodiodes PD2, PD3 and PD4. These 4-time frame transfer operations are all done in less than 100us, including signal transformation from 16 million photodiodes to 16 million storage nodes with the CDS operation. Current supply ID1 is enabled for only the 4-time frame transfer period by turning on the transistors controlled by using EN. The ID1 supply current is reduced to 0.1μA for the 16Mpixel global-shutter mode because of small parasitic capacitances caused by the shorter wire length of the 3D structure. Therefore, the total peak current is needed to transfer 16Mpixel signals to the storage node is 0.4A at less than the 100μs period.

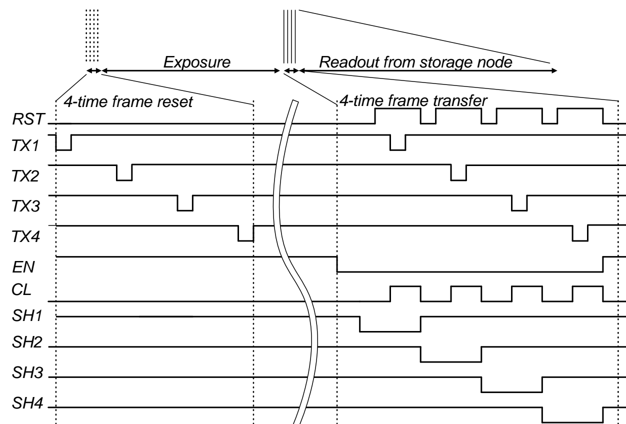

Fig.4: Timing diagram of 16Mpixel global-shutter mode

Results and discussion

Fig.5 shows a sample image of the 16Mpixel global-shutter mode.

No rolling shutter distortion was observed when capturing images with a 0.8ms exposure time. The total peak current of 0.4A for the frame shutter caused no harm because the ringing of the internal power supply and ground lines was less than 10μs.

The basic specifications of the 3D image sensor chip, the 16Mpixel global-shutter mode, are summarized in Table 1. For the basic specifications of the 3D imager chip, the top substrate was fabricated by using a 0.18μm 1P6M CMOS process, and the bottom substrate was fabricated by using a 0.13μm 1P6M CMOS process. The image sensor has a 4608 (H) × 3480 (V) pixel resolution, and the pixel pitch is 3.8μm. The image sensor has 4,008,960 micro bumps for the interconnections in a pixel array area of 17.55 × 13.22mm, and their pitches are 7.6μm. The image sensor size is 20.1 × 19.66mm. The interconnection number increased approximately 40-fold compared with our previous work due to the bigger chip size and the smaller pixel. However no distortion or degradation in characteristics due to 3D stacked image sensor was observed as well as our previous work.

Fig.5: Sample image of 16Mpixel global-shutter mode

Table 1: Specifications of the image sensor

	This work	Previous [1]
Fabrication process of top substrate	0.18μm 1P6M	0.18μm 1P6M
Fabrication process of bottom substrate	0.13μm 1P6M	0.18μm 1P6M
Chip size	20.1 × 19.66 mm	6.5 × 6.5 mm
Pixel area size	17.51 × 13.22 mm	3.03 × 2.20 mm
Effective pixels	4608 (H) × 3480 (V)	704 (H) × 512 (V)
Pixel size	3.8 × 3.8 μm	4.3 × 4.3 μm
Read out rate	5fps	30fps
Supply voltage	3.3V	3.3V
Number of interconnections in a pixel array area	4,008,960	90,112
Minimum pitch of interconnection	7.6μm	8.6μm

The measurement results of the image sensor with the 16Mpixel global-shutter mode are summarized in Table 2. Although the pixel size has reduced from 4.3μm × 4.3μm in previous work to 3.8μm × 3.8μm, its PLS has increased from -160dB to -180dB as well as the saturation signal has increased from 30Kh+ to 35Kh+, which were achieved by improving the pixel and modifying its layout enabled by 3D stacking technology. The dark current of the photodiode is 50h+/s at 60 degrees. These pixel characteristics are not affected by the wafer bonding process.

Table 2: Measurement results of the image sensor

	This work (Pixel size: 3.8um×3.8μm)	Previous [1] (Pixel size: 4.3um×4.3μm)
Conversion gain	35μV/h+	26μV/h+
Full well capacity	35,000h+	30,000h+
Sensitivity with 3200K light source	35000h+/lxs	60000h+/lxs
Dark current @60deg	50h+/s	1000h+/s
Parasitic light sensitivity (PLS)	-180dB	-160dB

Conclusion

In conclusion, a 16Mpixel 3D stacked CMOS image sensor with pixel level interconnections using 4,008,960 micro bumps at a 7.6μm pitch in a pixel array area, which set no layout restriction and causes no harm to improved sensor characteristics, was developed to achieve a distortion free 16Mpixel global-shutter mode with a -180dB PLS.

References

[1] J. Aoki et al., “A rolling shutter distortion free 3D stacked image sensor with -160dB parasitic light sensitivity in-pixel storage node,” ISSCC Dig. Tech. Papers, pp. 482-483, Feb. 2013.
[2] S. Sukegawa et al., “A 1/4-inch 8Mpixel Back-illuminated Stacked CMOS Image Sensor,” ISSCC Dig. Tech. Papers, pp. 484-485, Feb. 2013.
[3] K. De Munck et al., “High performance Hybrid and Monolithic Backside Thinned CMOS Imagers realized using a new integration process,” Proc. of the IEEE International Electron Devices Meeting, pp. 132-142, Dec. 2006
[4] K. De Munck et al., “Backside Illuminated Hybrid FPA achieving Low Cross-Talk combined with High QE,” IEEE Int. Image Sensor Workshop, pp.146-148, June 2011