A 1/1.7-inch 20Mpixel Back-Illuminated Stacked CMOS Image Sensor with Parallel Multiple Sampling

Hayato Wakabayashi Atsushi Suzuki Toshiki Kainuma Chihiro Okada Naoki Kawazu
Takumi Oka Kensuke Koiso† Atsushi Masagaki Youichi Yagasaki
Shigeru Gonoi‡ Tatsuya Ichikawa Tohru Ueda Masatoshi Mizuno‡ Tatsuya Sugioka
Takafumi Morikawa Yoshiaki Inada

Sony Corporation 4-14-1 Asahi-cho, Atsugi-shi, Kanagawa, 243-0014 Japan
†Sony Semiconductor Corporation 4000-1 Haramizu, Kikuyo-machi, Kikuchi-gun, Kumamoto, 869-1102 Japan
‡Sony LSI Design Inc. 4-16-1 Okada, Atsugi-shi, Kanagawa, 243-0021 Japan
E-mail: Hayato.Wakabayashi@jp.sony.com Tel:+81-50-3141-1136

Abstract

We have developed a 1/1.7-inch 20Mpixel back-illuminated stacked CMOS image sensor with parallel multiple sampling plus the two simultaneous output streams. This sensor has achieved the RMS random noise of 1.3e- with the parallel multiple sampling and the two simultaneous output streams of 4Mpixel for a movie mode and 16Mpixel for a still mode with a 2.3Gb/s/lane high-speed interface. The stacked structure realizes on analog implementation of the double column parallel ADCs.

1. Introduction

The demand for low-noise (for capturing a clear image in low-light conditions), high speed (for slow-motion applications and a reducing rolling shutter distortion) plus high-resolution (for formats beyond 4K) CMOS image sensors is still increasing. In addition, the emerging camcorder market typified by handsfree devices requires the simultaneous capture of still and moving images. For simultaneous capture of still and movie images, a seamless mode change has been proposed [1], but it is necessary to convert the still image (full pixel data) to a moving image (2x2 binning data) by an external Digital Signal Processor.

To improve noise performance, the conventional ways are a dynamic response pixel using a switchable floating diffusion conversion gain and a preamplifier at the foremost stage of the readout circuitry with a high analog gain [2], [3]. However the former way decreases the photo diode area and the latter increases the chip size because of an additional amplifier circuit. On the other hand, the image sensor using a pseudo-multiple sampling has been proposed without an additional circuit. However, the noise reduction effect is insufficient due to the non- uniformity of the Correlated Double Sampling (CDS) period [4].

This paper presents a 1/1.7-inch 20Mpixel back-illuminated stacked CMOS image sensor with two simultaneous output streams and a low-noise output. The parallel multiple sampling is realized not only without expanding the each CDS period but also without increasing the chip size by utilizing a stacked structure.

2. Block diagram

The block diagram of the sensor is shown in Figure 1. This sensor consists of a pixel array, the column parallel single-slope ADCs and Scalable Low Voltage Signaling interface with an Embedded Clock (SLVS-EC). Four pixels share a floating diffusion and two vertical signal lines (VSL) are assigned to each pixel column. To achieve a low-noise and high-speed readout, the sets of the two ADCs for each pixel column are located at the top and bottom sides of the pixel array. That is, the number of integrated ADCs is twice as the number of columns in the pixel array. The ADC employs the hybrid column counter [5] operating with 936MHz

clock. The speed of the SLVS-EC interface is 2.3Gb/s/lane.

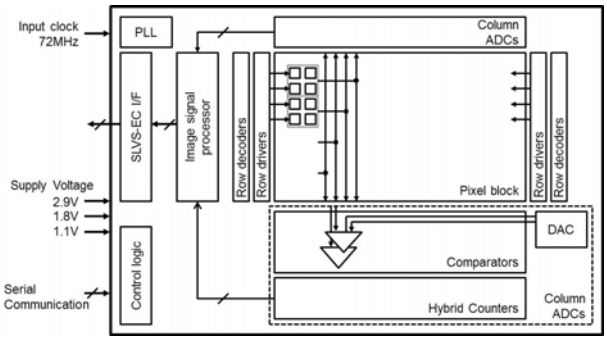

Figure1: Block diagram of the chip

3. SLVS-EC Lane information

The SLVS-EC Lane information of the two simultaneous output streams and multiple sampling data output stream are shown in Figure 2. The sensor has two Tx-Link layer circuits and eight Tx-Phy drivers and each Link layer is connected by intended drivers and the Lane is controlled according to each output stream. In this sensor, a 4Mpixel frame for the moving image outputs from two lanes as the main stream and a 16Mpixel frame for the still image outputs from six Lanes as the sub stream at 60frame/s (fps). Individual frame information is added in the header under each stream. It is possible to control the switching of sub stream at each frame.

On the other hand, the parallel multiple sampling data outputs as a one-output stream at six Lanes. To reduce the power consumption, the TX-Link2 is set to standby.

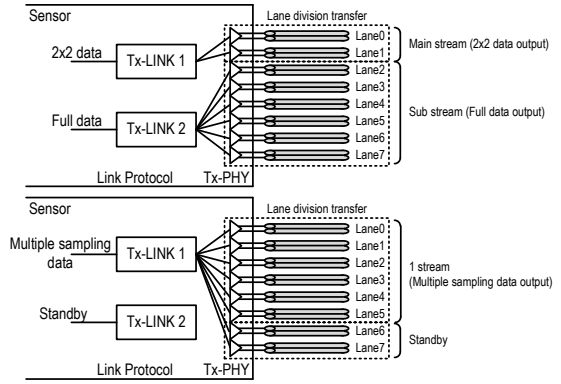

Figure2: Block diagram of two simultaneous output streams and one-output stream with lane information

4. Parallel Multiple Sampling Circuit

The parallel multiple sampling scheme is realized by a set of two ADCs that consist of two comparators, counters, and DAC. Two ADCs convert the same pixel signal to digital data by using a CDS technique. This circuit is shown in Figure 3.

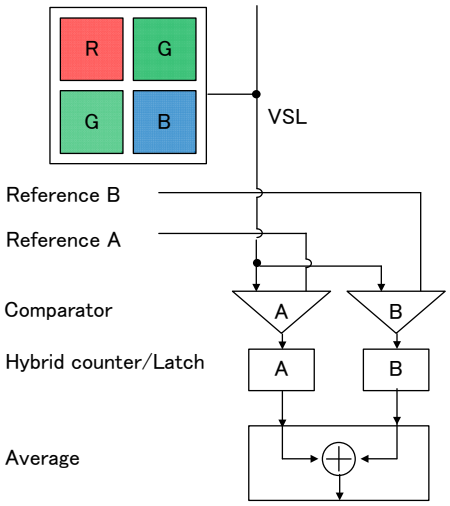

Figure3: Parallel multiple sampling circuit

The Column Parallel Correlated Multiple sampling (CMS) has been proposed [6].It can reduce the thermal noise by a factor of a square root of the sampling number and also reduce 1/f noise effectively. This scheme uses the sample-and-hold circuit, so it should be considered the bandwidth of CMS is inversely proportional to M (M is sampling number).

In contrast to that, this paper can verify the multiple sampling effects by optimizing the difference of conversion timing without considering the bandwidth. Figure 4 shows the timing diagram and this describes the difference of the two conversion timings is ΔT and each CDS period is the same.

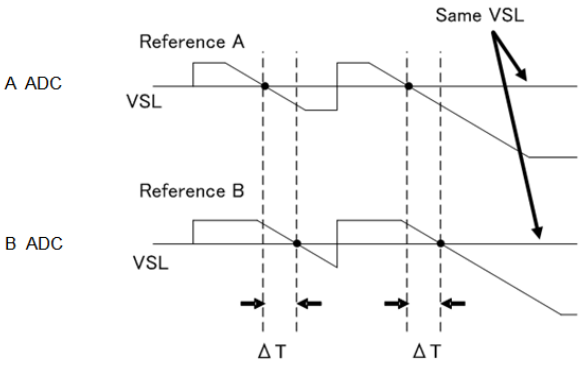

Figure4: Timing diagram for parallel multiple sampling

5. Measurements

The obtained random noise data by averaging the uncorrelated circuit is improved. The measured noise characteristic of the parallel multiple sampling is shown in Figure 5. The sensor achieves 1.3e-rms random noise which is a -3dB improvement vs. normal single sampling, where ΔT is 1.2μs. This sensor also improves not only the row temporal random noise but also the vertical FPN against a normal single sampling. As for pixel noise, the correlated multiple sampling can be reduced by optimizing the ADC timing delay.

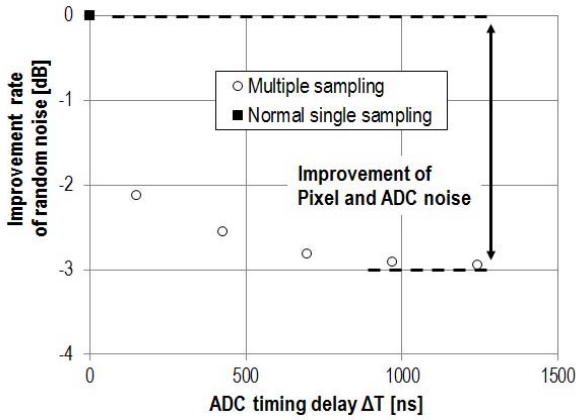

Figure5: The noise reduction effect of the multiple sampling

Item	Normal	Multiple sampling	Improvement rate
Random noise	1.84	1.29	-3.0dB
Row temporal noise	0.050	0.039	-2.1dB
Vertical FPN	0.024	0.018	-2.4dB

Figure6: Measured noise characteristics of the multiple sampling

Figure 7 indicates the sensor linearity, which shows the comparison of linearity between a normal single readout and a parallel multiple sampling readout. The measured nonlinearity shows that a parallel multiple sampling can be achieved with almost the same characteristics.

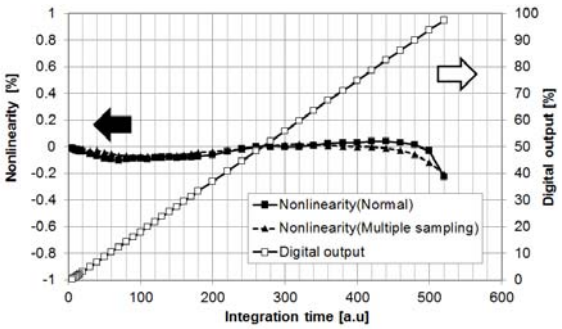

Figure7: Sensor linearity

The power consumption with the parallel multiple sampling at 20Mpixel 30fps is 532mW, and the power difference between the normal single readout and the parallel multiple sampling readout is about 116mW. Moreover, even though this sensor has double column ADCs, the chip size is not increased because the ADCs are implemented in the bottom part of the stacked structure.

The chip micrograph is shown in Figure 8. The chip size is 9.31mm (H) x 6.84mm (V).

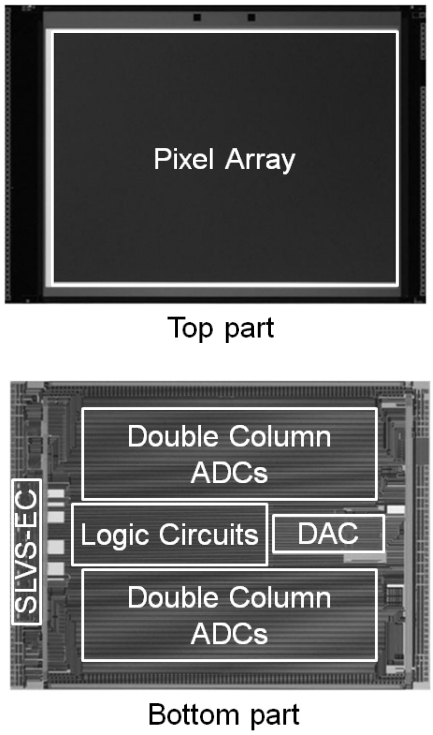

Figure8: Micrograph of the chip

6. Chip Specifications

The specifications of this sensor are summarized in Figure 9. The top part of the chip is fabricated by using a 90nm 1P4M MOS process and the bottom part of the chip is fabricated by using a 65nm 1P7M logic process. The pixel size is 1.43µm (H) x 1.43µm (V). By utilizing the parallel multiple sampling, the RMS random noise of 1.3e- is achieved at 8.47us A/D sampling period. And also the row temporal noise and the vertical FPN (without additional corrections) are measured at 0.039 e-rms and 0.018e-rms, respectively.

Fabrication Process		90nm 1P4M MOS / 65nm 1P7M Logic
Supply Voltage		2.9V / 1.8V / 1.1V
Pixel size		1.43µm (H) x 1.43µm (V)
Frame rate	Still (4:3)	30fps at 20Mpix 12b with multiple sampling
	Movie & Still (16:9)	60fps at 4Mpix 12b and 16Mpix 10b
Power consumption		532mW at 20Mpix 12bit 30fps with multiple sampling 416mW at 20Mpix 12bit 30fps
Saturation signal		9700e- at 60C
Sensitivity (typical value F5.6)		7922e-/lx-s (Green pixel, 3200K light source with IR cut filter of 650nm cut-off)
Conversion gain		76.6uV/e-
RMS random noise		1.3e- (AnalogGain:27dB)
Dynamic range		72dB at 12b

Figure9: Chip specifications

A comparison of the performance to recently published devices is shown in Figure 10. In terms of power efficiency of the noise performance, this sensor is now the state of the art.

Parameter	[9]	[5]	[7]	[8]	This work
ADC type	ΔΣ	SS	Cyclic	SAR	SS
ADC resolution [bit]	12.5	12	12	12	12
Frame rate [fps]	120	120	120	80	30
# of V pixels	1212	2160	4320	3084	3934
# of H pixels	1696	8192	7680	4620	5256
RMS random noise [e-]	2.4	2.8	3.7	1.7	1.3
Power consumption [mW]	180	3000	2540	1100	532
FoM [e-·nJ] for ADC	1.8	3.9	2.4	1.6	1.1
FoM [e-·pJ/step] for ADC	0.3	0.9	0.6	0.4	0.3

Figure10: Performance comparison

7. Conclusion

In conclusion, this paper presents a 1/1.7-inch 20Mpixel back-illuminated stacked CMOS image sensor with the parallel multiple sampling and the two simultaneous output streams. This sensor achieves the RMS random noise of 1.3e- with parallel multiple sampling. Moreover, the two simultaneous output streams of 4Mpixel and 16Mpixel at 60fps are achieved by two Tx-Links with an interface of 2.3Gb/s/lane. This sensor achieves low noise, high speed, high resolution and dual recording functionality.

Acknowledgment

The authors would like to thank the people of Sony Semiconductor Corporation, Sony LSI Design Inc. and Sony Corporation for their support of this work.

References

[1] S. Yoshihara, *et al.*, "A 1/1.8-inch 6.4MPixel 60 frames/s CMOS Image Sensor with Seamless Mode Change," *ISSCC Dig. Tech. Papers*, pp. 492-493, Feb.2006

[2] Dan Pates, et al., "An APS-C Format 14b Digital CMOS Image sensor with a Dynamic response pixel" *ISSCC Dig. Tech. Papers*, pp. 418-420, Feb. 2011.

[3] Yue Chen, et al., "A 0.7erms Temporal Readout-Noise CMOS Image Sensor for Low-Light-Level Imaging" *ISSCC Dig. Tech. Papers*, pp. 384-386, Feb. 2012.

[4] Y. Lim, *et al.*, "A 1.1e- Temporal Noise 1/3.2-inch 8Mpixel CMOS Image Sensor using Pseudo-Multiple Sampling," *ISSCC Dig. Tech. Papers*, pp. 396-397, Feb. 2010.

[5] T. Toyama, *et al.*, "A 17.7Mpixel 120fps CMOS Image Sensor with 34.8Gb/s Readout," *ISSCC Dig. Tech. Papers*, pp. 420-421, Feb. 2011.

[6] S. Kawahito, et al., "Noise Reduction Effects of Column-Parallel Correlated Multiple Sampling and Source-Follower Driving Current Switching for CMOS Image Sensors," *IISW*, June. 2009.

[7] T. Watabe, et al., "A 33Mpixel 120fps CMOS Image Sensor Using 12b Column-Parallel Pipelined Cyclic ADCs," *ISSCC Dig. Tech. Papers*, pp. 388-389, Feb. 2012.

[8] H. Honda, et al., "A 1-inch Optical Format, 14.2M-pixel, 80fps CMOS Image Sensor with a Pipelined Pixel Reset and Readout Operation," *IEEE Symp. VLSI Circuits*, pp. C4-C5, June 2013.

[9] Y, Chae, et al., "A 2.1Mpixel 120frame/s CMOS Image Sensor with Column-Parallel ΔΣ ADC Architecture," *ISSCC Dig. Tech. Papers*, pp. 394-395, Feb. 2010.