A Three-Dimensional Integration Technology with Embedded Au Electrodes for Stacked CMOS Image Sensors

Masahide Goto[1], Kei Hagiwara[1], Yoshinori Iguchi[1], Hiroshi Ohtake[1], Takuya Saraya[2], Masaharu Kobayashi[2], Eiji Higurashi[2], Hiroshi Toshiyoshi[2], and Toshiro Hiramoto[2]

[1] NHK Science and Technology Research Laboratories, 1-10-11 Kinuta, Setagaya-ku, Tokyo 157-8510, Japan,
Tel: +81-3-5494-3224, Fax: +81-3-5494-3278, Email: goto.m-fk@nhk.or.jp,
[2] The University of Tokyo, Tokyo, Japan

Abstract

We report on a novel 3D integration technology suitable for stacked CMOS image sensors by using high-density Au electrodes embedded within every pixel for vertical interconnection between silicon-on-insulator (SOI) layers. Unlike the conventional technique based on the through silicon vias (TSVs) or microbumps, the presented process is suitable for ultra-high-density 3D integration within an imaging pixel area of a few micrometers or less. We demonstrate a successful operation of the developed stacked CMOS image sensors and also evaluate the performance of the developed process, which indicates the technology is promising for high-density stacked CMOS image sensor.

Introduction

Vertical stacking of signal processing circuits is a More-than-Moore type solution to deliver multi-functions to CMOS image sensors such as high resolution, high sensitivity, and fast signal processing speed. Recent demands for higher density of sensors such as 8K imagers are escalating to reduce their pixel area down to a few μm^2. Previous works report on stacked image sensors [1-4] by using the TSV and microbump technologies. However, the diameter of the TSVs or bumps was usually larger than the imaging pixel, and such electrical interconnection is shared by multiple pixels, thereby limiting the throughput of signal processing speed.

Fabrication technology

To overcome this problem, we have developed a 3D integration technology without TSVs or bumps, as illustrated in Fig. 1 in comparison with conventional 2D sensor. Several functional layers such as photodiode (PD) and signal processors are vertically stacked, where Au interconnect electrodes are embedded in every pixel. Fig. 2 shows the fabrication process: (a) FETs for signal processor and PD are formed on a fully-depleted (FD) SOI wafer. (b) After an intermediate layer of SiO_2 is patterned, a Au layer is electroplated. (c) Chemical mechanical polishing (CMP) is applied to form embedded Au electrodes. (d) After dicing into 20-mm-square chips, the surface is activated by Ar and O_2 plasma and then directly bonded at 200 degree C. (e) To allow incident light come into the PD, the handle layer of the PD chip is grinded first and then finally removed by XeF_2 vapor phase etching. The direct bonding process allows the embedded Au electrodes smaller than 1 μm in diameter. This process can be extended to more than three-layers of stacking by repeating the above processes.

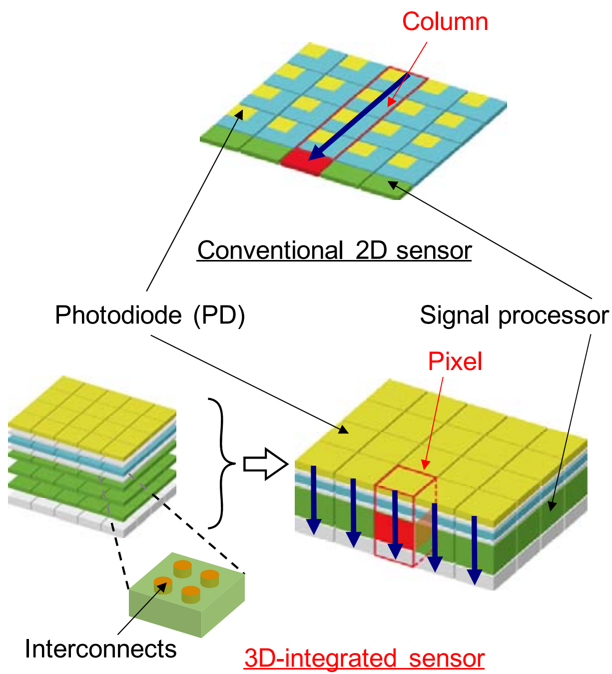

Figure 1: Proposed 3D integration technology compared with the conventional 2D type.

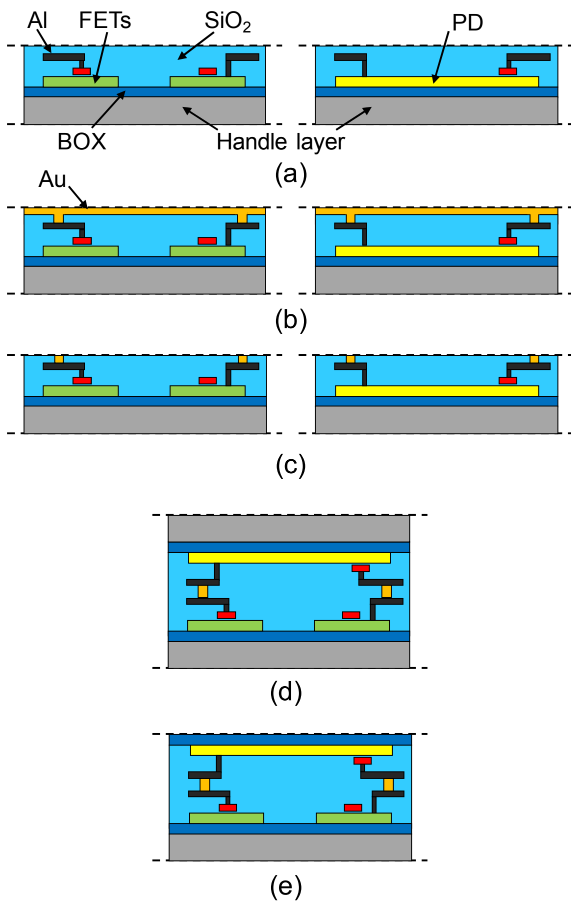

Figure 2: Fabrication process flow of the 3D integration technology.

Demonstration of prototype sensor

Photographs of a prototype sensor pixel are shown in Fig. 3 (a) before and (b) after stacking. An 80-µm-square pixel has four 10-µm Au electrodes within. A 60-µm-square PD was aligned and stacked for each pixel. The sensor output was tested, where pixel signals were converted into video images by an FPGA circuit board [5]. Fig. 4 shows examples of video images captured by the developed 8 × 8 pixel sensors, where the incident light was successfully converted into electrical signals in pixel-parallel manner through the vertically stacked electronics.

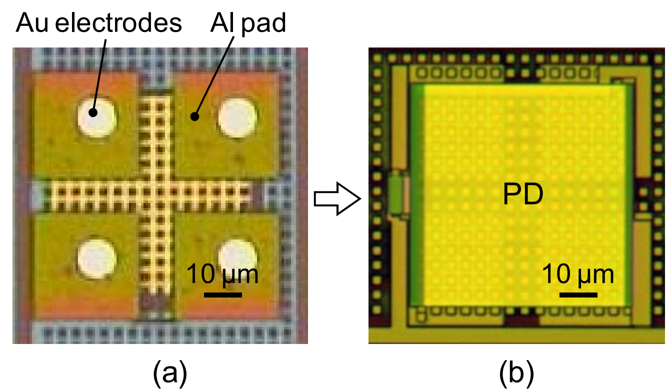

Figure 3: Photograph of prototype CMOS image sensor pixel (a) before and (b) after 3D stacking.

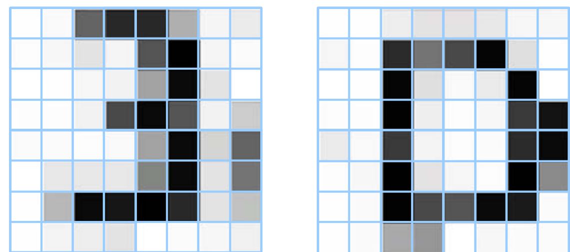

Figure 4: Examples of video images captured by the developed image sensor.

Evaluation of developed process

To evaluate the bonding reliability, a daisy-chain test-device was developed by using the aluminum wires and gold electrodes with a diameter of 10 μm [6]. Two FDSOI chips were bonded to form the daisy-chain, and the electrical resistance through many vertical interconnects was evaluated. Measurement results in Fig. 5 confirmed a series of electrical interconnection more than 23,000 electrodes. The Au resistance per contact was as small as 0.34 Ω as indicated by the inclination of the plot.

Fig. 6 shows the die shear stress measured on the bonded chips. While a sample without plasma treatment exhibited a low shear stress, the Ar and O_2 plasma processes were found to improve the critical stress to 11 MPa, which cleared the MIL-STD-883G requirement (5.9 MPa) [7].

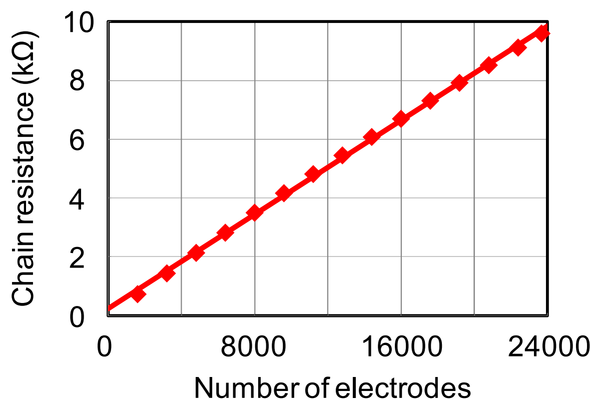

Figure 5: Chain resistance measured by using daisy-chain test device.

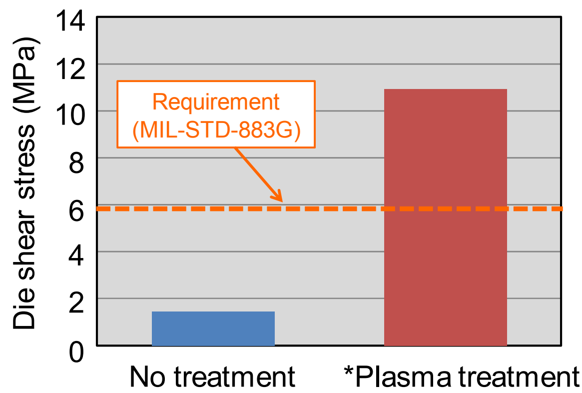

Figure 6: Measured die shear stress of bonded chips.

We have also studied on reduction of the diameter of the Au electrodes down to 1 μm. Fig. 7 shows photographs of (a) the 1-μm Au electrode embedded in the SiO_2 surfaces before bonding and (b) cross-sectional bonding interface for a 10-μm Au electrode, where no voids were observed. At this moment the misalignment was measured to be 3 μm but a precise alignment technology of as good as 1 μm is under development so as to apply our 3D integration technology to higher-density sensors with pixel area of a few μm^2.

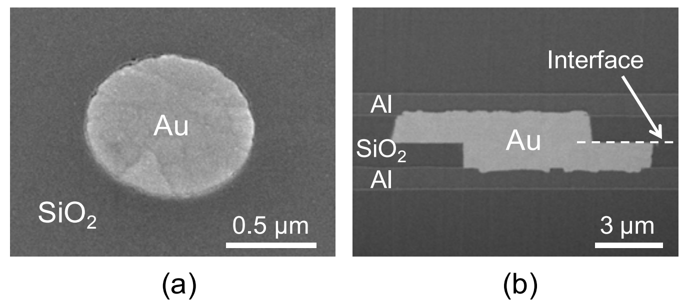

Figure 7: Photographs of Au and SiO_2 surfaces and its cross-sectional bonded interface.

Conclusion

We developed a 3D integration technology with high-density embedded Au electrodes. We demonstrated a successful operation of a stacked 8 × 8 pixel sensor and evaluated the electrical and mechanical performance of the developed process, which exhibited an excellent suitability for a stacked CMOS image sensor. This technology is applicable to most SOI-based integrated devices because it is performed at a low temperature.

References

[1] J. Aoki *et al.*, ISSCC, p. 482, 2013.

[2] S. Sukegawa *et al.*, ISSCC, p. 484, 2013.

[3] K. Lee *et al.*, IEEE T-ED, Vol. 60, p. 3842, 2013.

[4] J.C. Liu *et al.*, VLSI Tech, 21.3, 2014.

[5] M. Goto *et al.*, IEDM, 4.2, 2014.

[6] M. Goto *et al.*, IEEE T-ED, Vol. 61, p. 2886, 2014.

[7] MIL-STD-883G, Method 2019.7, 2003.