Detection and Shielding of Photon Emission in Stacked CIS

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INTRODUCTION

The mobile devices such as smart phones, tablet computers, and smart watches continue to demand thinner camera modules and smaller CIS dies with higher resolution and better performance. Similar to the industry paradigm shift from the frontside illumination (FSI) to the backside illumination (BSI) design around 2009~2010 to enhance the pixel-level fill factor and the light sensitivity, now the 3D stacking technology [1-4] is providing a new pathway to further maximizing the chip-level fill factor, adding more functions/features, and minimizing the CIS footprint at the same time. Moreover, 3D stacking decouples the process requirements for the sensor wafers from those for the ASIC wafers. Thus, process integrators have a greater degree of freedom to optimize the optical performance of the sensor and the electrical performance of the ASIC circuits independently.

During the development of the stacking process, we found unexpectedly that the circuits on the bottom ASIC layer could emit light even under normal operation conditions and the light could be detected by the pixel array on the top layer, causing degradation of image quality. In this paper, we study the nature of the photon emission, the spatial distribution, the dependence on device types, sizes, and operation conditions. From these results, we propose a set of practical design guidelines to shield the pixels from the emission.

PHOTON EMISSION IN STACKED CIS

Fig. 1(a) shows a dark image captured by a stacked 3MP test chip with 1.1u pixels. Under the high gain (e.g., 8X) and long integration time (e.g., 4s) conditions, several hot spots with different intensities are clearly observable in Figs. 1 and 2. All the hot spots can be traced back to specific transistors in the readout circuits as labeled in Fig. 1, such as the pipeline ADCs, PGAs, CDS amplifiers, DACs, and the reference generators. Our initial analysis ruled out the possibilities of temperature effects and thermal radiation. We concluded that the hot spots were the results of photon emission from the circuits under the pixel array. The sources of the hot spots were identified to be the 3.3V NMOS devices with high V_{ds} voltages. By comparing the devices of similar bias conditions but different sizes in a 12-bit pipeline ADC, we found that the hot spot intensities were proportional to the device sizes, but nonlinearly depending on the supply voltages.

Although the light emission in silicon has been known and studied in the past 30+ years [5-13], the phenomenon is probably reported for the first time here in a 3D stacked CIS. In fact, the Photon Emission Microscopy (PEM or EMMI) has become a powerful semiconductor process and circuit diagnostic tool [14-16], routinely used for detecting junction leakage, contact spiking, floating gates, avalanche breakdown, latch-up, and oxide damage problems. The known mechanisms of light emission from Si devices include the relaxation of field-accelerated hot carriers in MOS transistors and the radiative recombination of electron-hole pairs generated by hot carrier impact ionization or in forward-biased p-n junctions.

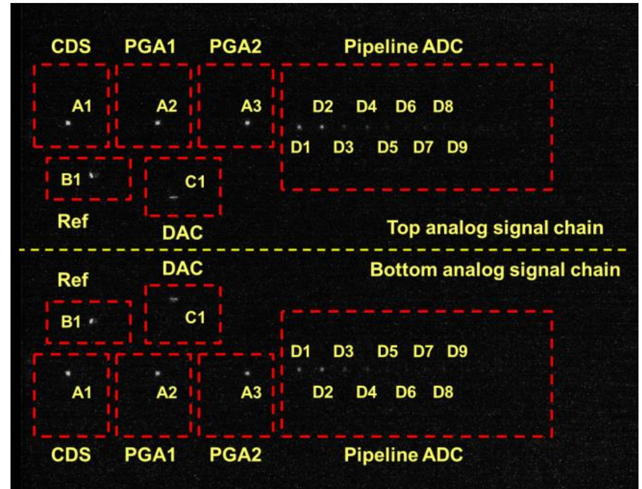


Fig. 1: A dark image captured by a 3MP, 1.1um pixel, 3D-stacked CIS showing a number of hot spots that can be precisely traced back to specific devices and circuit blocks on the bottom ASIC die.

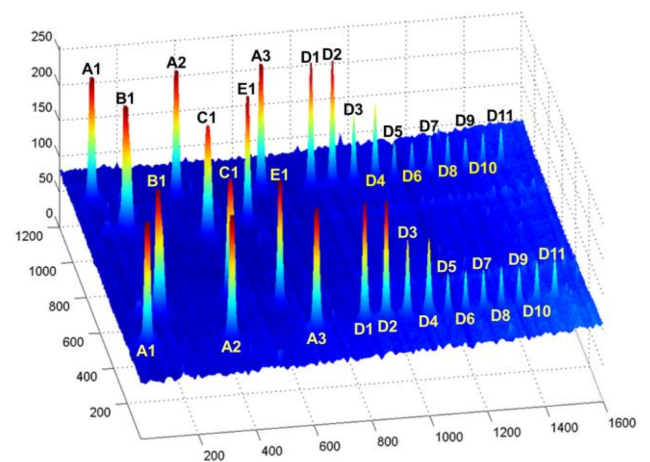
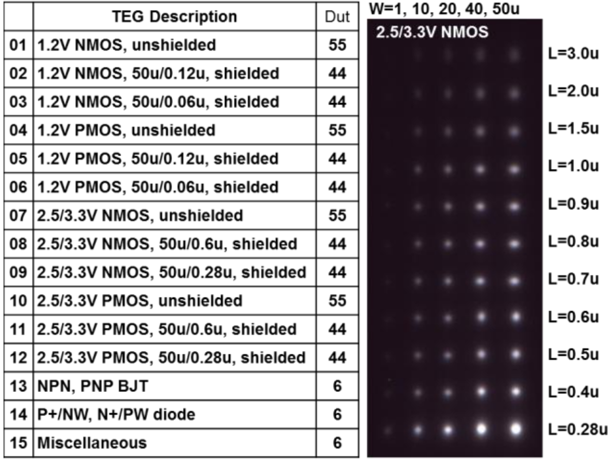


Fig. 2: 3D plot of the enhanced dark image in Fig. 1, cropped to 1600 by 1200. The intensities of the hot spots depend linearly on the device sizes, but nonlinearly on operation voltages. In this case, all emission sources are found to be NMOS devices with high V_{ds} biases (~2.4V).

PHOTON EMISSION TEST CHIP DESIGN

From the stacked CIS design point of view, the photon emission is an unwanted side effect that the designers need to be aware of and try to avoid. In order to investigate the nature of photon emission, its dependency on device types, sizes, operation conditions, we designed a group of test structures for a systematic study, as summarized in Fig. 3. The test element groups (TEG) include the 1.2V core



	TEG Description	Dut
01	1.2V NMOS, unshielded	55
02	1.2V NMOS, 50u/0.12u, shielded	44
03	1.2V NMOS, 50u/0.06u, shielded	44
04	1.2V PMOS, unshielded	55
05	1.2V PMOS, 50u/0.12u, shielded	44
06	1.2V PMOS, 50u/0.06u, shielded	44
07	2.5/3.3V NMOS, unshielded	55
08	2.5/3.3V NMOS, 50u/0.6u, shielded	44
09	2.5/3.3V NMOS, 50u/0.28u, shielded	44
10	2.5/3.3V PMOS, unshielded	55
11	2.5/3.3V PMOS, 50u/0.6u, shielded	44
12	2.5/3.3V PMOS, 50u/0.28u, shielded	44
13	NPN, PNP BJT	6
14	P+/NW, N+/PW diode	6
15	Miscellaneous	6

Fig. 3: The test element groups (TEG) incorporated in a stacked CIS test chip for photon emission study. The right hand side shows a sample dark image with a group of 11×5 unshielded 3.3V NMOS devices emitting light when biased at V_{gs}=1.2V and V_{ds}=3.0V.

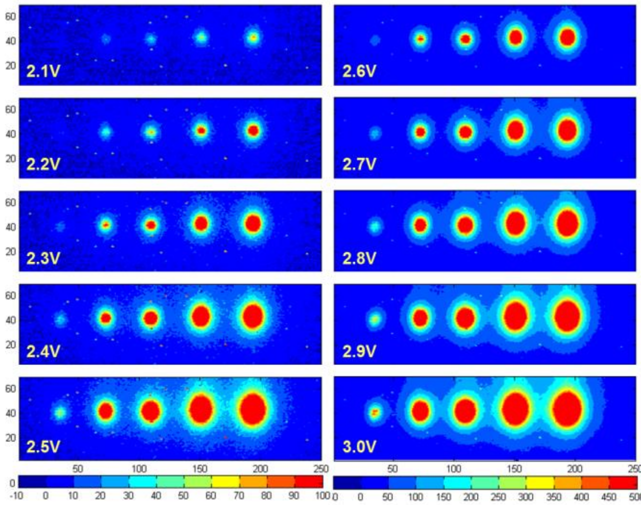


Fig. 4: Enhanced dark image contour plots of 5 NMOS DUTs in TEG-07 with L=0.28um and W=1um, 10um, 20um, 40um, 50um, respectively. The V_{gs} is fixed at 1.2V while V_{ds} varies from 2.1V to 3V. The intensities of right and left column plots are scaled differently.

MOSFETs, the 2.5/3.3V analog MOSFETs, a variety of junction diodes and BJTs, with and without metal shields. These devices can be turned ON and OFF either one by one individually, or by a group simultaneously, to facilitate the study of photon emission.

In this paper, we focus on the DC-biased 3.3V analog MOS devices. We found no detectable emission from the 1.2V MOS devices in DC operations. Because the Si-based photodiode has a cutoff energy around 1.1eV, and under the 1.2V supply, there is little probability the channel carriers can pick up sufficient energy to generate visible-spectrum photons. The near infrared emission below 1.1eV is not detected in this case. For 3.3V devices, the observable photon emission from PMOS is much weaker than NMOS, likely due to the smaller mean free path of holes than electrons. The right side of Fig. 3 shows a sample image from a group of 55 different sizes of NMOS without any metal shield. Fig. 4 shows the hot spots from 5 L=0.28u NMOS devices grow in sizes and intensities as the V_{ds} increases from 2.1V to 3V. When the V_{ds} is smaller than 2.1V, the photon emission is too weak to be reliably detected in our setup. For PMOS with similar sizes, the V_{ds} needs to be higher than 2.8V to generate observable hot spots.

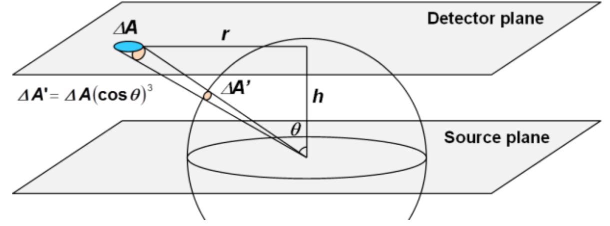


Fig. 5: The point spread function (PSF) follows a cosine-third-power law.

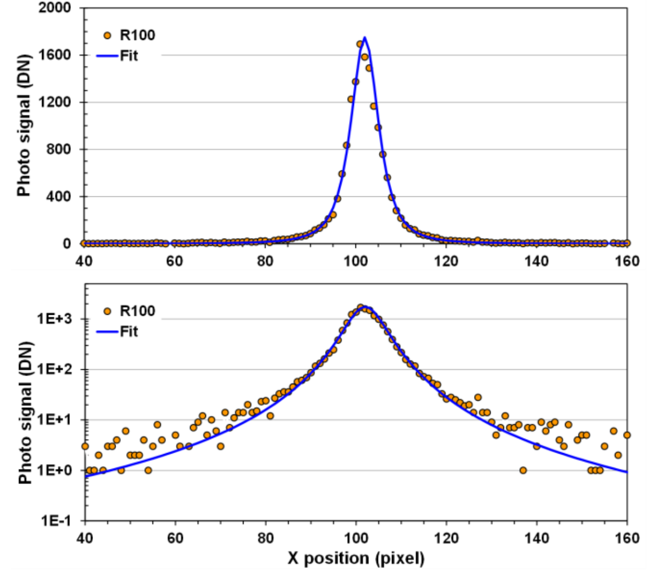


Fig. 6: Fitting the measured photon emission spatial distribution of one DUT using the simplified point spread function in Eq. (1).

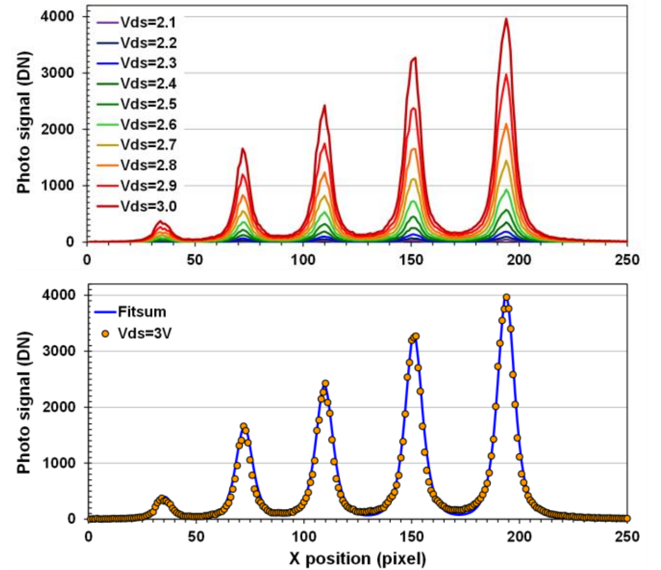


Fig. 7: Fitting the measured photon emission spatial distribution of 5 DUTs same as those in Fig. 4 using Eq. (2) with a single parameter h, the vertical distance between the source and the detector plane.

SPATIAL DISTRIBUTION

To the first-order approximation, we may consider the light emitting device as an isotropic point source from which the light spreads out uniformly in all directions. Under this simplification, the point spread function (PSF) on the detector plane can be described by a cosine-third-power law as the result of the combination of the inverse-square law and the cosine law as illustrated in Fig. 5,

$$E(r)=\left(\frac{J}{4\pi h^2}\right)(\cos\theta)^3=\left(\frac{J}{4\pi h^2}\right)\frac{1}{\left(1+r^2/h^2\right)^{3/2}}\quad, \qquad (1)$$

where J is the total emission of the point source; h is the

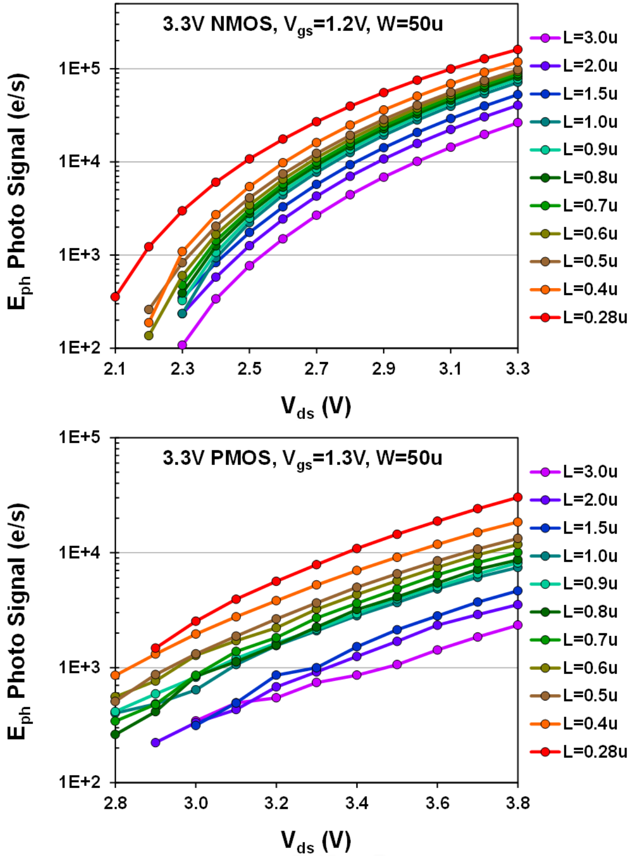


Fig. 8: Measured photon emission signal under 8X analog gain and 4s exposure time, converted to input-referred e/s, for NMOS and PMOS devices with various sizes, fixed V_{gs} and varying V_{ds}.

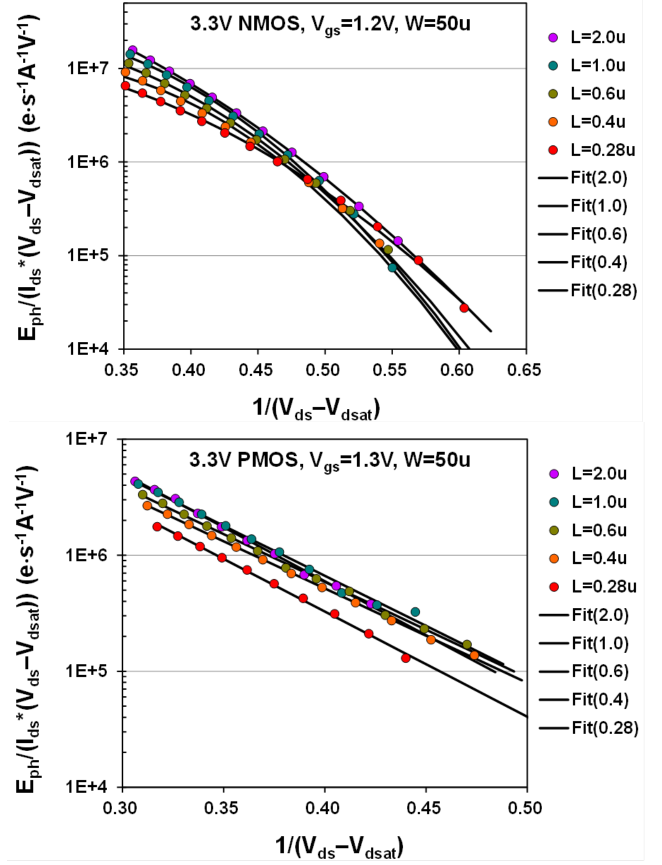


Fig. 9: Photon emission data same as that in Fig. 8, re-plotted and fit with the empirical Eqs. (3) and (4).

vertical distance between the source and the detector plane; θ is the angle between the light ray and the normal vector of the detector plane; and r is radial distance between the detector and the projected center on the detector plane. For multiple emission sources, we may sum up the contribution from each source linearly as,

$$E(x,y)=\sum_{n=1}^{N}\frac{P_n}{\left(1+\left((x-x_n)^2+(y-y_n)^2\right)/h^2\right)^{3/2}}\quad, \qquad (2)$$

where P_n is the peak signal and (x_n, y_n) is the location of each individual source.

In the face-to-face, wafer-level stacked CIS, the dielectric layer separating the emission sources on the ASIC wafer and the pixels on the BSI wafer is a complicated construct made of multiple-layer material with different refractive indices and various embedded metal and via/contact pieces. Optical simulation is required to account for the effects of light refraction, reflection, and diffraction accurately. Nevertheless, we found that the simple analytic formula could describe the measured data remarkably well as shown in Figs. 6 and 7, either for a single source or multiple sources. The only adjustable parameter used in the curve fitting was the distance h. From the numerical best fit, h is approximately equal to 5.5 pixels, or 6.05um. This is fairly close to the estimated total thickness of the actual dielectric stack, 6.25um, corresponding to the 1P4M structure for both of the ASIC and the BSI wafers used in this test chip. Therefore, for practical purposes, the empirical Eq. (2) may be used to predict the spatial distribution of hot spots in stacked CIS.

DEPENDENCE ON OPERATION VOLTAGES

For MOSFET under high V_{ds}, the majority carriers in the conduction channel are accelerated by the lateral electric field in the space-charge region. As they gradually pick up high kinetic energies, they become *hot* carriers. The photon emission can happen as a result of the hot carriers giving off their energies in the process of de-acceleration, known as the brake radiation (*bremsstrahlung*) via the interaction with lattice atoms. Alternatively, the hot carriers may generate additional electron-hole pairs through the process of impact ionization. Some of the e-h pairs may recombine radiatively to emit photons, and some of the un-recombined carriers contribute to the substrate currents. Since Si has an indirect band structure, it is known that the probability of radiative recombination is low. However, it is finite and certainly detectable. Both the brake radiation and the radiative recombination are possible causes of the photon emission. This subject has been extensively studied both experimentally and theoretically [5-16]. In our experiments, it is not possible to distinguish one process from the other. But in either case, we expect the photon emission to be strongly correlated to the hot-carrier population and the substrate current.

Indeed, the measured photo signal for 3.3V MOS in Fig. 8 showed exactly the same signature V_{ds} dependence as the substrate current I_{sub}. Due to the limitation of noise and leakage, the sensor array cannot detect reliably the photon emission for V_{ds} < 2.1V in NMOS, and for V_{ds} < 2.8V in PMOS. The weaker photon emission from PMOS is due to the lower mobility, higher effective mass and shorter mean free path of holes compared to electrons. Because the pho-

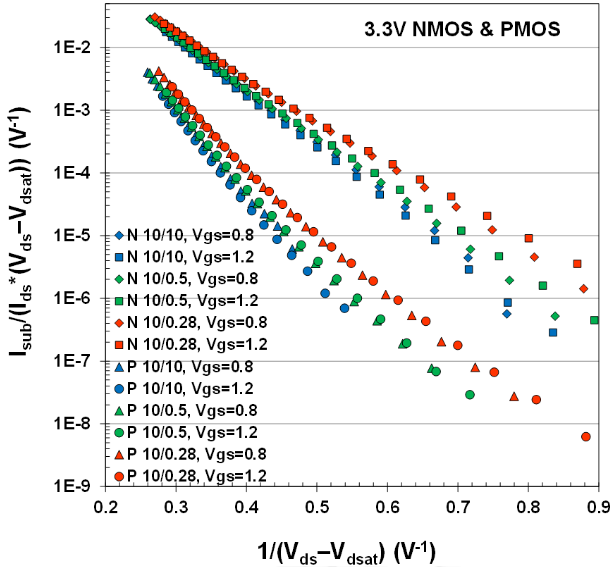


Fig. 10: Measured NMOS and PMOS substrate currents under fixed V_{gs} with V_{ds} varying from 1.5 to 4V. The saturation voltage V_{dsat} is simulated based on SPICE BSIM4 models.

ton emission and substrate current are both tied closely to the hot carrier population, it is reasonable to model the photon emission by the same equation used in BSIM4 MOSFET models describing the substrate current [17-18],

$$E_{ph} = P_0 I_{ds}(V_{ds} - V_{dsat})\exp\left(-P_1/(V_{ds} - V_{dsat})\right) \quad , \qquad (3)$$

where P_0 and P_1 are model parameters, typically binned to different device types and sizes. Fig. 9 shows that the PMOS photon emission can be fit very well by Eq. (3). However for NMOS, the data showed more curvature on the semi-log plot, we found it necessary to add another empirical quadratic term in the exponent to fit the data,

$$E_{ph} = P_0 I_{ds}(V_{ds} - V_{dsat})\exp\left(-P_1/(V_{ds} - V_{dsat}) + P_2/(V_{ds} - V_{dsat})^2\right). \qquad (4)$$

The physical justification of the quadratic term is still under investigation. For the purposes of simulation and estimation, Eq. (4) can be treated as an empirical formula with experimentally extracted parameters. For comparison, the measured MOSFET substrate currents are plotted in Fig. 10, showing the characteristics of Eq. (3). We found that the ratio of the detectable photo electrons and the measured substrate current was in the order of 10^{-9} to 10^{-10}.

METAL SHIELD DESIGN GUIDELINES

For stacked CIS, a combination of metal layers may be used to block the photon emission. The preliminary design guidelines are recommended as the following. Step 1: the designers need to identify the potential light emitting devices in the ASIC circuits, e.g., the NMOS with V_{ds} > 2.1V, the PMOS with V_{ds} > 2.8V. The forward-biased junction diodes, BJTs, and the AC-operated MOSFETs are not included in this report. The study is still a work in progress. Step 2: the intensity of the photo signal may be estimated from Fig. 8 or Eqs. (3) and (4) with technology-specific parameters, depending on the devices types, sizes, and operation conditions. Step 3: the area that needs to be shielded can be estimated by the spatial distribution function, the intensity of the emission source, and the specified maximal tolerable residual signal level. Step 4: the minimal metal shield size can then be determined by taking into account the distance between the

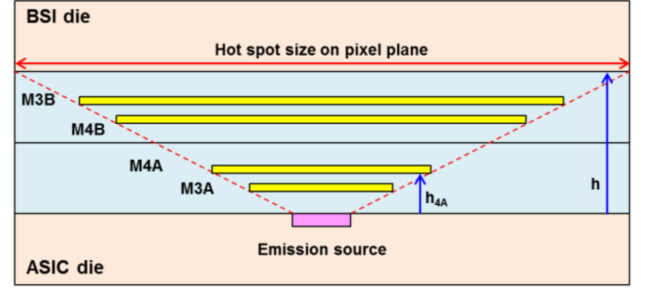


Fig. 11: The effectiveness of metal shielding depends on the distance between the metal and the source.

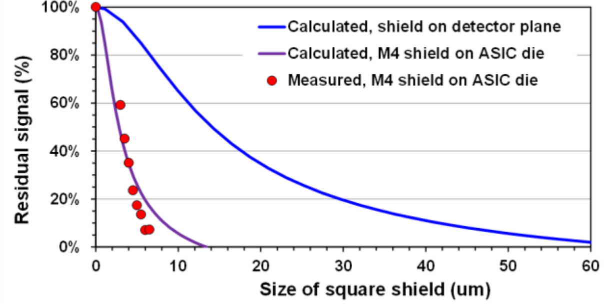


Fig. 12: Calculated and measured percentage of unshielded residual photo signal assuming a square shield centered at the emission source, based on Eq. (1) and the parameter h=6.25um, h_{4A}=1.25um.

metal shield and the source as illustrated in Fig. 11; the closer the shield is to the source, the smaller is the required size. One example in Fig. 12 shows that the experimental results match reasonably well with the calculation based on above guidelines.

CONCLUSIONS

In summary, we systematically studied the MOSFET photon emission in stacked CIS. An analytic formula for spatial distribution was derived and matched well to experimental data. We found that the photon emission was highly correlated to the hot-carrier substrate current; therefore, could be modeled by a similar equation. Based on these, we proposed a set of preliminary guidelines to design photon emission metal shield in stacked CIS.

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