The source decomposition of Dark FPN and its improvement by Stacked CIS process

Y. Yamashita, W.H. Wu, W.J. Chiang, C.H. Chung, R.J. Lin, J.J. Sze, J.C. Liu, C.H. Tseng, H. Sumi and S.G. Wuu

Taiwan Semiconductor Manufacturing Company, Ltd.
8, Li-Hsin Rd, 6, Hsinchu Science Park, Hsinchu, Taiwan 300-78, R.O.C.
Tel: +886-975904784, e-mail: yuichiro@tsmc.com

Abstract:

Based on the 1.1um, 8M-pixel tsmc process development vehicle made with 45nm CIS technology, the source decomposition of Dark Fixed Pattern Noise (Dark FPN, DFPN) and its improvement are demonstrated along with the process optimization using Stacked CIS technology[1][2]. Negative Transfer Gate Bias Operation (NB), Positive Transfer Gate Bias Operation (PB) and Floating Diffusion Leakage (FD) are three main sources, and the process optimization with Stacked CIS technology provides 20 percent total DFPN improvement with the significant reduction to PB and FD-DFPN. This result successfully demonstrates the possibility of the Stacked CIS for the pixel performance improvement, with pointing out the remaining room of improvement to NB-DFPN.

Dark FPN Modeling and Decomposition:

Figure 1 shows the example of the histogram of the dark signal output, with R.T, 240us integration time. DFPN here is the index to describe the pixel output variation, using the standard deviation of the signal distribution. [3]

Figure 2 is the diagram to model the DFPN generation. NB-DFPN and PB-DFPN are those generated by the leakage around the Transfer Gate (TG) under either negative [4]/positive [5] transfer gate bias, and FD-DFPN is the one generated at the floating diffusion. The source of the DFPN, i.e., signal variation, is induced by the dark current variation in a pixel and source follower V_{th} residual variation after CDS. In following study, the scope of the study in this paper is limited to the pixel leakage variation generated at the Floating Node (FN). Here, the dark current and white pixel component is ignored due to low temperature and short integration time.

Figure 3 is the timing diagram showing how the leakage current impacts the final DFPN performance. After the FN reset finishes, the potential of FN starts drooping due to the leakage current on the node. In period A, the amount of leakage is determined by NB component and the FD component. In period B, when the TG is turned on for the charge transfer, the leakage is determined by PB component and FD component. In period C, again NB and FN component determine the leakage. The signals at period A and C are processed by CDS, and the variation of the leakage among the pixels is seen as DFPN.

The above leakage phenomena have been confirmed with the experiments. **Figure 4** is the NB-DFPN + FD-DFPN dependency vs. interval time of CDS operation confirmed with Transfer Gate turned off. **Figure 5** is the PB-DFPN dependency vs. Transfer Gate ON time. Both results show increasing DFPN because the variation of leakage current multiplied by the interval time increases the FN voltage variation. **Figure 6** is the NB-DFPN + FD-DFPN dependency vs. TG negative bias voltage. The result shows that DFPN becomes stable when the bias voltage is more than -0.5[V]. NB-DFPN mainly comes from Gate Induced Leakage (GIL) as previously reported, and only the FD-DFPN is seen after the GIL is minimized by the relaxed biasing condition. Also note that the operation temperature is R.T. and dark current is negligible; hence we haven't confirmed the improved DFPN with lower TG bias unlike the previous study [6].

Figure 7 is the DFPN decomposition flow. The total DFPN is decomposed into individual items using 4 different images: 1) normal dark image; 2) the image without charge transfer; 3) the image with higher negative transfer gate bias; 4) the image with CDS interval equal to zero, i.e. reset sampling and signal sampling of CDS done simultaneously. The decomposition provides us the way to confirm the validity of DFPN model after the process optimization experiments.

Experimental result and Discussion:

Figure 8 is the experimental result. Compared to the control, the total thermal budget has been increased on the sample with Stacked CIS process, with expecting the better damage recovery in Silicon. Here, though the "variation" is the source of the DFPN, we rather focused on the average leakage reduction in order to minimize DFPN, under the assumption of strong correlation between average leakage and its variation.

Total DFPN of is reduced by 20 percent compared to the control. The decomposed analysis shows 24

percent and 44 percent reduction of PB-DFPN and FD-DFPN with 48 percent degradation of NB-DFPN. The guess model of this result is that the higher thermal budget helped the damage recovery, but the slight implant profile around the transfer gate increased GIL under the negative bias operation. This suggests that the next direction is the implant tuning to reduce the GIL.

References:

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[2] J.C. Liu et al., "Advanced 1.1um pixel CMOS image sensor with 3D stacked architecture," VLSI Technology (VLSI-Technology): Digest of Technical Papers, 2014 Symposium on , vol., no., pp.1,2, 9-12 June 2014

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[4] Hirofumi Yamashita et al., "Analysis of Dark Current in 4-Transistor CMOS Imager Pixel with Negative Transfer-gate bias Operation," IISW 2009

[5] Xinyang Wang et al., "Fixed-Pattern Noise Induced by Transmission Gate in Pinned 4T CMOS Image Sensor Pixels," Solid-State Device Research Conference, 2006. ESSDERC 2006. Proceeding of the 36th European , vol., no., pp.331,334, 19-21 Sept. 2006

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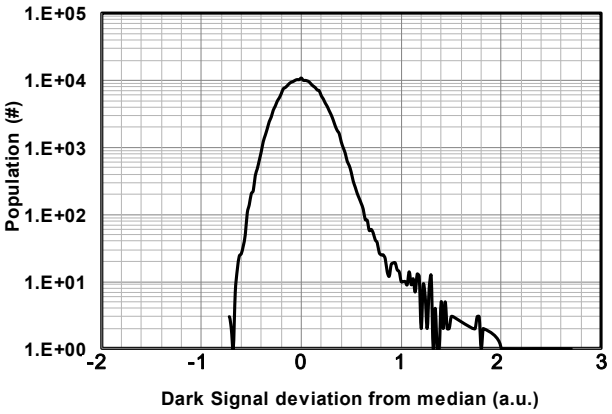

Figure 1. Histogram of the dark signal output. Total pixel = 250K pixels. T = R.T., 240us integration time.

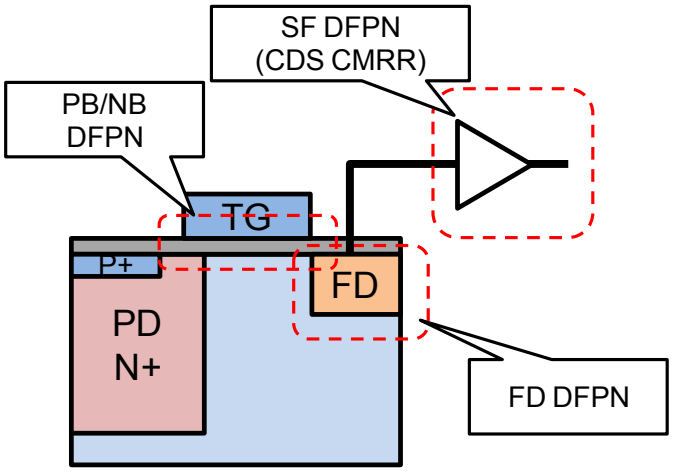

Figure 2. The model of DFPN generation

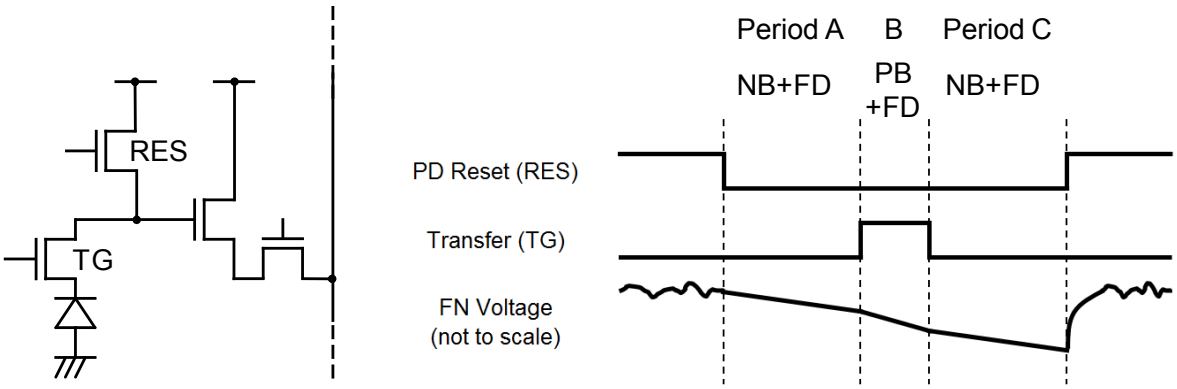

Figure 3. Pixel schematic and the timing diagram to describe the each DFPN component during the each timing interval.

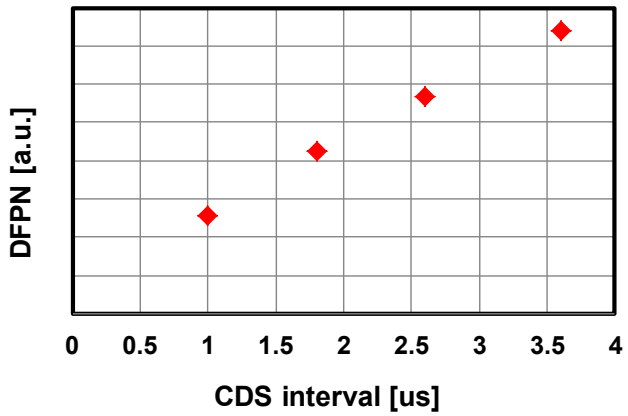

Figure 4. NB-DFPN + FD-DFPN dependency to CDS interval time.

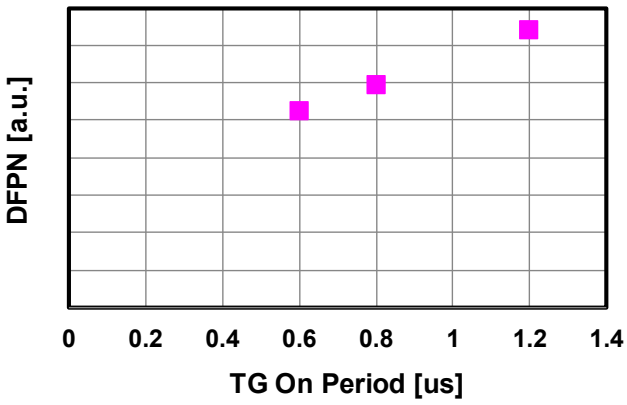

Figure 5. PB-DFPN + FD-DFPN dependency to TG On period.

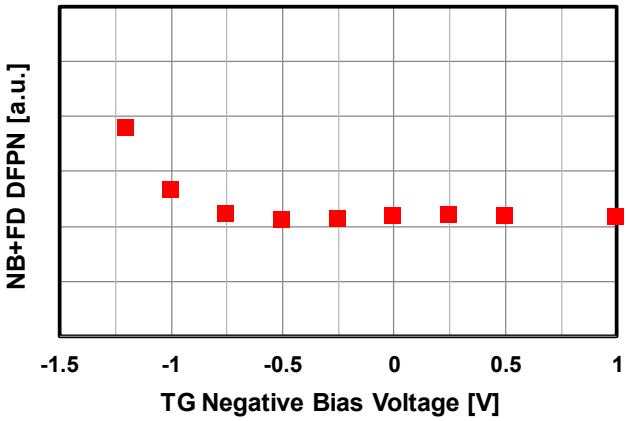

Figure 6. NB-DFPN + FD-DFPN dependency to TG Negative Bias Voltage.

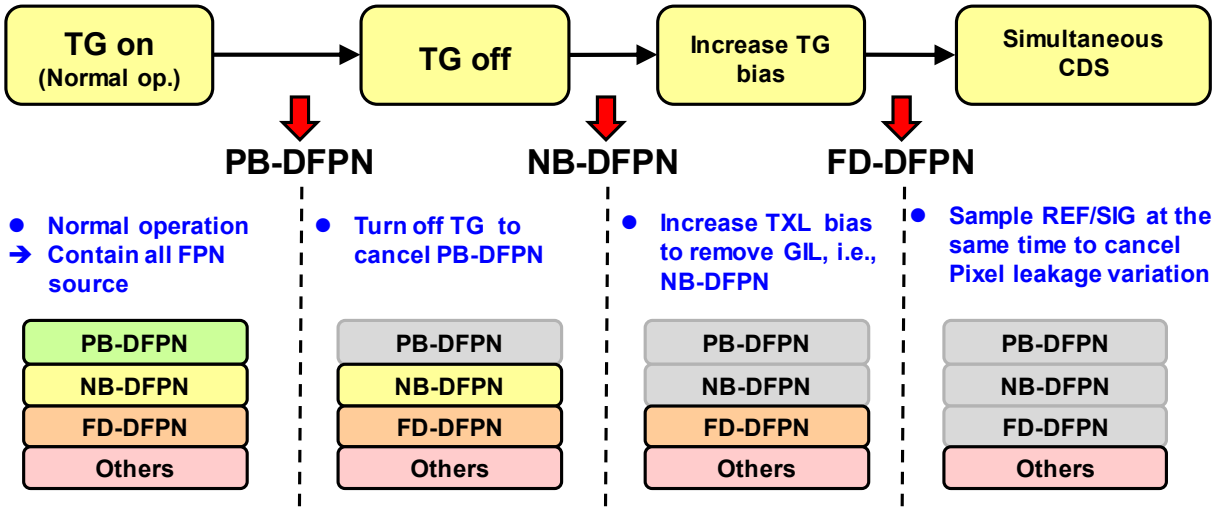

Figure 7. DFPN decomposition flow

Unit [%]	Total FPN	PB-FPN	NB-FPN	FD-FPN
Control	100	100	100	100
Stacked CIS process	80	76	148	56

Figure 8. Experimental result. FPN value in standard deviation is normalized to its control.