Interface State Generation by Substrate Injection Through the Transfer Gate

Chris Hong[1], Rick Jerome[1], David Price[1], Verne Hornback[1], Kyle Thomas[2], Rusty Winzenread[2]
[1] ON Semiconductor, 23400 NE Glisan St., Gresham, OR 97030,
[2] ON Semiconductor, 2975 Stender Way, Santa Clara, CA, 95054,
Phone: +1-503-618-5631, email: chris.hong@onsemi.com

Abstract—**This paper discusses Fowler-Nordheim stress induced dark current generation via a substrate electron injection at the Transfer Gate in a 4T pixel CMOS image sensor. It has been reported that substrate injection causes less damage to the Si-SiO$_2$ interface compared to electron injection from the gate. However, the stress effect on dark current from Fowler-Nordheim substrate injection can be enhanced at high temperatures, large bias levels and longer stress times. Negative bias on the Transfer Gate is confirmed to effectively suppress the increased dark current generated at the damaged Si-SiO$_2$ interface underneath the Transfer Gate.**

I. Introduction

It is well known that the silicon-oxide interface under transfer gate (TG) channel is one of the major sources of dark current (DC) in CMOS image sensors due to electron generation at the interface states. Depending on the gate oxide process, the Si-SiO$_2$ interface can have a large number of dangling bonds, traps and energy states because of the abrupt lattice transition. To effectively minimize dark current under the transfer gate or the spacer region adjacent to the gate, a negative bias technique has been widely utilized to suppress Shockely-Read-Hall (SRH) surface electron generation [1]. A negative transfer gate bias causes hole accumulation in the channel, filling defect sites with holes and supressing dark current generation. However, it has been reported that higher negative gate biases can create interface trapped charges via the gate injection tunneling current process [2]. If the electric field is high enough, Fowler-Nordheim (FN) tunneling or hot carrier electron injection occurs into the oxide conduction band from the gate. As a result of the energy loss process of the high energy electron in the oxide, the oxide and Si can be damaged. When the gate oxide is formed with a thickness of just a few nanometers, as is consistent with current image sensor technology, direct tunnelling at low electric fields becomes significant. Therefore, the negative TG off bias needs to be carefully optimized. Alternatively, electrons injected from the substrate due to a positive bias to the MOS gate cause less damage to the Si-SiO$_2$ interface compared to electrons injected from the gate [3]. In the case of FN tunnelling from the substrate, most of the damage is to the gate / oxide interface, which has little effect on transistor operation. Substrate injection can also increase dark current in a CMOS image sensor. Recently, we discovered that FN stress by substrate tunneling with positive bias (+Vg) on transfer gate is responsible for higher dark current in 4T pixels. In this report we will present measurements of FN stress induced dark current generation by substrate injection and calculations of the changes in dark current activation energy.

II. Experiments and Measurement

In order to measure the dark current contribution from the channel interface and exclude TG dark current from shallow trench isolation (STI) edge, several 4T, 8um-11um pitch pixel designs with pinned photodiodes (PPD) and TG length variations were fabricated as illustrated in Fig. 1 [4]. For this layout, the poly gate for the transfer gate transistor does not overlap the STI edge. Gate oxide thickness is about 65Å, so FN tunneling current can be expected in the presence of a large gate electric field on the oxide. Transfer gate bias was applied from external power supply for both negative and positive voltages. Fig. 2 shows calculated and measured FN gate tunneling current at temperatures of 30°C and 120°C. FN tunneling current as a function of temperature can be written as follows:

$$J_{FN} = \frac{q^2}{8\pi h \emptyset_b} E_{ox}^2 e^{\left(-\frac{4}{3}\frac{\sqrt{8\pi^2 m_{ox}}}{qh}\frac{(q\emptyset_b)^{3/2}}{E_{ox}}\right)} \frac{\beta\pi}{\sin(\beta\pi)} \quad (1)$$

where $\beta = k_B T \frac{\sqrt{8\pi^2 m_{ox}}}{qh} \frac{(q\emptyset_b)^{1/2}}{E_{ox}}$, $\emptyset_b$ is the barrier height, q is the electron charge, m_{ox} is the electron effective mass, E_{ox} is the electric field across the gate oxide, h is Planck's constant, k_B is Boltzmann constant and T is temperature [5]. As one can see from the measurement data and the calculated FN tunneling current in Fig. 2, there was no significant impact on FN tunneling current between the two temperatures. Dark current from the pixel array was measured as a function of TG off state bias as shown in Fig. 3. Dark current gradually improves as larger negative TG off bias is applied until -0.6V. As the TG off bias becomes less than -0.6V, dark current rapidly increases due to a trap assisted tunneling current mechanism [6]. In this report, we present dark current data for two different TG off biases, with 0V as a nominal condition and -0.6V as an alternative condition with lower dark current. Modified pixel timing was used on the sensor to keep the transfer gate transistors turned on (+Vg) inducing FN stress via substrate injection. Pixel signal value was read via correlated double sampling (CDS) and external ADC. Raw pixel image data were averaged out over several tens of frames to eliminate temporal noise. Before and after

FN stress on the TG channel, dark current at 30°C temperature and the Arrhenius activation energy (E_a) at temperatures over 60°C, where diffusion dark current is a dominant component, were measured for analysis.

III. Results and Discussion

Fig. 4 and Fig. 5 show measured dark current and E_a as a function of FN stress time with variations of stress temperature and FN bias level on the transfer gate. With the increase of stress temperature, dark current becomes larger and the diffusion E_a decreases. This clearly suggests that higher temperature enhances interface damage level with the same level of FN tunneling current as discussed in Fig. 2. Higher stress voltage results in more dark current degradation and larger shifts of E_a by about 40-60 meV, especially when TG off bias is set at 0V during dark current measurement. This tells us that the electron generation rate is enhanced by increased interface states at the Si-SiO_2 interface. Based on SRH theory, the interface generation-recombination rate is a linear function of the interface states density with a temperature dependence, and its activation energy is close to the mid-gap value [7]. Ref. 7 describes the relationship between dark current and interface state density well. Nowadays most CMOS image sensors use the pinning implantation technique in the photodiode region to passivate the Si-SiO_2 interface. However, it is not possible to implement this passivation implantation technique to the interface underneath transfer gate without affecting charge transfer and/or anti-blooming control. Interestingly, it can be seen that dark current degradation slows down or reverses with FN stress time larger than 120 minutes when FN stress was paused to measure dark current on the same device. After measuring dark current, the same device was stressed for next period of time. If FN stress is continuously applied without interruption for dark current characterization, no annealing effect was observed, as depicted in Fig. 6 where each data point represents a different device. The annealing effect can be explained by a substrate carrier injection mechanism [8]. When positive charge or negative charge traps are created by FN stress underneath the gate, the trapped charges are neutralized by means of recombination of injected carriers from photodiode and trapped charges. A feature to be noted in Fig. 4 - Fig. 5 is that negative TG off bias technique results in a significant improvement in both dark current and activation energy in the stress damaged devices. Fig. 7 shows the link of dark current to its activation energy for individual pixels from the same chip. Random defect density in each pixel spreads out the distribution of dark current and activation energy. The linear relation is predicted by the Meyer-Neldel Relation (MNR) and was observed in CCDs [9][10]. The MNR equation for dark current can be written by:

$$ln(DC) = ln(DC_{00}) - E_a\left(\frac{q}{k_B T} - \frac{q}{E_{MN}}\right) \qquad (2)$$

where DC_{00} is the dark current at isokinectic temperature in which dark current is independent of activation energy, and E_{MN} is an empirical characteristic energy. In our measurement a value of E_{MN}=0.0328eV was determined. Finally, we can extract the slopes of Eq. (2) at temperature of 30°C and 60°C. The results agree well with the slope of linear fit line as shown in Fig. 7. Fig. 7 also illustrates that negative TG off bias shifts the activation energy as well as dark current along the same characteristic line. FN stress also creates a wider distribution. Fig. 8 shows pixel distribution plots of dark current before and after the FN stress for comparison. The fact that the trend lines have a positive y-intercept with a slope of unity reveals that FN stress induced dark current degradation does not rely on initial interface state density.

Creation of interface states underneath the transfer gate is responsible for dark current degradation via FN stress and further more by broken bonds. The mechanism is depicted in Fig. 9. Electrons are injected from substrate conduction band to oxide conduction band by tunneling under substrate injection mode (+Vg) if a sufficiently high electric field is applied. For positive gate voltage, injected electrons gain high energy, and electrons cause primary damage on poly-oxide interface by losing the excess energy of 3-9 eV, generating electron-hole pairs in the gate poly and holes are injected from poly gate to oxide; however, it also contributes to silicon-oxide bonding breaking at the channel [11][12]. On the other hand, injected holes from poly gate create positive charge centers inside oxide via an impact ionization process, and the recombination with electrons leads to trap creation and trapping at the Si-SiO_2 interface. As the interface state density increases as a result of FN tunneling, the depletion dark current is increased as described by SRH generation-recombination rate.

We also investigated FN stress induced dark current dependence on transfer gate channel length (Fig. 10). Dark current shows a positive linear relation with transfer gate length when TG off state bias was 0V for both pre- and post-FN stress, and the slope of post-FN stress relation gets steeper than that of pre-FN stress dark current. This indicates that FN stress uniformly creates the interface damage under transfer gate poly. To achieve low initial interface states density and to suppress interface trap generation, fabrication process techniques must be carefully optimized for silicon substrate and gate oxide growth. With negative voltage on TG off state, the stress induced dark current dependence on transfer gate length can be significantly reduced on the same device although the negative bias technique cannot completely remove the FN stress damage effects. The linear relation between dark current versus transfer gate length disappears when a negative TG off bias is used.

IV. Conclusion

We have demonstrated FN stress induced dark current generation by substrate injection mode at transfer gate. Higher temperature and larger bias levels exacerbated FN stress induced interface damage. However, negative bias for the transfer gate off state is an effective technique to suppress the increased dark current due to the damaged Si-SiO_2 interface underneath the transfer gate.

V. Acknowledgement

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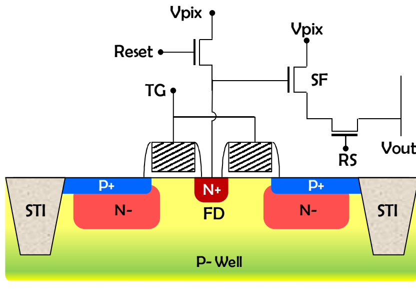


Fig. 1. Schematic view of a pixel PD and signal readout.

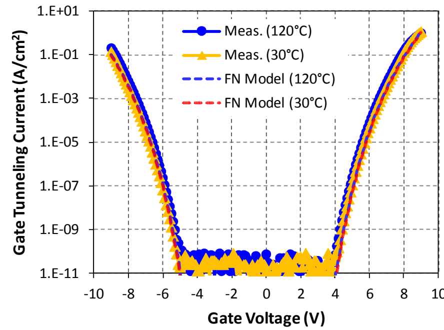


Fig. 2. Measured and calculated gate tunneling current (abs[Ig]) as a function of gate voltage, Vg.

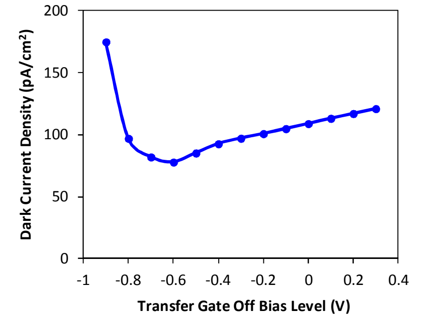
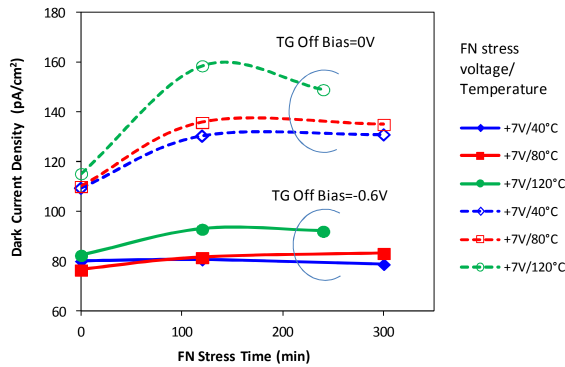
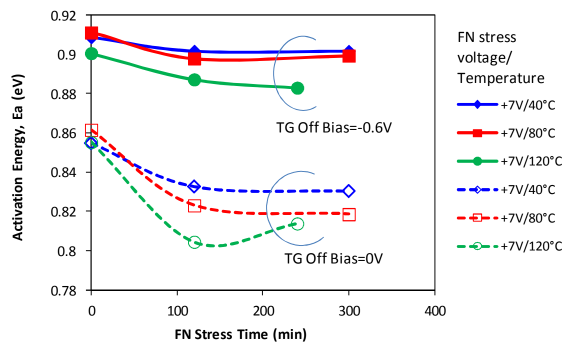


Fig. 3. Photodiode dark current measured at 30°C and normalized by pixel area.

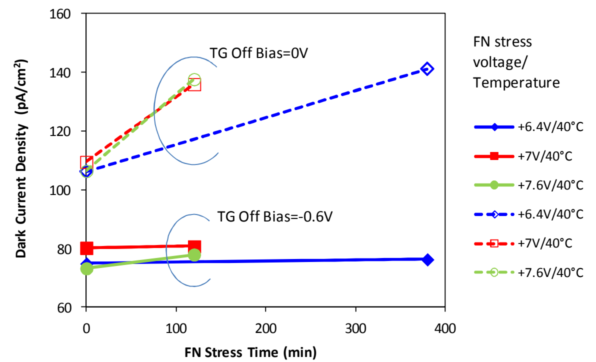


(a) dark current density vs. FN stress time

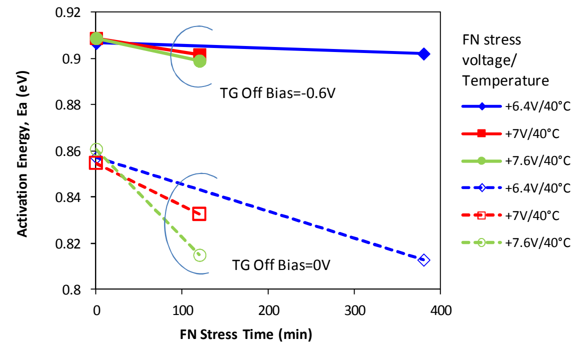


(b) activation energy vs. FN stress time

Fig. 4. (a) Dark current density and (b) E_a dependence on FN stress through TG with various temperature.



(a) dark current density vs. FN stress time



(b) activation energy vs. FN stress time

Fig. 5. (a) Dark current density and (b) E_a dependence on FN stress voltage through TG at a fixed temperature.

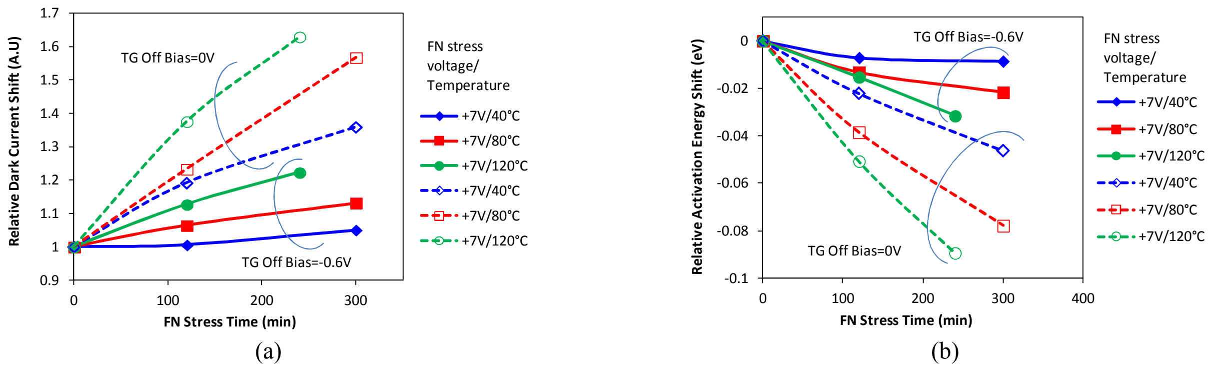


Fig. 6. (a) Dark current degradation ratio to pre-FN stress and (b) activation energy shift amount as a function of FN stress time without annealing effect.

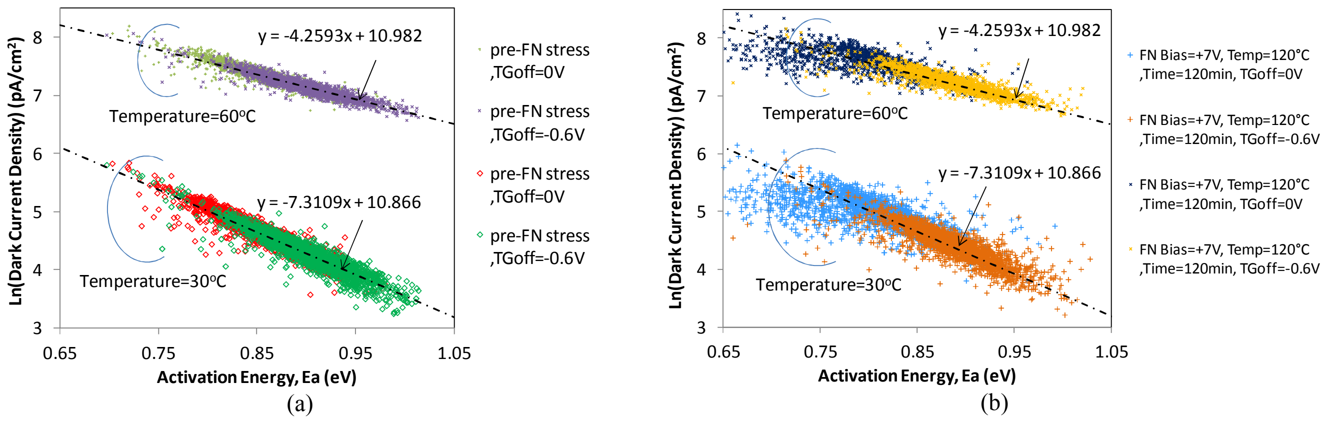


Fig. 7. The relation between dark current versus activation energy from individual pixel. Measurement temperatures were 30°C and 60°C.

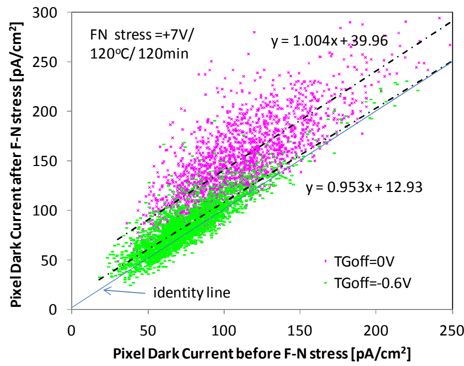


Fig. 8. Dark current distribution at 30°C between pre- and post-FN stress.

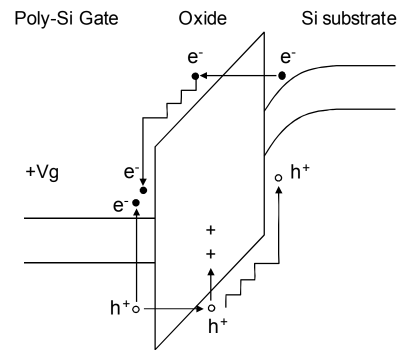


Fig. 9. Energy band diagram showing FN tunneling under substrate electron injection with +Vg.

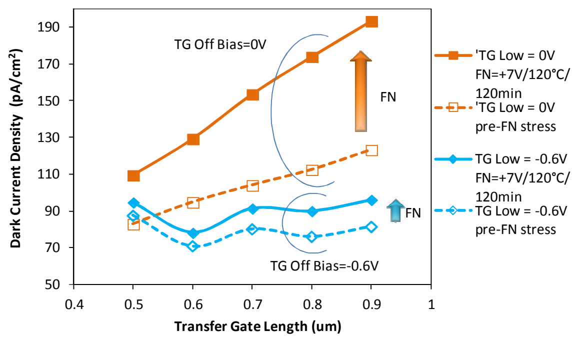


Fig. 10. FN stress induced dark current for various TG poly lengths and the effect of TG off state bias level.