Absolute Pinning Voltage Measurement: Comparison between In-pixel and JFET Extraction Methods

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I. Introduction

The pinning voltage (V_{pin}) represents a crucial design parameter in Pinned Photodiodes (PPD) CMOS Image Sensors (CIS) (Fig. 1) [1], which affects both the Equilibrium Full Well Capacity (EFWC) [2] and image lag performances. Two main approaches are currently used to estimate V_{pin}: in-pixel extraction methods [3], [4] and JFET-based extraction methods [5]–[7]. The goal of this work is to investigate whether JFET and in-pixel extraction methods provide an absolute value of the pinning voltage by comparing experimental measurements to 3D TCAD simulations. This study also shows that two different pinning voltage definitions can be used to characterize the PPD in terms of EFWC or charge transfer efficiency. All the tested devices have been designed in a commercially available $0.18\ \mu\mathrm{m}$ PPD CIS technology.

II. Experimental Results

Different JFET extraction methods, based on very different physical principles, are used in the CIS community to estimate V_{pin} (which is extracted as the pinch-off voltage V_{p} of PPD-JFET isolated structures such as the one shown in Fig. 2a). Whereas the square root (SQRT) method [5] (Fig. 3) is a well established JFET pinch-off characterization technique, other methods, such as the ones described in [7] and [6], do not provide an absolute estimation of V_{p}, as they are based on the assumptions that for $V_{\mathrm{GS}} > V_{\mathrm{p}}$ the JFET is OFF (I_{DS}=0), whereas in practice the current flowing in a JFET is never null [8].

The floating source method proposed by Coudrain et *al.* in [7] consists in leaving the source of a PPD-JFET structure floating and measuring its source potential V_{S} as a function of the applied drain potential V_{D}. The pinch-off voltage is extracted as the V_{S} potential at which V_{S} does not follow V_{D} any-more (as the JFET current I_{JFET} is assumed to be null at pinch-off). In practice, as shown in Fig. 4, V_{S} can increase when V_{D} is increased even after pinch-off. In particular,

- For $V_{\mathrm{D}} < V_{\mathrm{p}}$ (Fig. 5b), the current charging the source capacitance (I_{C}) is null when $I_{\mathrm{JFET}} = I_{\mathrm{leak}}$ (with I_{leak} the test-set-up leakage current).
- For $V_{\mathrm{D}} > V_{\mathrm{p}}$ (Fig. 5c), the JFET is in subthreshold conduction and the measured V_{S} depends on I_{leak} and on the hold time t_{H} between two V_{D} steps.

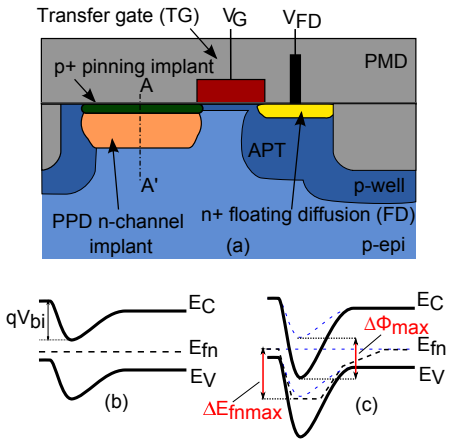

Fig. 1. (a) Schematic drawing of a PPD 4T APS. Band Diagram at equilibrium conditions (b) and at full depletion conditions (c) along the cutline A-A'. $\Delta E_{\mathrm{fnmax}}$ and $\Delta\Phi_{\mathrm{max}}$ correspond to the maximum variation of the electron quasi-Fermi level and of the electrostatic potential Φ, respectively.

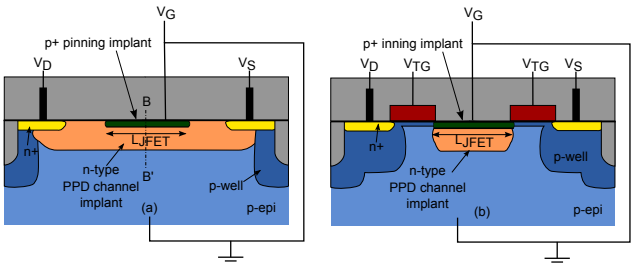

Fig. 2. (a) Schematic drawing of a PPD-JFET structure implemented with typical PPD implants. (b) Schematic drawing of a TG-PPD-JFET structure implemented with typical PPD implants.

As a result, the extracted V_{p} strongly depends on the experimental conditions and on the accuracy of test set-up.

In the extraction method proposed by Park et *al.* [6], a small voltage difference is applied between V_{D} and V_{S} (10 mV), and I_{DS} is monitored as their potential is increased with respect to V_{G}. V_{pin} is estimated as the V_D potential at which $I_{\mathrm{DS}} = 0$. As previously discussed, this condition is never reached, hence the measured V_{pin} depends on the accuracy of the test set-up (thus on the minimum measurable current). Note also that whereas the V_{pin} extracted with the SQRT method does not depend on

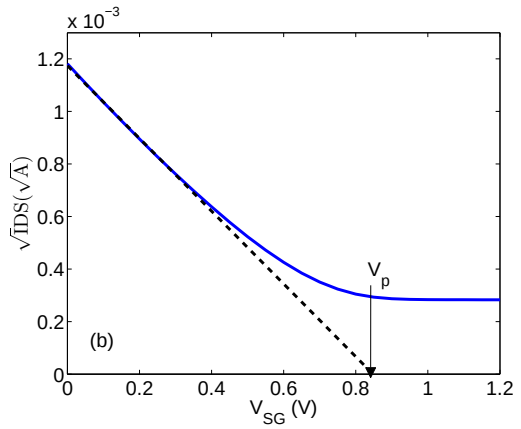

Fig. 3. Square root of the drain to source current (I_{DS}) as a function of the gate to source biasing voltage V_{SG} measured on a PPD-JFET structure (with a constant drain to source biasing voltage $V_{\mathrm{DS}} = 2\,\mathrm{V}$). In the square root (SQRT) extraction method [5] the pinch-off voltage V_{p} of the JFET can be extracted as the X-intercept of the tangent to $\sqrt{I_{\mathrm{DS}}}$ at small V_{SG}. The tested device is a PPD-JFET with $W_{\mathrm{JFET}}/L_{\mathrm{JFET}} = 2\ \mu\mathrm{m}/20\ \mu\mathrm{m}$.

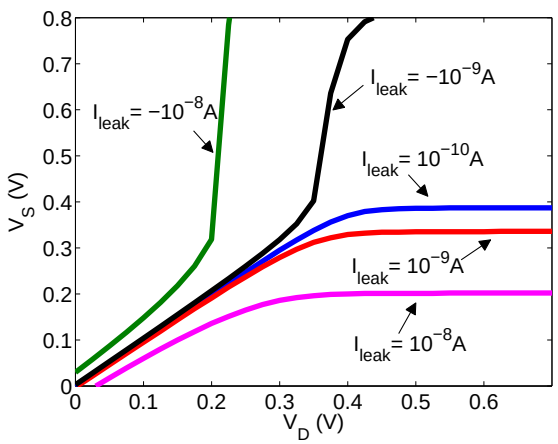

Fig. 4. Source potential (V_{S}) as a function of the drain potential (V_{D}) measured on a PPD-JFET structure for different leakage current values with the floating source extraction method [7]. The pinning voltage is extracted as the V_{S} potential at which V_{S} does not follow V_{D} any-more. As it can be observed, depending on the accuracy of the experimental set-up (I_{leak}), an arbitrary V_{p} can be estimated with this method. The tested device is a PPD-JFET with $W_{\mathrm{JFET}}/L_{\mathrm{JFET}} = 0.6\ \mu\mathrm{m}/20\ \mu\mathrm{m}$.

the W/L of the JFET, the methods in [7] and [6] depend on the absolute value of I_{JFET} and might not give the same pinning voltage for two devices with the same width and different lengths.

To respect design rules and to approach as well as possible in-pixel conditions, PPD-JFET isolated structures can be designed with a TG on both source and drain sides (TG PPD-JFET in Fig. 2b). As shown in Fig. 6 a particular care must be taken in the characterization of such structures since, if the TG and the JFET are not properly sized, the TG can limit the current flowing in the JFET and no meaningful V_{p} can be extracted.

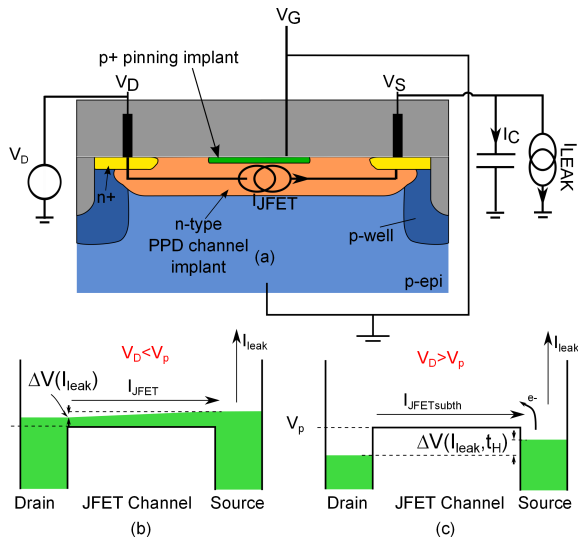

Fig. 5. (a) Equivalent circuit of the test set-up for the floating source extraction method discussed in [7]. I_{leak} can be due to parasitic leakage currents or can be forced during the measurement. As illustrated in (b) and (c), if $V_{\mathrm{D}} < V_{\mathrm{p}}$ the current charging the source capacitance $I_{\mathrm{C}} = 0$ when $I_{\mathrm{JFET}} = I_{\mathrm{leak}}$, whereas if $V_{\mathrm{D}} > V_{\mathrm{p}}$ the JFET is in subthreshold conduction and the measured V_{S} depends on I_{leak} and on the hold time t_{H} between two V_{D} steps.

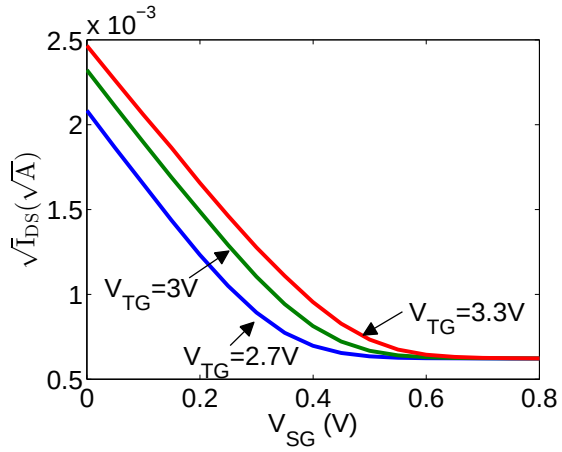

Fig. 6. Experimental measurement: square root of the drain to source current I_{DS} as a function of the gate to source voltage (V_{SG}) measured on a TG-PPD-JFET structure (Fig. 2b). As it can be observed, I_{DS} always depends on the TG biasing voltage V_{TG} and no meaningful V_{pin} can be extracted. The tested device is a TG-PPD-JFET with $W_{\mathrm{JFET}}/L_{\mathrm{JFET}} = 10\ \mu\mathrm{m}/20\ \mu\mathrm{m}$. The TG size is $W_{\mathrm{TG}}/L_{\mathrm{TG}} = 10\ \mu\mathrm{m}/0.7\ \mu\mathrm{m}$

III. Definition and Estimation of the Pinning Voltage

In the literature, V_{pin} is defined as the maximum deviation $\Delta E_{\mathrm{fnmax}}$ of the electron quasi-Fermi level from the Fermi level at equilibrium [9], whereas in TCAD simulations it is often extracted as the maximum variation of the electrostatic potential ($\Delta\Phi_{\mathrm{max}}$) between equilibrium and full depletion conditions [1], [10]. In this work, these two pinning voltage definitions will be referred to as $V_{\mathrm{pin}\Delta\mathrm{E_{fn}}}$ and $V_{\mathrm{pin}\Delta\Phi}$, respectively.

Both in-pixel and JFET pinning voltage measurements have been simulated to answer the following questions:

- Do the two methods provide the same pinning voltage?

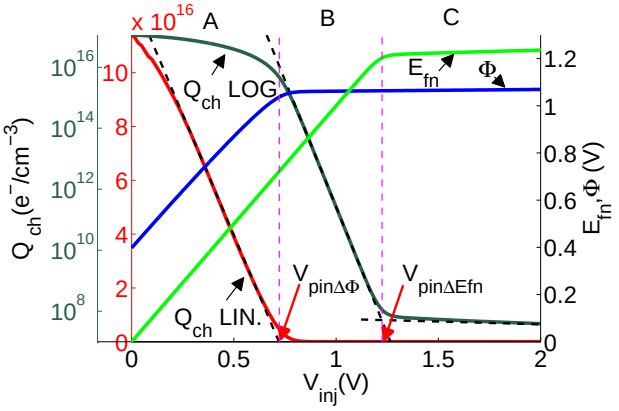

Fig. 7. TCAD simulation: maximum Φ and E_{fn} (along the cutline B-B' in Fig. 2a) and maximum JFET channel charge density $Q_{\mathrm{ch}}^{'}$ (in linear and logarithmic scales) plotted as a function of the biasing potential V_{inj} applied to both the source and drain of a PPD-JFET. The simulated device is a 3D PPD-JFET device with $W_{\mathrm{JFET}}/L_{\mathrm{JFET}} = 2.5\ \mu\mathrm{m}/2.5\ \mu\mathrm{m}$.

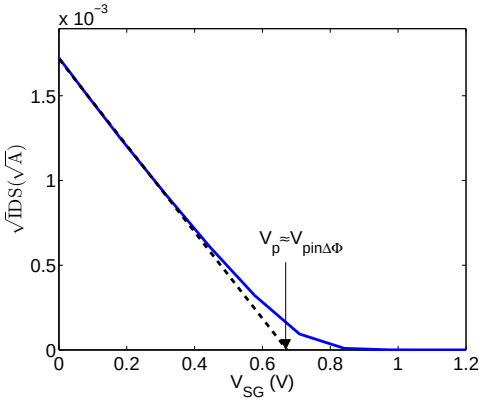

Fig. 8. TCAD simulation of the SQRT method on the same 3D PPD-JFET structure as in Fig. 7: by comparing the curve to Fig.7, it can be observed that the estimated V_{p} well approximates $V_{\mathrm{pin}\Delta\Phi}$. Note that TCAD simulations have not been calibrated to fit experimental measurements, thus the simulated V_{pin} is not meant to correspond to the one extracted from the experimental data presented in Fig. 3.

- Which definition ($V_{\mathrm{pin}\Delta\Phi}$ or $V_{\mathrm{pin}\Delta\mathrm{E_{fn}}}$) better represents the extracted pinning voltage?

Figure 7 shows the evolution of Φ, E_{fn}, and of the PPD channel charge density $Q_{\mathrm{ch}}^{'}$, with the biasing voltage V_{inj} applied to both the source and the drain of a 3D PPD-JFET structure simulated in TCAD. Three main regions can be identified:

- A linear region (A) (V_{inj}<$V_{\mathrm{pin}\Delta\Phi}$) where
$$Q_{\mathrm{ch}}(V_{\mathrm{inj}}) \approx \mathrm{EFWC} - \int_0^{V_{\mathrm{inj}}} C_{\mathrm{PPD}} dV_{\mathrm{PPD}}.$$
- An exponential region (B) ($V_{\mathrm{pin}\Delta\Phi}$<$V_{\mathrm{inj}}$<$V_{\mathrm{pin}\Delta\mathrm{Efn}}$) where $Q_{\mathrm{ch}}^{'}$ depends on the thermionic emission of charges from the biasing electrodes toward the PPD channel.
- A full depletion region (C) (V_{inj}>$V_{\mathrm{pin}\Delta\mathrm{Efn}}$) where $Q_{\mathrm{ch}}{}'$ reaches a plateau.

In these TCAD simulations, $V_{\mathrm{pin}\Delta\Phi}$ can be extracted from the linear fit of Q_{ch}, whereas $V_{\mathrm{pin}\Delta\mathrm{E_{fn}}}$ can be extracted by finding the crossing between the Q_{ch} plateau and the fit of the exponential region. Figure 8 shows the results of the TCAD simulation of the SQRT method on the same 3D PPD-JFET structure. By comparing Fig. 7 and Fig. 8, it can be observed that the V_{pin} extracted with the SQRT method provides a good approximation of $V_{\mathrm{pin}\Delta\Phi}$.

As shown in Fig. 9, the in-pixel extraction method also gives an estimation of $V_{\mathrm{pin}\Delta\Phi}$. It can also be observed that, because of the presence of a barrier potential at the PPD/TG interface in the simulated structure, the PPD cannot be completely emptied (E_{fn} saturates at smaller V_{inj} than in the PPD-JFET structure in Fig. 7), leading to an underestimation of $V_{\mathrm{pin}\Delta\mathrm{E_{fn}}}$. This means that $V_{\mathrm{pin}\Delta\mathrm{E_{fn}}}$ can be extracted experimentally from in-pixel measurements (pinning voltage characteristic in Fig. 10) only on the condition that the potential barrier limiting charge transfer is low enough (thus that the exponential region is well visible on the characteristic).

IV. Conclusions

The absolute value of the two pinning voltage definitions which are used in the literature ($V_{\mathrm{pin}\Delta\Phi}$ and

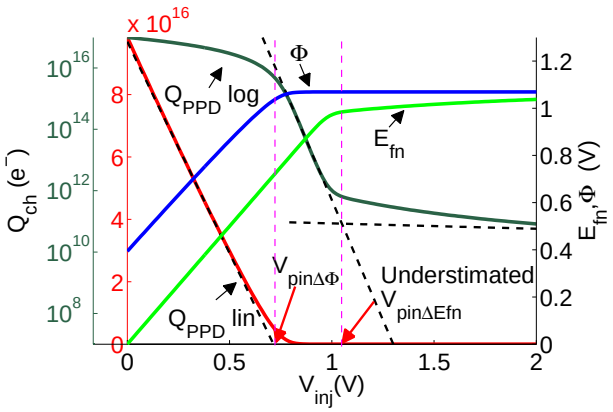

Fig. 9. TCAD simulation of the pinning voltage characteristic (in-pixel pinning voltage extraction method [3]): maximum Φ and E_{fn} (along the cutline A-A' in Fig. 2a) and maximum PPD charge density $Q_{\mathrm{PPD}}^{'}$ (in linear and logarithmic scales), plotted as a function of the biasing potential V_{inj} applied to $\mathrm{VDD_{RST}}$ (TG ON). The transfer phase has not been simulated, thus the pinning voltage characteristic does not show the charge partition regime [4]. The simulated structure is a 3D square $2.5\ \mu m \times 2.5\ \mu m$ PPD with the same doping profiles as the buried channel of the PPD-JFET in Fig. 7. By comparing the curves to Fig. 7 it can be observed that the potential barrier at the PPD-TG interface leads to an underestimation of $V_{\mathrm{pin}\Delta\mathrm{Efn}}$.

$V_{\mathrm{pin}\Delta\mathrm{E_{fn}}}$) can differ of more than 500 mV. Both parameters represent important figures of merit for the characterization of PPD CIS:

- $V_{\mathrm{pin}\Delta\Phi}$ allows to estimate the PPD EFWC as:
$$\mathrm{EFWC} \approx \int_0^{V_{\mathrm{pin}\Delta\Phi}} C_{\mathrm{PPD}} dV_{\mathrm{PPD}}$$
- $V_{\mathrm{pin}\Delta\mathrm{Efn}}$ represents the minimum TG channel potential that must be induced to guarantee an optimal charge transfer (neglecting charge partition).

It has been shown, by means of 3D TCAD simulations, that both in-pixel and JFET-based pinning voltage extraction methods give an estimate of $V_{\mathrm{pin}\Delta\Phi}$. A method to extract $V_{\mathrm{pin}\Delta\mathrm{E_{fn}}}$ from in-pixel measurements has been proposed.

Fig. 11 presents a comparison between experimental pinning voltage measurements: as expected, in-pixel measurements are in good agreement with the SQRT method. The lower in-pixel V_{pin} value extracted at W_{PPD} =

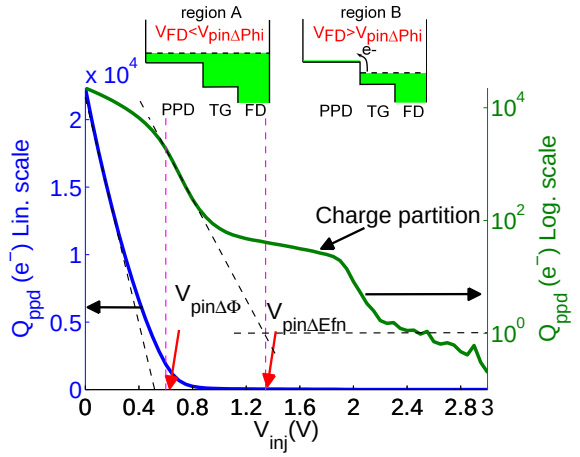

Fig. 10. Experimental in-pixel pinning voltage measurement [3] for a square 2.5 μm × 2.5 μm PPD (averaged over a 64×128 pixel array). With respect to Fig. 9, the experimental pinning voltage characteristic also shows a charge partition regime [4] before reaching the full depletion plateau (this is due to the additional transfer phase required by the experimental measurement). As the logarithmic region is well visible on the pinning voltage characteristic, $V_{\mathrm{pin}\Delta\mathrm{Efn}}$ can be extracted by finding the crossing between the fit of the exponential region and the Q_{PPD} plateau (which has been approximated to $1e^-$). Note that by using the integral method [4] instead of the linear method to fit the pinning voltage characteristic, a better approximation of $V_{\mathrm{pin}\Delta\phi}$ could be obtained.

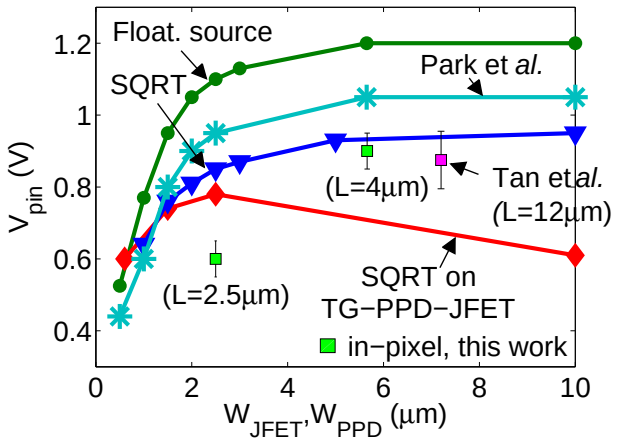

Fig. 11. V_{pin} as a function of the PPD-JFET channel width W_{JFET} (or mimum PPD width W_{PPD}) extracted with the in-pixel method [3], with the floating source method [7] ($I_{\mathrm{leak}} = 1$ pF), with Park's method [6] and with the SQRT method [5]. The channel length of all tested PPD-JFETs is $L_{\mathrm{JFET}} = 20$ μm. For all the tested devices which include a TG, the TG width is equal to the PPD width (or to the TG-PPD-JFET width) and the TG length is 0.7 μm.

2.5 μm can be explained by additional 3D effects [6], [11] (combination of a small W_{PPD} and a small L_{PPD}). It can also be observed that, even if the floating source method and Park's method do not provide an absolute value of the pinning voltage (100 mV-300 mV higher here), they still allow to observe relative pinning voltage variations due to geometrical variations. The figure also shows that if the gain of the JFET is increased (larger $W_{\mathrm{JFET}}/L_{\mathrm{JFET}}$), the SQRT method might not provide meaningful results on TG PPD-JFETs, thus these structures are not recommended for the extraction of V_{pin}.

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