Fully Depleted SOI Pixel Photo Detectors with Backgate Surface Potential Pinning

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Abstract

A novel SOI (Silicon-On-Insulator) pixel photo detector with full depletion and backgate surface potential pinning is proposed in this paper. The detector greatly increases charge-to-voltage conversion gain while stabilizing the operation of SOI circuits. Low noise and wide dynamic range operations are attained. A double doping technique increasing potential barrier to holes at the surface region is effective for a stable operation to the variation of back bias voltage. The structure of the pixel detector and simulation results of potential distributions are described.

1. Introduction

For the scientific imaging, particularly in high energy physics, photo detectors with a fully depleted substrate and on-chip circuitry are required [1][2]. The SOI (Silicon-On-Insulator) pixel detector with a fully-depleted substrate as a photo detector and SOI circuits for in-pixel processing are an ideal solution for such scientific imaging for high energy physics [3][4][5].

In order to improve the sensitivity and stable operation of SOI circuits, this paper proposes a novel SOI pixel detector with potential profile for charge collection backgate surface potential pinning. Event-driven pixel circuits for X-rays imaging at cosmic space are designed as SOI circuits.

2. Backgate potential pinning structure

Fig. 1 shows a conceptual schematic of the proposed SOI pixel detector. A SOI layer is used for CMOS pixel and peripheral circuits. The substrate, which is conventionally a supporting substrate, is used for a fully-depleted photo detector. In order to reduce the back-gate effect to SOI circuits, a BPW (Buried P-Well) is formed underneath the SOI circuits. A charge collector n+ and two different buried n-wells, BNW1 and BNW2 are formed in the n-type high-resistivity substrate. p+ layer is formed at the backside

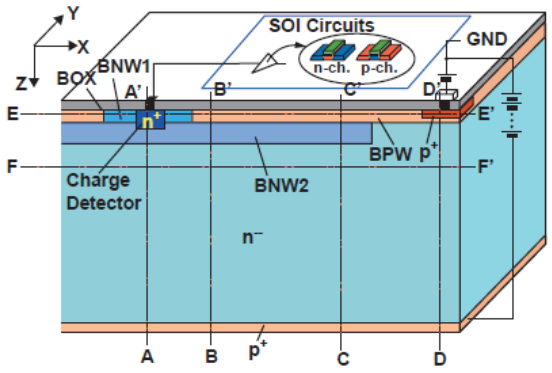

Fig.1. Proposed detector

of the substrate with a back-end process steps. The charge collector is electrically connected to the upper SOI circuits through a via-hole and plug-metal formed in the buried oxide (BOX). Thanks to the pinned surface potential of the backgate (BPW), the SOI CMOS circuits are isolated from the photo detector in the substrate and the operation is stabilized. The BPW also acts as a pinning layer to reduce the dark current. The fast charge correction inside the pixel is done by a depleted potential profile created in the substrate. The BNW2 plays an important role for creating lateral electric field for high-speed charge correction and increasing a potential barrier to holes in the BPW. This allows us to use this detector under a fully depleted condition by applying negative voltage to the backside p+ region while preventing the punch-through to the

back-gate (BPW) and injection of holes from the BPW. Since the BNW1 and BNW2 are fully depleted and the capacitance of the charge collector is only due to the n+/BPW junction, high charge-to-voltage conversion gain is realized. The SOI circuits are used for event-driven measurement of X-ray energy spectrum.

3. Event-driven pixel circuits

In cosmic space, the population of the target X-ray event is low. To achieve a long-term efficient observation, event-driven circuits are useful for the X-ray coming [6].

Fig. 2 shows the pixel circuits. It consists of a comparator for event detection, charge amplifier for photon energy measurement, and in-pixel CDS (correlated double sampling) circuits for cancelling kTC noise. Each pixel has own event-driven circuits and works independently in parallel. Indeed the detector with the SOI circuits has high energy resolution with low power consumption.

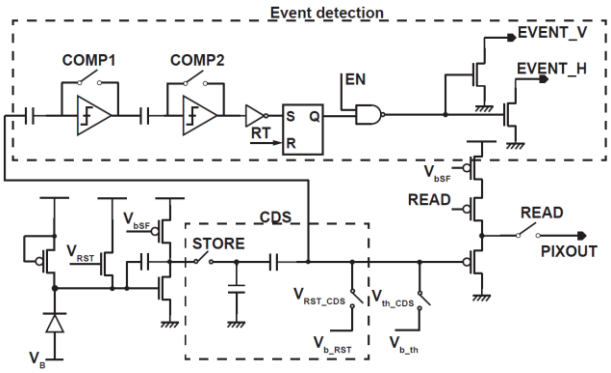

Fig. 2. Event-driven pixel circuits

4. Potential profile simulation of the SOI pixel detector

Fig. 3 shows the simulated potentials of the SOI pixel detector. The pixel size of the detector is 40μm×40μm, and thickness of sensor-layer (n—substrate) is 200μm. The voltages at the charge detector, the back-gate (BPW), and the substrate backside p+ (Vback) are set to be -2V, 3V and -120V, respectively.

Fig. 3(a) shows potential distribution of vertical cross-sections of A-A', B-B', C-C' and D-D' of Fig.1. The entire sensor layer is fully depleted from the backside to the surface.

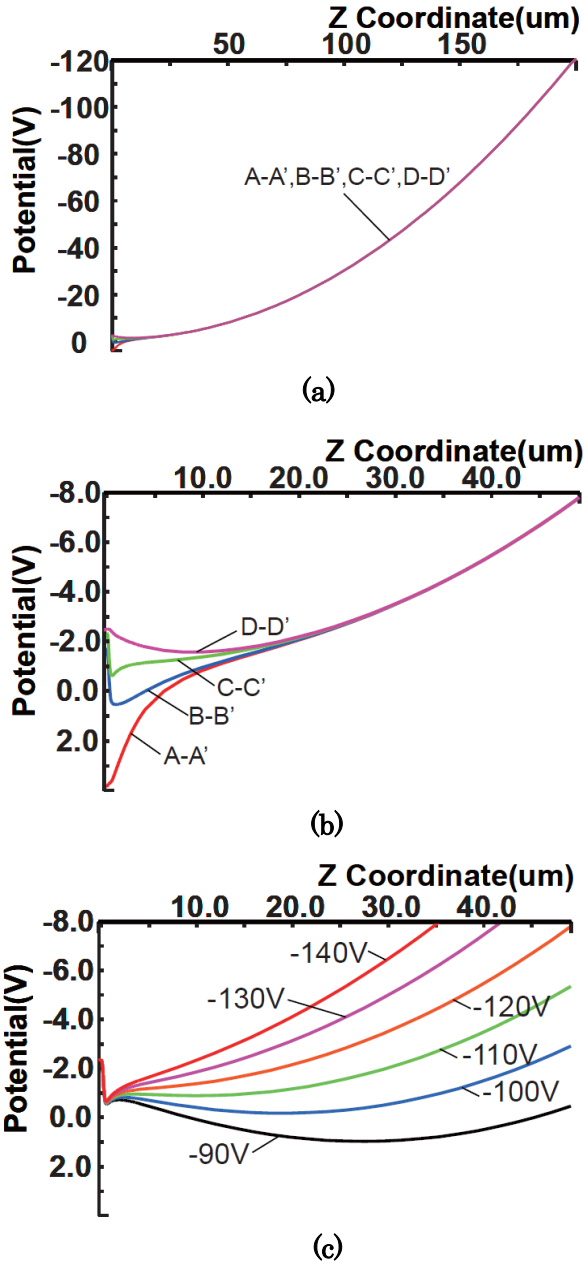

Fig. 3. Maximum potential distributions to depth (a) vertical cross-section [0-200μm], (b) enlarged at the vicinity of the surface [0-50μm], (c) varied Vback voltage along with C-C'.

Fig. 3(b) is a zoomed potential distribution from the depth of 50μm to the surface. In the cross-sections of B-B', C-C' and D-D', the back-gate surface is pinned to the supply voltage of the BPW(-2V), while creating a potential distribution and resulting vertical and lateral electric fields to accelerate photo-electrons to the n+ charge collector. As shown in Fig. 3(c) which is potential distributions of C-C', the BNW2 creates a large potential barrier to holes in

the BPW and is almost unchanged for the variation of the backside junction voltage. The punch-through is prevented even if an excess bias voltage (-130V to -140V) is applied. As shown in Fig. 4 which is a horizontal maximum potential distribution at the cross-section of E-E' and F-F' in Fig. 1, the back-gate (BPW) is pinned to -2.4V and lateral electric field to collect photo-electrons in the pixel to the charge collector is created. Fig. 5 is a 2-D plot of the potential distribution near surface (Z=0 to 30 μm).

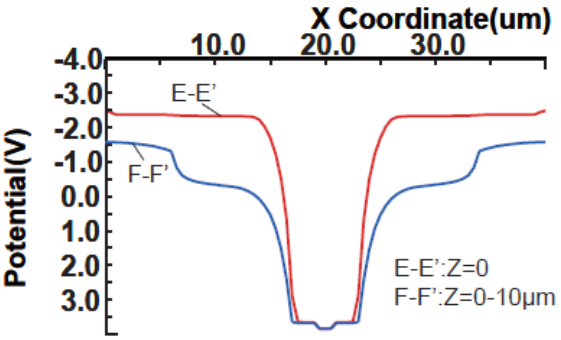

Fig. 4. Maximum potential distributions of horizontal cross-section

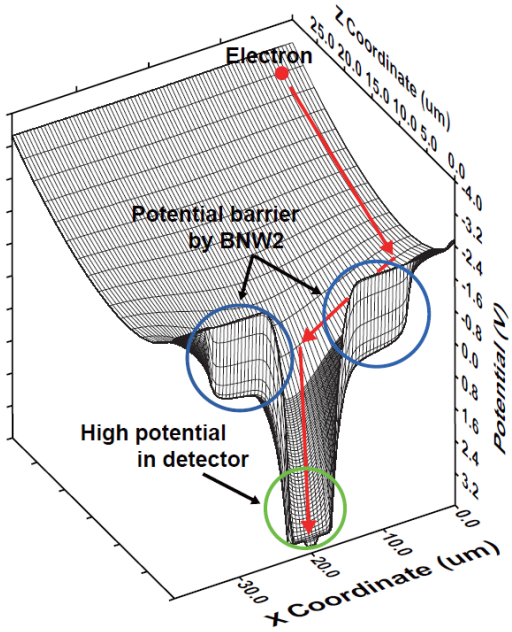

Fig. 5. Electron path on surface potential profile

An experimental chip (Fig. 6) to demonstrate the novel SOI pixel detector is being manufactured. To verify the high-conversion gain and high quantum efficiency, several test pixel are implemented in this chip. Also, 8×8 pixels event-driven circuits are included.

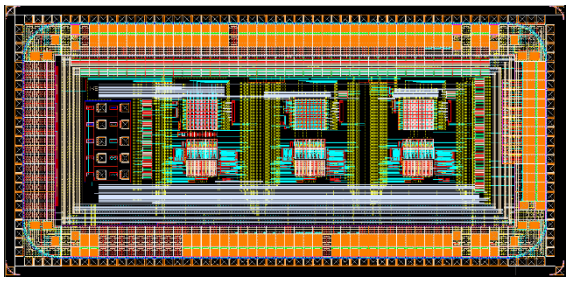

Fig. 6. Implemented chip layout

5. Conclution

In this paper, a X-ray photon detector with charge collection and surface potential pinning structure based on SOI technology has been presented. The SOI pixel detector realizes high charge-to-voltage conversion gain and high quantum efficiency based on event-driven detection. X-ray energy distribution imaging is feasible with high SNR by integrated event-driven circuits in the proposed detector.

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