

# A 80% QE High Readout Speed 1024 Pixel Linear Photodiode Array for UV-VIS-NIR Spectroscopy

Rihito Kuroda<sup>a</sup>, Takahiro Akutsu<sup>a</sup>, Yasumasa Koda<sup>a</sup>, Kenji Takubo<sup>b</sup>, Hideki Tominaga<sup>b</sup>,  
Ryuuta Hirose<sup>b</sup>, Tomohiro Karasawa<sup>b</sup> and Shigetoshi Sugawa<sup>a</sup>

<sup>a</sup> Graduate School of Engineering, Tohoku University, <sup>b</sup> Shimadzu Corporation  
6-6-11-811, Aza-Aoba, Aramaki, Aoba-ku, Sendai, Miyagi, Japan 980-8579  
TEL: +81-22-795-4833, FAX: +81-22-795-4834, Email address: rihito.kuroda.e3@tohoku.ac.jp

## ABSTRACT

A high QE and high readout speed linear photodiode array (PDA) with high transmittance optical layers for multiply divided pixel regions and multiple transfer gates along the long side of PD was developed in this work for UV-VIS-NIR spectroscopy. The fabricated 1024 pixel PDA with the pixel size of  $25 \mu\text{m}^{\text{H}} \times 2500 \mu\text{m}^{\text{V}}$  exhibited an average QE of 70% for 200-800 nm and 80% for 200-320 nm wavebands, FWC of over 70 pC and a line scan period of 0.33 msec simultaneously.

## INTRODUCTION

Spectrometers are widely used in the various fields of scientific analyses, life science, environmental assessment, food inspection and so on [1-2]. High sensitivity through UV-VIS-NIR light waveband is strongly required for PDA used in spectrometers to analyze various measurement samples accurately. In addition, a high readout speed performance is beneficial to shorten the measurement time. Fig.1 (a) shows the schematic image of a spectrometry system with a grating and a PDA as spectral light detector. In general, spectral light is irradiated to the pre-designated positions of the PDA. A high sensitivity is to be achieved for a wide light waveband if each PD region contains a high transmittance optical layer corresponding to the receiving light waveband as illustrated in Fig.1 (b). This concept has been proposed recently [3]. In this work, we demonstrate a 1024 pixel

PDA for UV-VIS-NIR spectroscopy with high transmittance optical layers for multiply divided pixel regions for a high QE for UV-VIS-NIR waveband and multiple transfer gates along the long side of each PD for a high readout speed from a large pixel PD. In addition, a high concentration Si surface  $\text{p}^+$  layer with steep dopant concentration profile was introduced to improve Si incident light sensitivity and stability to UV-light irradiation [4-5].

## PDA DESIGN AND FABRICATION PROCESS TECHNOLOGY

Fig.2 shows the circuit block diagram of the developed PDA. The pixel size is  $25 \mu\text{m}^{\text{H}} \times 2500 \mu\text{m}^{\text{V}}$ . This large PD height is beneficial to account for various types of spectrometers' optical configurations as well as to improve the FWC. Here a high FWC is advantageous for improving photon shot noise limited SNR for absorption spectrometers. The signal readout speed limited by the RC delay of PD is to be improved by placing multiple numbers of transfer gates along the long side of each PD [6]. Fig.3 shows the cross sectional viewgraph of a PD with high transmittance optical layer. In the developed PDA, pixel region was divided into seven regions having a band pass filter type optical layer each with high transmittance toward corresponding receiving light waveband. Fig.4 shows the chip fabrication process flow and table 1 shows the detailed structure of optical layers.

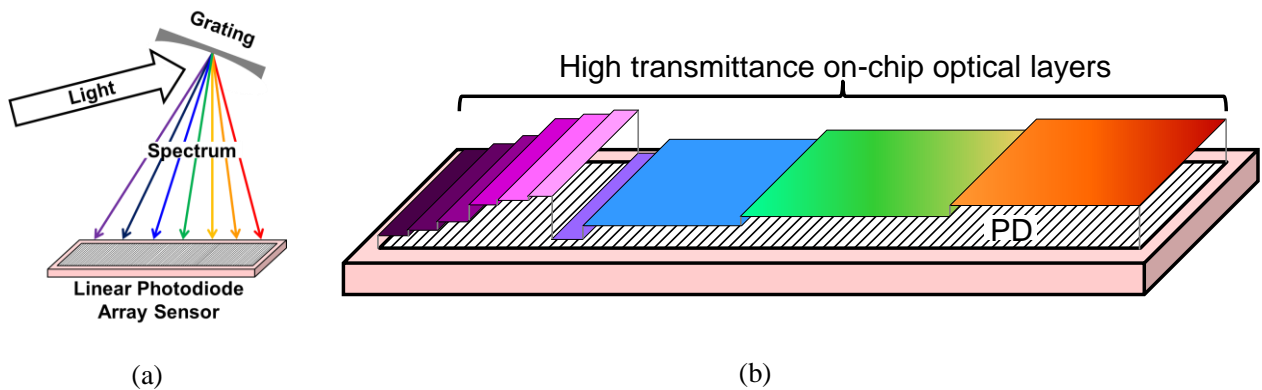


Fig. 1. (a) Schematic image of the typical detector of a spectrometer using PDA and (b) conceptual illustration of the proposed PDA structure with optimum optical layers for multiply divided pixel regions.

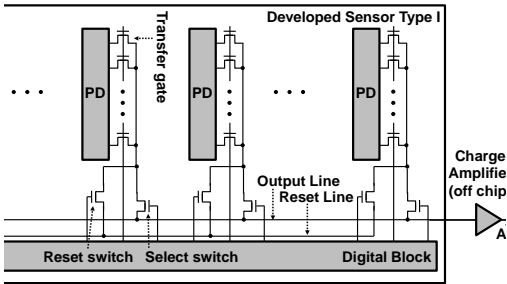


Fig. 2. Circuit block diagram of the developed PDA. The pixel size is  $25\mu\text{m}^{\text{H}} \times 2500\mu\text{m}^{\text{V}}$ . Multiple numbers of transfer gates are placed along the long side of PD.

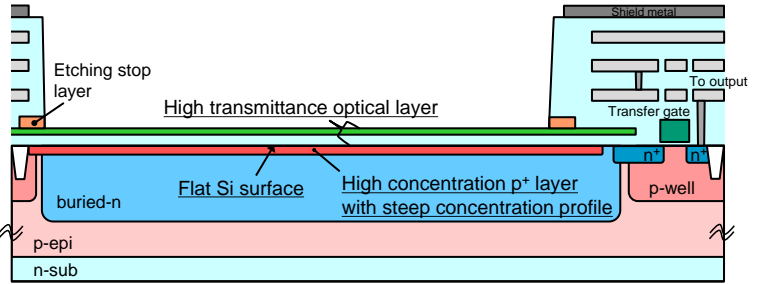


Fig. 3. Cross sectional viewgraph of a PD with high transmittance optical layer. The surface pn junction technology enabling high sensitivity and high stability to UV-light was also introduced [4-5].

p-epi/n-sub wafer

- CIS front-end-of-line process featuring surface high concentration p<sup>+</sup> layer with steep dopant concentration profile [4-5]
- Formation of multiple optical layers; seven types of stack structures of SiO<sub>2</sub> and small extinction coefficient SiN<sub>x</sub>
  - \* Thickness variation tolerant stack structure design.
  - \* In-line thickness monitoring for fine process control.
- Etching stopper layer formation
- Back-end-of-line process; M3 process with shield metal
- Inter-metal dielectric removal on PD region
- Etching stopper layer removal

Fig. 4. Chip fabrication process flow.

Here, for the fabrication of on-chip high transmittance multiple optical layers, several design and fabrication strategies were employed as summarized below. For materials of the optical layers above PDs, high integrity SiO<sub>2</sub> and small extinction coefficient SiN<sub>x</sub> were used. This is beneficial to maintain the process simplicity and long term reliability of the optical layers. The small extinction coefficient SiN<sub>x</sub> film which is transparent to UV light waveband down to at least 200 nm was formed by plasma CVD process with optimized mixed gas flow rate and deposition pressure. Also, the thickness of the top surface layers of all the regions were designed to be the same. This enables to apply the same film for all of the regions resulting in a reduction of process-induced thickness variation. In addition, SiO<sub>2</sub>/Si interface was applied for all the types to maintain the high quality interface. This is beneficial to reduce an increment of fixed charges due to UV light exposure stress, resulting in an improvement of performance stability for a long time use of the PDAs. Moreover, regarding the fabrication process, the optical layer thickness was tuned carefully using the in-line layer thickness monitoring results during the film

Table 1  
Detail of the high transmittance optical layers formed on PD.

Optical layer type		1	2	3	4	5	6	7	1	3
		Two layers			Four layers				Two layers	
Layer and thickness[nm] (0th-layer: Si)	4th SiN <sub>x</sub>	-	-	-	20	20	20	-	-	-
	3rd SiO <sub>2</sub>	-	-	-	68	80	95	-	-	-
	2nd SiN <sub>x</sub>	20	20	20	10	10	10	20	20	20
	1st SiO <sub>2</sub>	56	66	76	7	7	7	20	56	76
Receiving light waveband [nm]		200-209	210-223	224-244	245-267	268-286	287-316	317-443	444-628	629-1100
Pixel number		1023-977	976-954	953-919	918-881	880-850	849-801	800-595	594-298	297-0

etching process. These high transmittance optical layers were formed before metallization process. After the shield metal formation process, inter-metal dielectric film was removed on the PD regions by an etching process. In order to stop this dielectric film etching above the optical layers, an etching stopper layer was formed prior to the metallization process. Finally, the etching stopper layer was removed. Fig.5 shows the micrograph of the fabricated PDA chip. The chip fabrication technology was based on a 0.18 μm 1P3M CMOS process with buried partially depleted PD, and the above mentioned optical layer formation technology was integrated into the process flow.

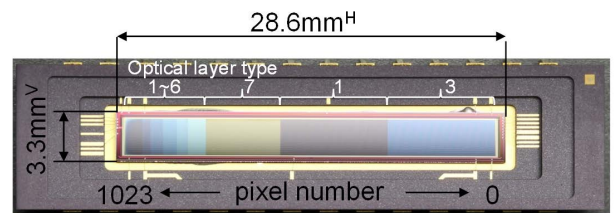


Fig. 5. Micrograph of the fabricated PDA chip with high transmittance optical layers for multiply divided pixel regions.

## FABRICATED PDA CHIP PERFORMANCE

Fig.6 shows the photoelectric conversion characteristic of the fabricated PDA. A good linearity and a high FWC of 73 pC sufficient for absorption spectrometers were successfully obtained due to the large PD size with the buried partially PD structure. Fig.7 (a-b) shows the measured QE as a function of wavelength of the developed PDA and a reference sample with 3.8  $\mu\text{m}$ -thick  $\text{SiO}_2$  above PD. For the developed PDA, the high QE performance was successfully obtained, i.e., the average and the minimum QEs ( $QE_{\text{average}}$  and  $QE_{\text{minimum}}$ ) were 70 % and 50 % for 200-800 nm waveband and 80% and 70 % for 200-320 nm waveband, respectively. In addition, the beat of QE curve due to the optical interference appeared for the reference sample was significantly reduced in the developed PDA. It is to be beneficial to improve spectral sensitivity variation due to the fluctuation of optical system of spectrometers. Fig.8 (a) shows the pixel driving pulse and (b-c) show the PD photo charge readout efficiency as a function of transfer gate on time. Over 100 times faster readout speed was achieved for the developed PDA in comparison to the conventional structure with single transfer gate on the short side of PD. Fig.9 shows the stability of QE and dark current toward the deuterium lamp irradiation having the peak light intensity at around 204 nm. The irradiation time of 200 h with the employed lamp is sufficiently long for the evaluation of performance stability for general spectrometers. Due to the employed PD junction technology, high stability of both QE and dark current were achieved. Tale 2 summarizes the developed PDA chip design specifications and measured performances. The superior performances of the developed PDA chip were successfully confirmed.

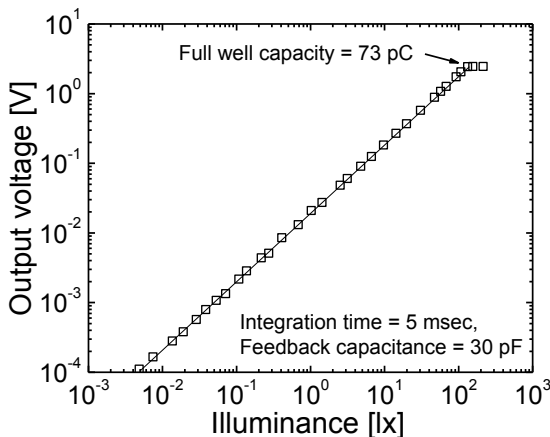


Fig. 6. Photoelectric conversion characteristic of the fabricated PDA. The FWC was 73 pC/pixel.

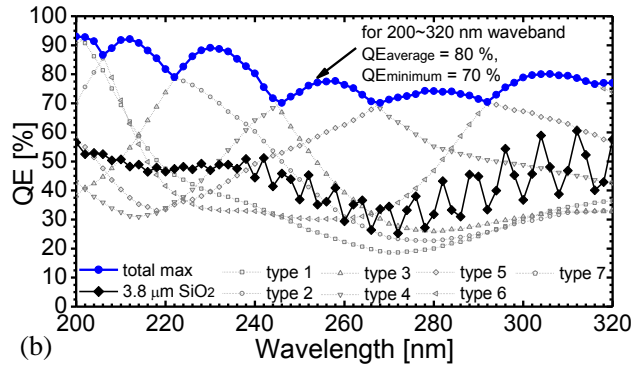
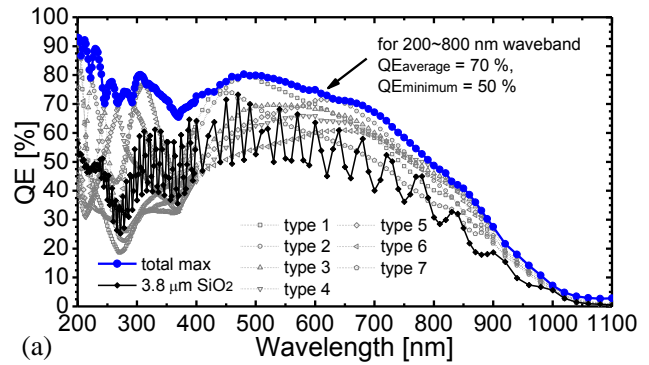


Fig. 7. Measured QE as a function of wavelength of the developed PDA and a reference for (a) 200-1100 nm UV-VIS-NIR waveband and (b) 200-320 nm UV waveband.

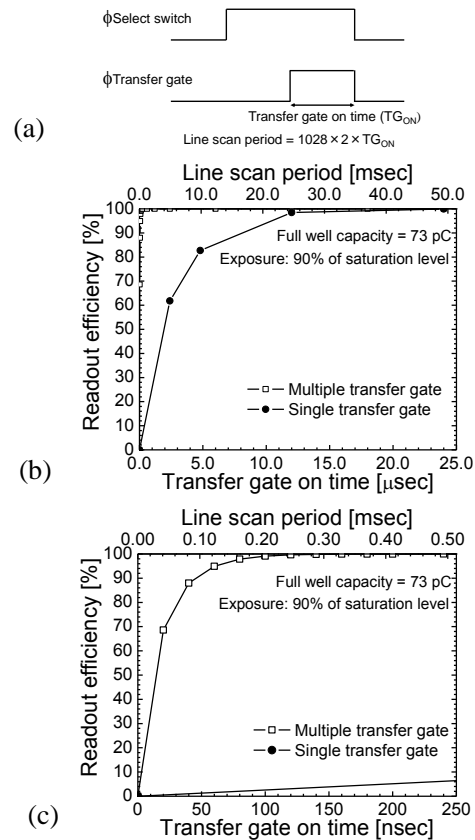


Fig. 8. (a) Diagram of pixel driving pulse, (b) and (c) PD photo charge readout efficiency as a function of transfer gate time for the developed PDA with multiple transfer gates along the long side of PD and the reference PDA, where (c) is the enlarged view of (b).

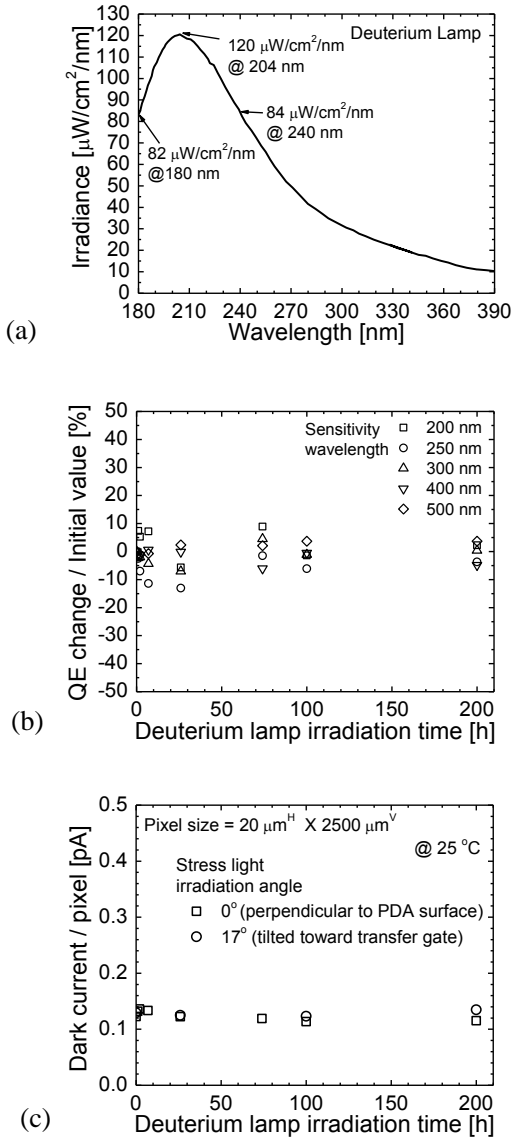


Fig. 9. (a) Spectral irradiance of the deuterium lamp employed for stability evaluation. (b) change of QE for various wavelength normalized by the initial values and (c) dark current as functions of deuterium lamp irradiation time, respectively.

## CONCLUSION

A high QE and high readout speed 1024 pixel PDA with high transmittance optical layers for multiply divided pixel regions and multiple transfer gates along the long side of PD was designed, fabricated and evaluated. The very high average QE of 70% for 200-800 nm and 80% for 200-320 nm wavebands were successfully obtained. Also, a high FWC of over 70 pC and a high line scan period of 0.33 msec as well as a high stability of sensitivity and dark current toward strong UV light irradiation were achieved simultaneously. The developed PDA is promising for performance improvement of UV-VIS-NIR spectrometers.

## REFERENCES

- [1] R. J. Robbins, S. R. Bean, "Development of a quantitative high-performance liquid chromatography-photodiode array detection measurement system for phenolic acids," *J. Chromatography A*, Vol.1038, pp.97-105, 2004.
- [2] X. Hou, B. T. Jones, R. A. Meyers, "Inductively Coupled Plasma/Optical Emission Spectrometry," *Encyclopedia of Analytical Chem.*, John Wiley & Sons Ltd, Chichester, pp.9468-9485, 2000.
- [3] Y. Koda, R. Kuroda and S. Sugawa, "High quantum efficiency 200-1000 nm spectral response photodiodes with on-chip multiple high transmittance optical layers," in *Proc. IEEE Sensors 2014*, pp.1664-1667, 2014.
- [4] T. Nakazawa, R. Kuroda, Y. Koda and S. Sugawa, "Photodiode dopant structure with atomically flat Si surface for high sensitivity to UV-light," *IS&T/SPIE EI*, Vol.8298, pp.82980M-1-8, 2012.
- [5] R. Kuroda S. Kawada, S. Nasuno, T. Nakazawa, Y. Koda, K. Hanzawa and S. Sugawa, "A Highly Ultraviolet Light Sensitive and Highly Robust Image Sensor Technology Based on Flattened Si Surface," *ITE Trans. MTA*, Vol.2, pp.123-130, 2014.
- [6] T. Akutsu, S. Kawada, Y. Koda, T. Nakazawa, R. Kuroda and S. Sugawa, "A 1024×1 Linear Photodiode Array with Fast Readout Speed Flexible Pixel-level Integration Time and High Stability to UV Light Exposure," *IS&T/SPIE EI*, Vol.9022, pp.90220L-1-8, 2014.

Table 2  
Design specifications (left) and performance summary (right).

Process technology	0.18 $\mu\text{m}$ 1P3M CMOS with buried partially depleted PD	Spectral sensitivity range	200~1000 nm
Supply voltage	3.3V	QE <sub>average</sub> and QE <sub>minimum</sub>	70% and 50% for 200~800 nm 80% and 70% for 200~320 nm
Die size	28.6 mm <sup>H</sup> × 3.3 mm <sup>V</sup>	Full well capacity	73 pC
Pixel size	25 $\mu\text{m}^{\text{H}}$ × 2500 $\mu\text{m}^{\text{V}}$	Minimum transfer gate on time (lag < 0.1%)	160 nsec (line scan period: 0.33 msec)
Number of pixels	Total	1028	Dark current
	Effective	1024	