Electrical Characterization Method for Two Stage Transfer Global Shutter Pixels

Manuel Innocent
ON Semiconductor, Schaliënhoevedreef 20B, 2800 Mechelen, Belgium.
Manuel.Innocent@onsemi.com, tel +32 15 446 390, fax +32 15 448 780

During a pixel development there is a need to extract basic electrical pixel performance parameters in a reliable and convenient way. Therefore a method has been developed based on electrical injection and read back to measure data such as Vpin, image lag, capacitance and equilibrium full well charge on real pixels in the array. Pixels provide more statistical information and more similar conditions to the final application than typical electrical test structures. As this method does not rely on optical stimulation, it is very suited to be implemented on a prober, where usually there is no high quality, full featured, light source available. Once the required functionality is supported by the test chip frame, this method may earn a fixed place a pixel developer's toolkit.

Motivation

During the development of charge domain global shutter pixels (two stage charge transfer pixels) [4,5,6,7], there is a need to extract basic electrical performance parameters in a reliable and convenient way. This type of pixels has too many degrees of freedom to treat it as a black box. It is hard to deduce all information from optical measurements since these only show an input-output relation without intermediate observable points. Typically, the optical measurements are complemented with data from measurements on E-test structures. Unfortunately, E-test structures do not have the exact same environment and operating conditions as the real pixel and these also lack the statistical information which can be gathered from measurements on a real pixel array.

Therefore a set of electrical measurements has been developed that allows extracting C-V curves, Vpin [1,3], equilibrium FWC [2] and image lag in a fast and reliable way and that produces results with an absolute voltage reference. These measurements have shown to be very helpful in optimizing the technology for a two stage charge transfer pixel. Clearly, these measurements do not provide any information on the optical performance of the pixel.

Structural Requirements

The structure targeted for these measurements is a charge domain global shutter pixel with photo diode reset and two stage charge transfer readout (Figure 1). The sensor frame needs to support a pixel supply which is controlled by pixel timing and is switchable between two programmable levels. Typically this type of functionality is only available in a test chip frame although it may also be used for hard-soft reset operations. Additional functionality, such as programmable low and high levels for the control signals, allows getting additional information such as transfer gate Vt and memory node full well charge as a function of gate potential.

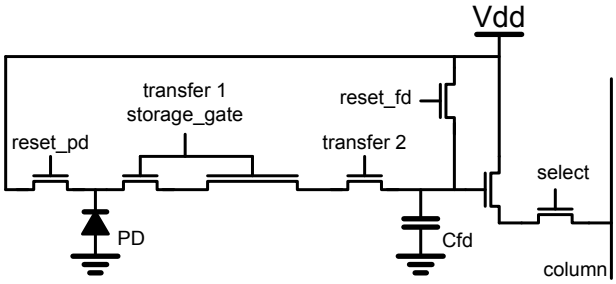

Figure 1: Schematic of a charge domain global shutter pixel with photo diode reset and two stage charge transfer readout.

Measurement Approach

The measurements are based on injecting a voltage in the pixel, followed by the read out of the sensor output in the regular way. Voltage injection can either be done directly through e.g. an ohmic contact to the photo diode or it can be done by lowering the pixel supply voltage to the intended injection voltage and connecting either to the photo diode or the memory node. Photo diode injection is typically performed through the photo diode reset transistor, while memory node injection is typically through the floating diffusion reset and the transfer 2 transistors. After the injection phase the pixel supply is brought back to its nominal value and the pixel is read out. Conceptual timing diagrams for these operations are provided in figures 10, 11 and 12 on the last page of this paper.

The measurements on the next pages are classified in three categories: Vpin measurements, electrical lag measurements and electrical response measurements with a parametric sweep. In the examples shown all lag measurements are based on photo diode injection and the response measurements with parametric sweep are based on memory node injection. This is just an illustrative set of examples. It does not intend to be exhaustive or represent the current state of the technology development. Additionally, the description of the method in this paper assumes a pixel configuration with transfer 1 and the storage gate controlled by the same control signal. Alternatively, the storage gate can have a separate control signal to further increase timing flexibility or in case of a storage diode pixel, the memory node may not have a control signal.

Vpin Measurement

The Vpin measurement on the array can be done with the inject-and-read-back method [1] or with a dedicated pixel structure with a DC connection to the photo diode [3]. Figure 12 at the end of the paper shows the timing diagram for the inject-and-read-back measurement while figure 2 shows the schematic of the dedicated pixel with a DC connection. On large pixels both measurement will give the same result. However on small pixels, the dedicated pixel may result in a higher reported Vpin as the part of the diode where the connection is, is by definition not pinned. Edge effects from this region may make it harder to deplete the photo diode. Figure 3 shows a measurement of this structure with regular CDS readout timing. When the injection voltage is above the Vpin level, there is a dark level readout and when the injection voltage is below the Vpin level, the readout goes to full scale. This results in a sharp transition from which the photo diode Vpin level can be extracted.

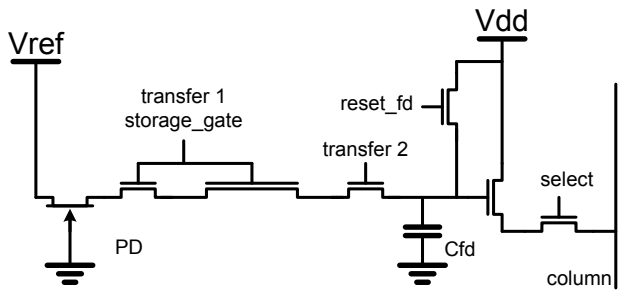

Figure 2: Schematic of the dedicated Vpin measurement pixel with a DC connection to the photo diode. The photo diode is to be considered as a JFET.

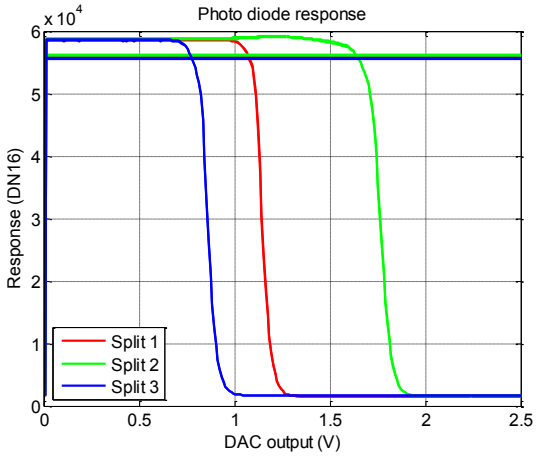

Figure 3: *Response as function of applied DC voltage for the dedicated Vpin test pixels in three different process splits. The reported Vpin is the voltage at which the average response crosses 95% of its final value*

Electical Lag Measurement

The electrical lag measurement is a measurement where a voltage is injected and in addition to the first (response) image also the second and third images are read out without memory node reset in between the samples. In the examples shown here, the injection is done at the photo diode (timing shown in figure 10) and the result is representative for the entire lag of the pixel. Similarly, the injection can also be done at the memory node (timing shown in figure 11) in order to measure the transfer 2 lag separately. The examples shown in figures 4, 5 and 6 originate from two pixels with much more charge storage capacity in the photo diode than in the memory node. From the pixel represented in figure 4 and figure 5 all charge can be read in 3 read operations. Adding the 3 reads together yields a linear curve. The onset of charge injection from the photo diode reset and the image lag are clearly visible in the zoom of the low signal levels shown in figure 5. The pixel represented in figure 6 has a higher memory node full well charge, but some signal is lost in the readout and the total response of the three reads has a (non-linear) S shape.

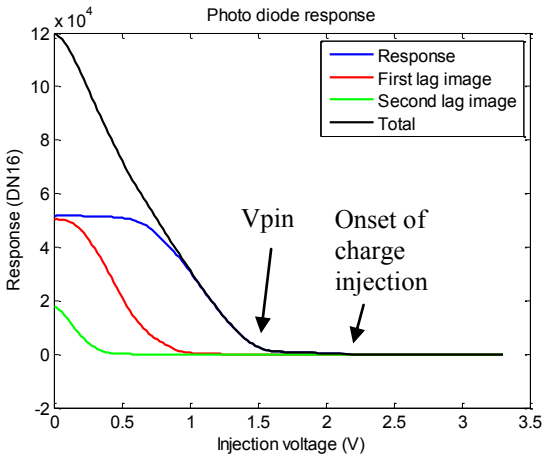

Figure 4: Response, first lag response and second lag response as a function of photo diode injection voltage. The graph shows data from a pixel that can store much more charge in the photo diode than in the memory node. All electrons from the photo diode are read out in 3 reads. Below 1.2 V, the photo diode and the memory node are in charge sharing during the first transfer 1 and the residual charge is read as the first lag image. Similarly for the second lag image around 0.6 V. The black curve shows the sum of the 3 reads. The smaller response in the region between 1.5 V and 2.3 V is believed to represent charge injection from the photo diode reset transistor.

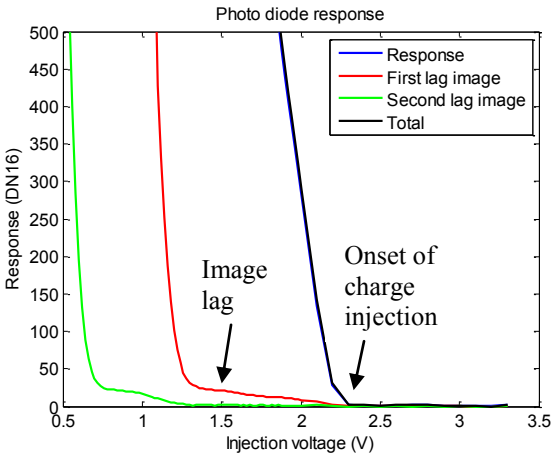

Figure 5: Response, first lag response and second lag response as a function of photo diode injection voltage. The graph shows a zoom of figure 4. The small response on the first lag image (right of the knee point) is representative for the image lag.

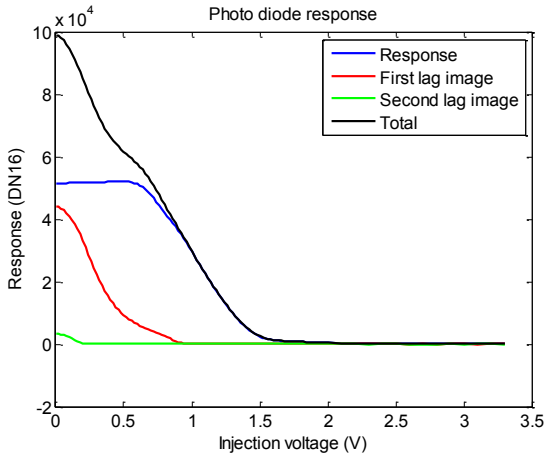

Figure 6: Response, first lag response and second lag response as a function of photo diode injection voltage. When the response exceeds 40000 DN the first lag image contains the residual response. However, some signal is lost which results in the S-shape on the total response (black curve) around 60000 DN. The signal loss is either due to saturation of the readout or charge loss due to transfer 2 punch through (or a combination). There are two distinct slopes on the first lag image (red curve) where the slope between 0 V and 0.5 V is believed to represent the residual charge in the photo diode while the slope between 0.5 V and 1.0 V is believed to represent charge sharing between the memory node and the floating diffusion.

Parametric Sweeps

As examples of parametric sweeps this section shows two voltage sweeps and one design rule sweep. Figure 7 shows the memory node response for different transfer 1 / storage gate low voltages. In the configuration used with a shared control signal for the two gates, the storage gate voltage sets the effective Vpin of the storage gate in the hold phase. However, it also sets the transfer 1 low level and hence sets the level at which spill back from the memory node to the photo diode will occur. Figure 8 shows the memory node response for different transfer 2 high voltages. Generally a higher transfer 2 voltage improves the transfer speed, but as it also moves up the onset of charge injection it effectively limits the available linear swing on the floating diffusion. Finally, figure 9 shows the memory node response for different transfer 2 gate lengths. For shorter gate lengths the memory node full well charge is limited by transfer 2 leakage.

The response curves of both photo diode and memory node end at their respective equilibrium full well charges [2] at an injection voltage of 0 V. To acquire a more complete view, the injection voltage sweep can be extended to negative injection voltages. With negative injection voltages there will typically be signal loss over time approaching the equilibrium full well charge from the high side. This decay over time can also be measured conveniently by varying the time between injection and readout.

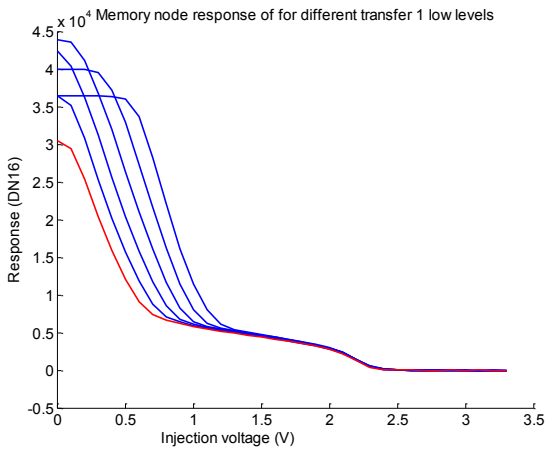

Figure 7: Response as a function of memory node injection voltage with transfer 1 low voltage as a parameter. The transfer 1 low voltage varies from 0.0 V to 1.0 V in steps of 0.2 V. The red curve is for the nominal value of 0.0 V.

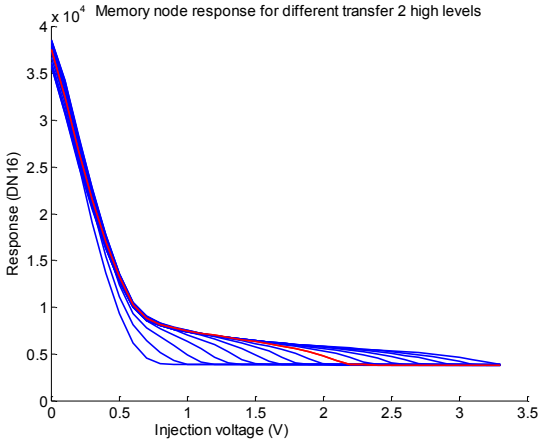

Figure 8: Response as a function of memory node injection voltage with transfer 2 high voltage as a parameter. The transfer 2 high voltage varies from 1.6 V to 4.4 V in steps of 0.2 V. The red curve is for 3.2 V, which is close to the nominal value of 3.3 V. The voltage of the onset of charge injection into the memory node scales linear with the transfer 2 high level.

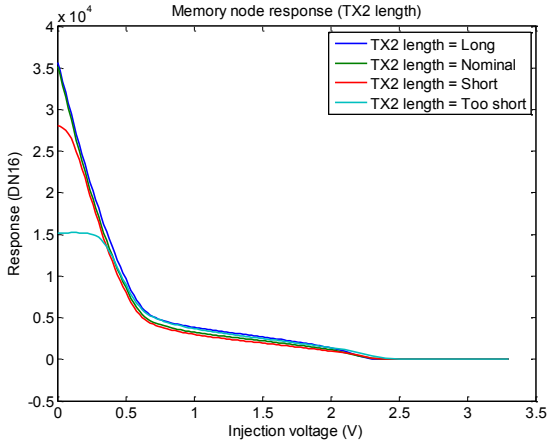

Figure 9: Response as a function of memory node injection voltage with transfer 2 length as a parameter. For shorter transfer 2 lengths the output swing is reduced.

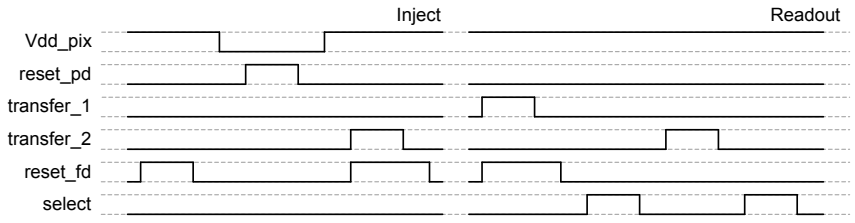

Figure 10: Timing diagram for photo diode injection through the photo diode reset transistor. The injection phase forces a lowered vdd_pix to the photo diode through reset_pd. The readout phase reads the pixel with nominal vdd_pix and a CDS read with two consecutive transfers.

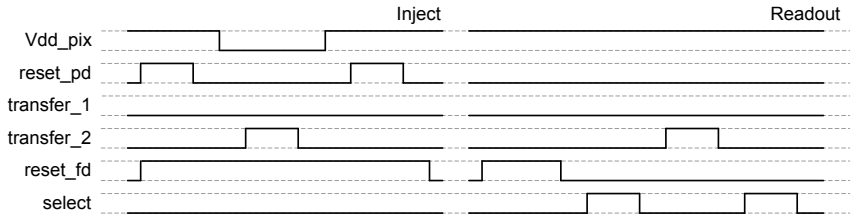

Figure 11: Timing diagram for memory node injection through the floating diffusion. The injection phase forces a lowered vdd_pix to the memory node through reset_fd and transfer_2. The readout phase reads the pixel with nominal vdd_pix and a normal CDS read from the memory node.

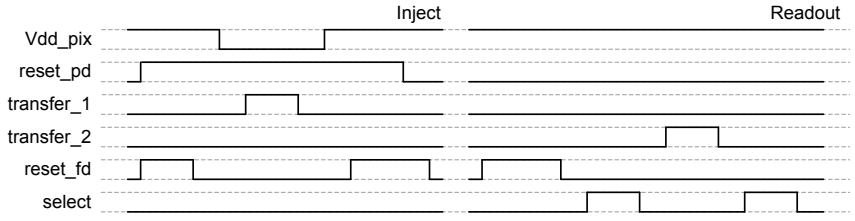

Figure 12: Timing diagram for memory node injection through the photo diode. The injection phase forces a lowered vdd_pix to the memory node through the photo diode reset and the photo diode. This can only happen when the injection voltage is below the photo diode Vpin. The readout phase reads the pixel with nominal vdd_pix and a normal CDS read from the memory node.

Conclusion

This paper presents an electrical pixel characterization method. This method allows the extraction of basic electrical performance parameters such as Vpin, image lag and equilibrium full well charge in a reliable and convenient way and with an absolute voltage reference. As this method does not require an optical setup, it is very well suited to be implemented on a wafer prober.

The method can be applied on 4T and 5T pixels, but the real benefit is truly shown in case of two stage transfer global shutter pixels. These pixels have intermediate nodes that are poorly observable in typical optical measurements. The additional insights gained from the presented measurements have been well appreciated during the development of this global shutter pixel. This method has earned its place in the author's pixel development toolbox.

Acknowledgement

The measurements presented in this paper are performed on test chips processed by TowerJazz in the framework of a two stage transfer global shutter pixel development.

References

[1] V. Goiffon, J. Michelot, P. Magnan, M. Estribeau, O. Marcelot, P. Cervantes, A. Pelamatti and Ph. Martin-Gonthier, "On The Pixel Level Estimation of Pinning Voltage, Pinned Photodiode Capacitance and Transfer Gate Channel Potential" in Proc. IISW, 2013.

[2] A. Pelamatti, V. Goiffon, M. Estribeau, P. Cervantes and P. Magnan, "Estimation and Modeling of the Full Well Capacity in Pinned Photodiode CMOS Image Sensors," IEEE Electron Device Letters, vol. 34, pp. 900-902, 2013.

[3] M. Innocent, "A Radiation Tolerant 4T pixel for Space Applications: Layout and Process Optimization," in Proc. IISW 2013.

[4] A. Lahav, J. Crooks, B. Marsh, R. Turchetta and A. Fenigstein, "CMOS Image Sensor Pixel with 2D CCD Memory Bank for Ultra High Speed Imaging with Large Pixel Count" in Proc. IISW2013.

[5] H.J.Yoon, S.Itoh, and S.Kawahito, "A CMOS Image Sensor With In-Pixel Two-Stage Charge Transfer for Fluorescence Lifetime Imaging", IEEE Trans. ED, Vol.56, No.2, pp.214-221, Feb. 2009.

[6] S. Velichko, G. Agranov, J. Hynecek, S. Johnson, H. Komori, J. Bai, I. Karasev, R. Mauritzson, X. Yi, V. Lenchenkov, S. Zhao, H. Kim, "Low Noise High Efficiency 3.75 µm and 2.8 µm Global Shutter CMOS Pixel Arrays," in Proc. IISW 2013.

[7] J. Solhusvik, S. Velichko, T. Willassen, S. Yaghmai, J. Olsson, A. Rosnes, T. Martinussen, P. O. Pahr, S. Eikedal, S. Shaw, R. Bhamra, D. Pates, S. Smith, L. Jiang, D. Wing , J. Bai, S. Nagaraja and A. Chilumula, "A 1.2MP 1/3" Global Shutter CMOS Image Sensor with Pixel-Wise Automatic Gain Selection," in Proc. IISW 2011.