Analysis and Reduction of Floating Diffusion Capacitance Components of CMOS Image Sensor for Photon-Countable Sensitivity

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ABSTRACT

In this paper, we describe an analysis methodology of components of floating diffusion (FD) capacitance (C_{FD}) and propose C_{FD} reduction methods for photon-countable sensitivity. We extracted each C_{FD} component using developed test patterns and confirmed that the sum of them agrees well with the measurement result of C_{FD} in sensor. C_{FD} reduction method based on the result of analysis was applied to FD and pixel source follower (SF). Its effectiveness was verified by the fabricated CMOS image sensor chip exhibiting conversion gain (CG) of 243μV/e^- (C_{FD} of 0.66fF).

INTRODUCTION

Image sensors with high signal-to-noise ratio (SNR) are required in various areas; information equipment including smartphone, industrial measurement, medical, in-vehicle equipment, security, etc. To achieve the high SNR, some approaches, electron multiplication [1], column amplifier and ADC [2-3], increasing CG at FD [4-5], have been reported.

Recently, many researches with regard to high SNR that allows photon counting have been carried out actively. It is necessary to reduce the input referred noise to 0.20e^-_{rms} for achieving the photon-countable sensitivity [6-7].

In the CMOS image sensor, increasing the gain at input stage of the readout circuit is the most valid method to reduce the input referred noise. In that sense, increasing CG is the most effective way. Therefore, analysis and reduction of the C_{FD} components are extremely important. It should be noted that satisfying both high CG and high full well capacity (FWC) is also important.

In this paper, an analysis methodology of C_{FD} using test element group (TEG) is described at first. Then, C_{FD} reduction method with device structure is proposed. Finally, the measurement results of image sensor chip we designed and fabricated are discussed.

THE ANALYSIS OF C_{FD} COMPONENTS

C_{FD} consists of p-n junction capacitance, gate overlap capacitance, and metal capacitance. Figure 1 shows an example of general pixel layout and its cross-sectional views and table 1 summarizes the detailed components of C_{FD}.

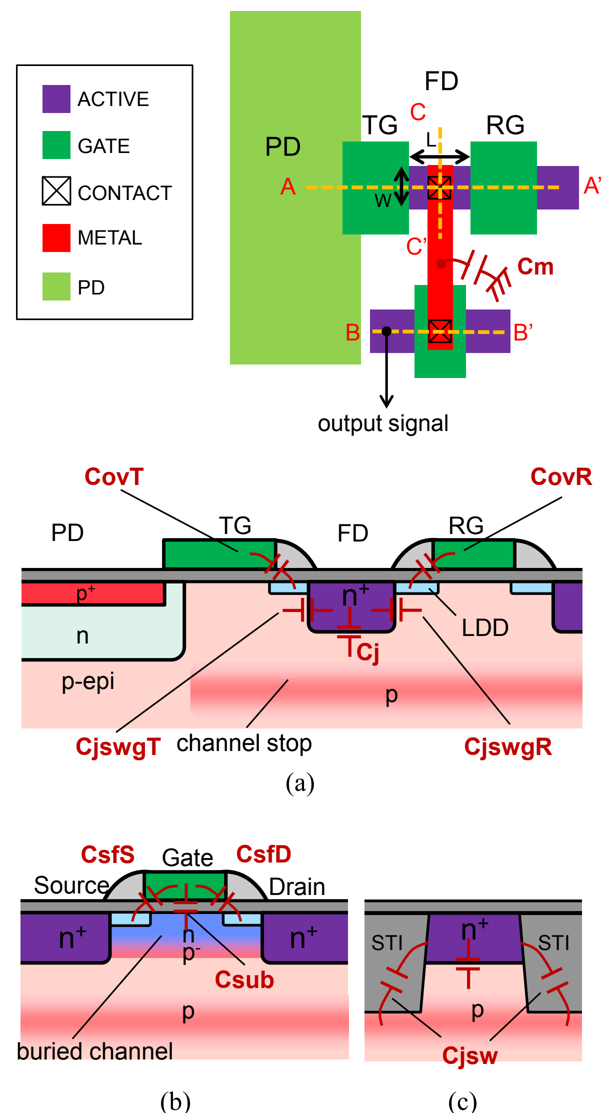

Fig. 1. Example of general pixel layout (upper figure) and cross-sectional views of (a) A-A', (b) B-B', (c) C-C'. C_{FD} consists of p-n junction capacitance, gate overlap capacitance, and metal capacitance.

Table 1. The detailed components of C_{FD}.

Main components of C_{FD}	Components of C_{FD}	Explanation
Gate overlap capacitance	$(1\text{-}G_{SF})\times CsfS$	gate overlap capacitance between gate and source at pixel SF with mirror effect
	CsfD & Csub	gate overlap capacitance between gate and drain at pixel SF and capacitance between gate and substrate at pixel SF
	CovR	gate overlap capacitance between FD and RG
	CovT	gate overlap capacitance between FD and TG
P-n junction capacitance	Cjsw	p-n junction capacitance between FD and p-epi under STI
	CjswgR	p-n junction capacitance between FD and p-epi under RG
	CjswgT	p-n junction capacitance between FD and p-epi under TG
	Cj	p-n junction capacitance between FD and p-epi under FD
Metal capacitance	Cm	metal capacitance

Figure 2 shows the conceptual diagrams of TEG used for extracting the components of C_{FD} in this work. Table 2 summarizes the detail of the TEG. The area of developed TEG is large enough to measure C-V characteristics accurately by existing impedance analyzers. Measuring the C-V curve of two TEGs, type A and B, and normalizing to the real size of FD in sensor, we can extract both p-n junction capacitance components, Cj and Cjsw. Additionally, measuring type C and using the data of Cj and Cjsw extracted from type A and B, we can obtain p-n junction capacitances, CjswgT and CjswgR, and gate overlap capacitance, CovT, CovR, CsfD, and CsfS. Thus, using linear calculations with various areas and lengths of STI and gate, we can extract all of the C_{FD} components listed in Table 1.

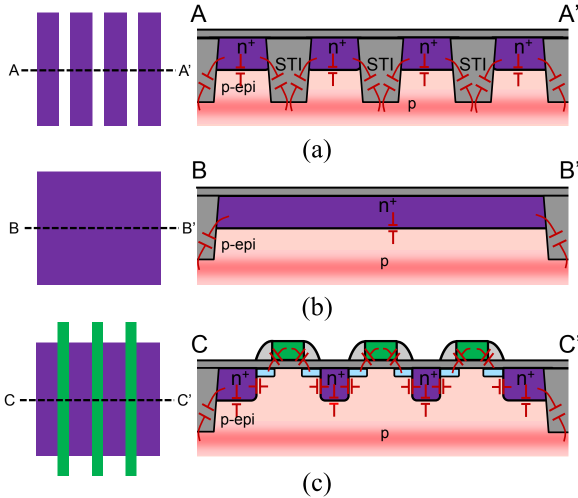

Fig. 2. Measurement TEG for
(a) type A (b) type B (c) type C

Table 2. The detailed of TEG patterns.

TEG patterns	Area [μm^2]	Length of STI [μm]	Length of gate [μm]
type A	1254	2552	–
type B	3648	242	–
type C	2337	200	2394

Measurement results of C-V characteristics about the components of C_{FD} assuming the image sensor with FD size (W/L) of 0.34μm/0.44μm are shown in Figure 3. The capacitances are almost constant for V_{FD} of 2.0-3.0V, where this voltage range is used for the actual image sensor.

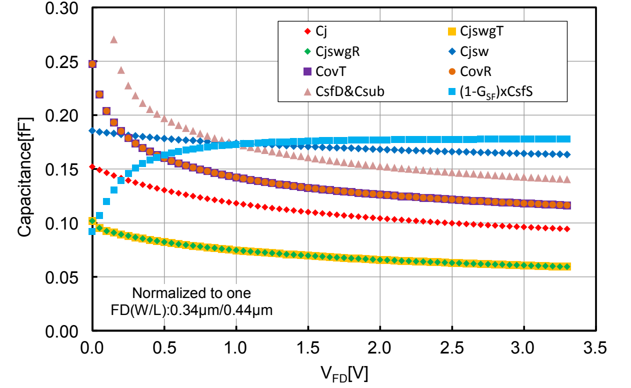

Fig. 3. Measurement results of C-V characteristics.

In Figure 4, the measurement result of C_{FD} in conventional CMOS image sensor is compared with TEG. Here, FD size of the sensor chip was 0.34μm/0.44μm and pixel SF size was 0.45μm/0.50μm. Pixel SF gain was 0.827 that was the measurement result of the sensor. Metal capacitance was estimated by the layout of the sensor. It is clear that the sum of C_{FD} components agrees well with the measurement result of C_{FD} in sensor. Also, gate overlap capacitance accounts for the highest percentage of C_{FD}, and p-n junction capacitance is following.

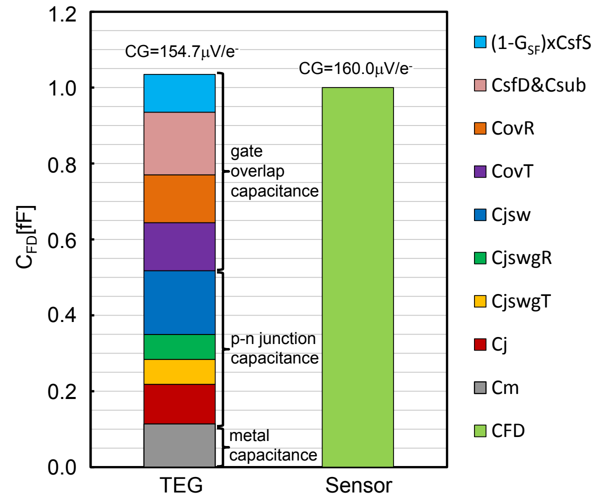

Fig. 4. Measurement results of C_{FD} in TEG and sensor

DEVICE STRUCTURE FOR REDUCING C_{FD}

Based on the results so far, we propose a device structure for reducing C_{FD}. Figure 5 shows the cross-sectional views of the small C_{FD} device structure. In this structure, omitting the implantation process of lightly doped drain (LDD) at FD and drain of pixel SF, n^+ diffusion layers with offset are formed by the self-aligned process [4]. By this means, gate overlap capacitance decreases. Also, using low dose at FD and drain of pixel SF and omitting the implantation process of channel stop under FD, depletion layer width increases. It contributes to the reduction of p-n junction capacitance. Additionally, applying low implant energy to FD and drain of pixel SF to make the p-n junction shallow. In consequence, the surface area of p-n junction reduces and this leads to the farther decrease of p-n junction capacitance and gate overlap capacitance. We revealed the implantation condition with no problem about charge transfer and hot electron. Regarding the pixel SF, the reason for omitting the implantation process of LDD and applying low dose and implant energy only to drain side is that source side is affected by a mirror effect which multiplies CsfS by ($1-G_{SF}$), where G_{SF} is the gain of pixel SF. It is the purpose of this asymmetric pixel SF structure to suppress an increase of resistance and the degradation of the pixel SF gain. It is important to note that these processes were applied to FD and pixel SF.

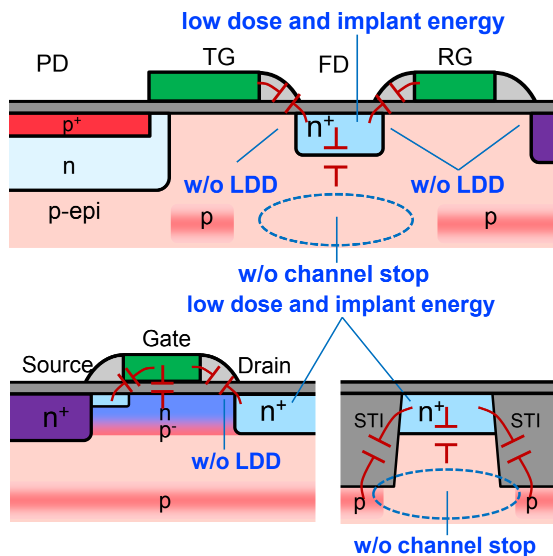

Fig. 5. Cross-sectional views of the proposed small C_{FD} device structure

CHIP FABRICATION AND RESULTS

We designed and fabricated image sensor chip with the device structure reflecting the proposed reducing method. Figure 6 shows the C_{FD} components and the net doping distribution of (a) conventional FD (n^+ with LDD), (b) n^+ without LDD, (c) low dose and implant energy n^+ without LDD and channel stop, (d) fine processing technology in (c). The values of C_{FD}s were obtained by measurements and the device simulations and the net doping distributions were calculated by the device simulation. We achieved a CMOS image sensor with high CG over 240μV/e^- in the case of (c) because of low dose and implant energy n^+ without LDD in FD and drain of pixel SF and no channel stop under FD. The lines on the net doping distribution illustrate the edges of the depletion layers. Though, this time, we used 0.18μm CMOS process technology, if we use more miniaturized process technology, for example, supposing FD size is 0.12μm/0.25μm and pixel SF size is 0.20μm/0.52μm, and apply the proposed method, we can estimate C_{FD} of 0.38fF and CG of 420μV/e^-.

Figure 7 shows the fabricated image sensor chip employing the device structure reflecting the proposed C_{FD} reducing method. This chip was fabricated using 0.18μm 1-Poly 5-Metal CMOS process technology with pinned PD. FD is the minimum size in this process, 0.34μm/0.44μm, and pixel SF size is 0.34μm/0.52μm. Figure 8 shows the captured image by using the CMOS image sensor with CG of 243μV/e^- (C_{FD} of 0.66fF) at room temperature with the average number of signal electrons, (a)~3e^-, (b)~10e^-, (c)~30e^-. Input referred noise of this sensor is 0.46e^-_{rms} [8]. Combining the proposed small C_{FD} pixel with lateral overflow integration capacitor (LOFIC) technology [8-9], we can achieve both almost photon-countable sensitivity and high FWC with a single exposure.

CONCLUSION

The components of C_{FD} extracted experimentally were demonstrated, and we proposed the very small C_{FD} structure with low concentration and shallow FD junction without LDD. We designed and fabricated the image sensor chip with the device structure reflecting the proposed C_{FD} reducing method, and it exhibited C_{FD} of 0.66fF and CG of 243μV/e^-.

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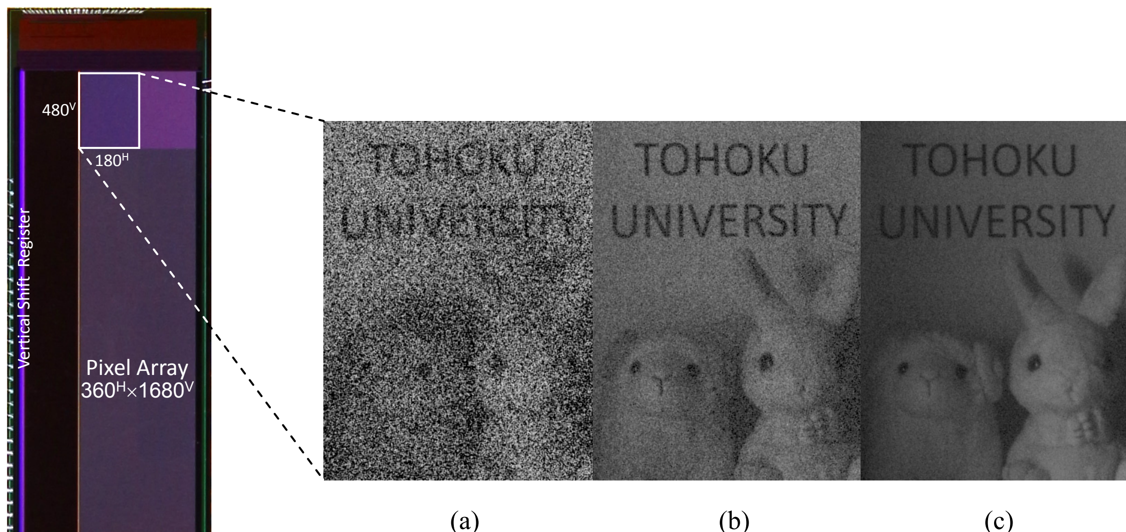
Fig. 6. Measurement and simulation results of C_{FD} in pixel transistors and simulation results of net doping distribution.



(a) (b) (c)

Fig. 8. Captured image at room temperature with the average number of signal electrons, (a)~3e$^-$, (b)~10e$^-$, and (c)~30e$^-$, with F#=4.0. The number of pixels is $180^H \times 480^V$.

Fig. 7. Fabricated CMOS image sensor chip micrograph.