Active Pixel Concepts for High-Resolution Large Area Imagers

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***Abstract*—In this paper, we show that for large area imagers the use of a current mode active pixel engine can increase the speed compared to a voltage mode pixel. Changing from a source follower topology to a common source amplifier can increase the charge gain while having no effect on other performance parameters.**

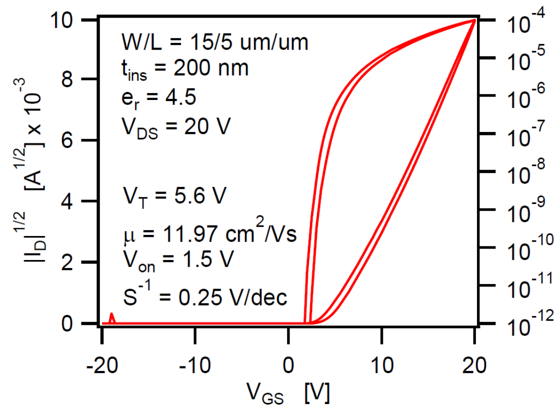
I. Introduction

Large area X-ray image sensors are attracting more and more interest in the last years [1]. For a long time only a-Si imagers could be fabricated [2]. Due to the low performance of a-Si in terms of mobility and stability, only passive pixel sensors (PPS) schemes could be used effectively. Thanks to new thin film semiconductors like a-IGZO showing higher mobility (see Figure 1a) and stability (see Figure 1b) [3], imagers with improved performance can be envisioned. In recent years, the first attempts to make an active pixel sensor (APS) have started using organic and oxide thin film semiconductors [1], [4]. This paper addresses the circuit perspective of such large area imagers, as shown in Figure 2 [5], mainly focussing on very high resolution .

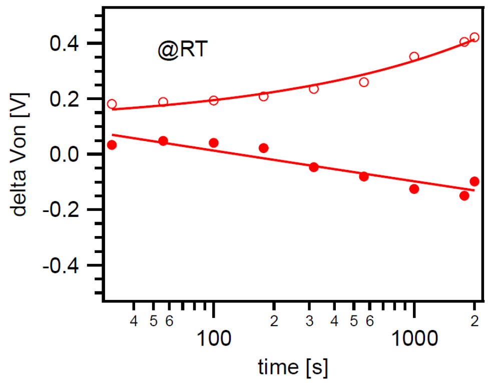
II. Voltage versus current mode

The active pixel sensor used in CMOS imagers is used in voltage mode, as shown in Figure 3a. It is common practice to use a source follower topology, shown in Figure 4a, as first introduced by Fossum [6]. If a pixel is read out, the voltage on the capacitor is transferred out of the matrix by a source follower (AMP in Figure 4a), hence voltage mode. The speed is limited, however, by the capacitance of the line, which has to be charged by the source follower. For large area imagers with high resolution, this is detrimental. Usually, the semiconductor is not single crystalline silicon, but a thin film semiconductor with much lower mobility (typically 10 cm^2/Vs in a-IGZO versus 1000 cm^2/Vs in bulk CMOS), limiting the current drive of the source follower. Furthermore, very large panels (sometimes hundreds of cm^2) will give dataline capacitances large enough to compromise imager performance. In Figure 5, a realistic simulation with relevant input parameters demonstrates this.

To overcome this issue, designers of large area imagers have looked to current mode pixels, schematically depicted in Figure 3b. The output of every pixel is a current proportional to the illumination, which is then integrated on a capacitor. The main advantage of this topology is higher speed, as the dataline voltage is fixed and charging of the line is not required. According to Gruev et al.



(a) Transfer curve of a typical a-IGZO transistor.



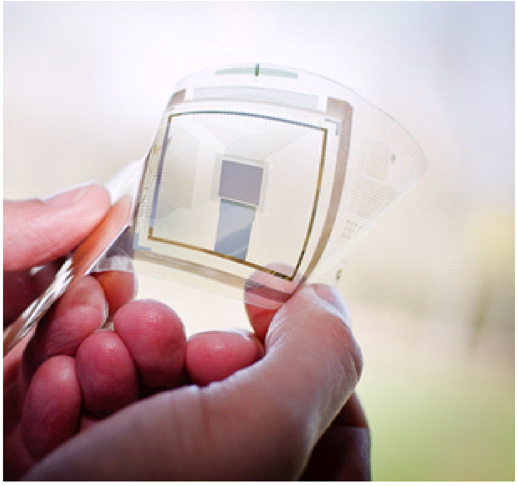
(b) Bias stress stability of a-IGZO transistors under 1 MV/cm continuous gate voltage applied.

Fig. 1. Transfer curve (a) and bias stress stability (b) of our self-aligned a-IGZO transistors [3].

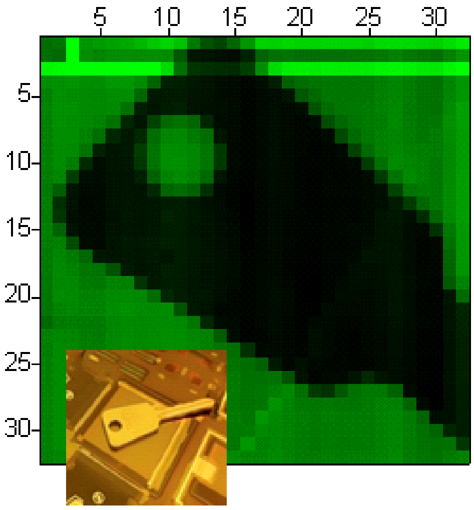
[7], this increased speed pixel design does on the other hand introduce more fixed pattern noise (FPN), decreased linearity and more temporal noise. The problem of FPN and decreased linearity can however be migitated in the digital domain, so that its influence is smaller than for imagers fabricated ten years ago. The increased noise can partially be compensated by using correlated double sampling, as proposed by Enz [8]. Furthermore, the noise performance is much better than the traditional passive pixel sensor (PPS) of large area imagers, since signal levels on the dataline are increased by the gain.

III. Current mode pixel circuits

Karim et al. [2] proposed to use the same source follower topology as for the voltage mode, but fix the dataline to

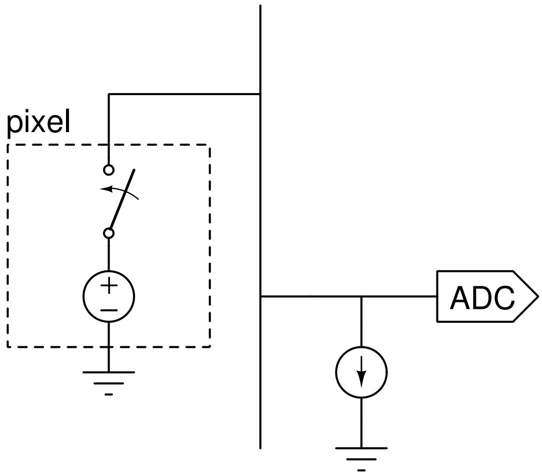


(a)

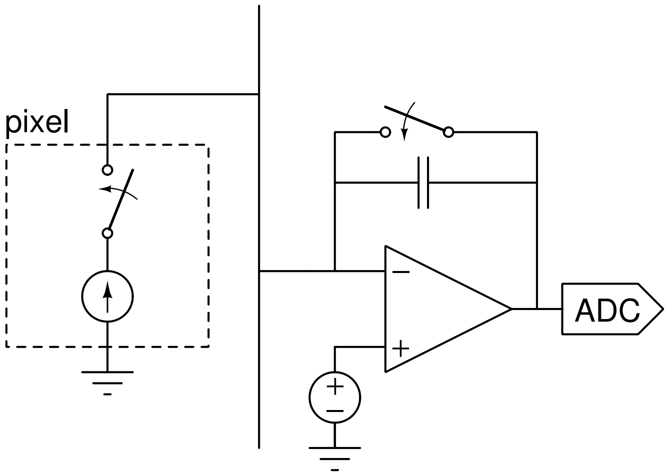


(b)

Fig. 2. A typical large area X-ray image sensor previously presented by our group [5].



(a) Voltage mode pixel readout



(b) Current mode pixel readout

Fig. 3. (a) Voltage mode readout of an imager pixel. This topology is typically used in CMOS imagers [6]. The voltage in the pixel is linear with the current of the photodiode and is directly converted to a digital signal. (b) Current mode readout of an imager pixel. This pixel is commonly used in large area imagers [2]. The current of the photodiode is amplified and the readout circuits integrate the current on a capacitor to a voltage, which is then converted to the digital domain.

a constant voltage and measure the current as shown in Figure 4a. This topology has been used in most other large area implementations [1], [4], [9]. Although Karim claims it is still a source follower, the circuit has essentially become a common source amplifier with source degeneration, and therefore less gain. We propose to put this upside down and use the amplifier in a pure common source topology with the select transistor on the drain side, as depicted in Figure 4b. This topology increases gain, since there is no degeneration. The dependence on the select transistor decreases, as the current is insensitive to the drain voltage of the amplifier transistor. In Figure 6, the gain is plotted in function of the ratio between the size of the select and the amplifier transistor. From simulations, the small signal gain has been calculated for a plausible situation with realistic transistor sizes and reference voltages. To determine the range of gains that can be obtained for a fixed pixel footprint, we keep the sum of both widths W_{tot} constant for a fair comparison. The ratio in Figure 6 determines the transistor size as $W_{AMP} = rW_{tot}$ and $W_{SEL} = W_{tot} - W_{AMP}$. From this figure, it can be seen that the in-pixel gain can be increased by a factor 1.8 by switching from the traditional large area pixel implementations to the common source amplifier pixel. In the future, we will show this in a large area X-ray imager demonstrator.

IV. Conclusion

For high resolution large area imagers, the voltage-based topology used in CMOS imagers cannot be used due to speed limitations. Current mode sensing can improve the performance of such panels by keeping the voltage on the dataline constant. In this case, the use of a common source amplifier instead of a source follower can increase the charge gain by up to a factor of 1.8.

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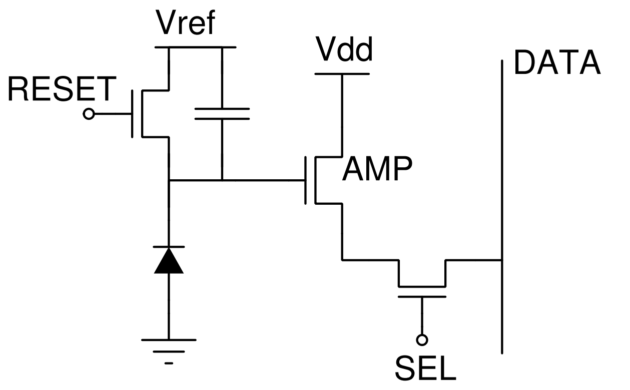
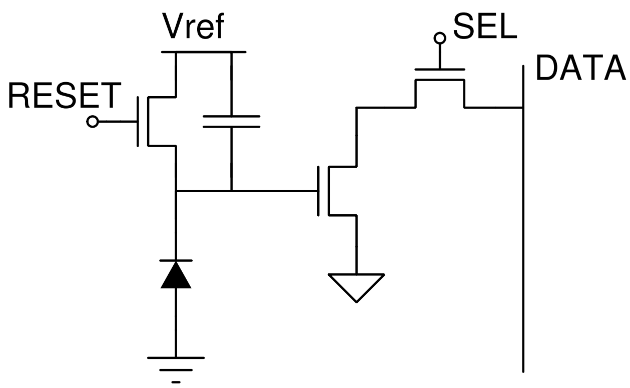


(a) Source follower topology



(b) Common source topology

Fig. 4. (a) Typical transistor schematic for an APS pixel used in voltage mode readout (see Figure 3a) [6]. It has also been previously proposed by Karim et al. to be used for current mode readout (see Figure 3b) of large area imagers [2]. Current is drawn from the source of the amplifier transistor. (b) Typical current mode pixel (see Figure 3b) with a common source amplifier. It was previously proposed by for CMOS current mode readout using pMOS transistors [7], [10]. It has higher charge gain thanks to the elimination of the source degeneration.

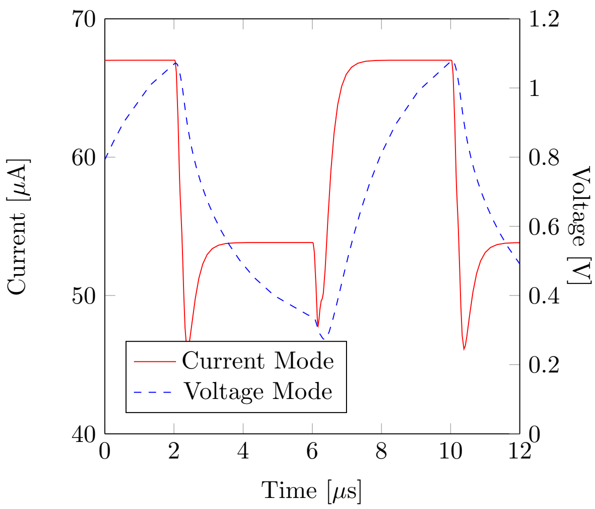


Fig. 5. Comparison of the speed of voltage and current mode under realistic conditions and with realistic models for transistors and panel parasitics. The dips in the current are caused by the switching of the access transistors. For the applied (and required) speeds, the voltage mode hasn't saturated to its final value value yet, and can therefore not be read out reliably.

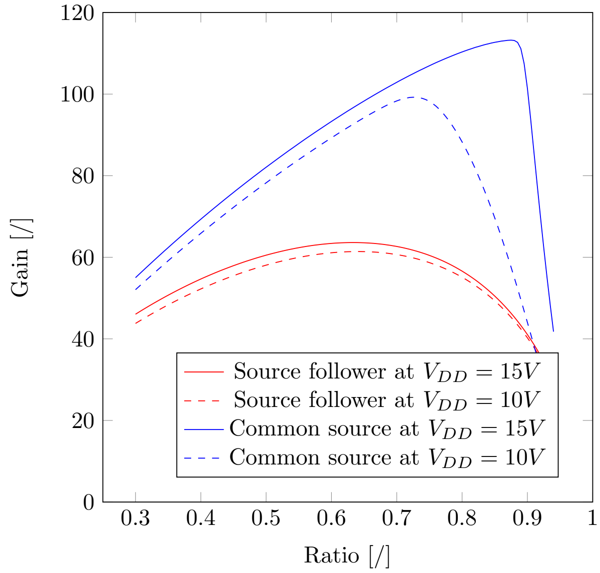


Fig. 6. Small signal charge gain of a current mode active pixel with constrained area (W_{tot}) as defined by Karim et al [2]. The ratio r determines the size of amplifier transistor (rW_{tot}) and select transistor($(1-r)W_{tot}$). The common source topology has always a significantly larger gain than the source follower topology, because there is no source degeneration. The steep drop of the source follower at high ratios is caused by the the voltage drop across the select transistor becoming too big and driving the amplifier transistor in linear regime.

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