High-density 3D interconnects Technology: The key for burst-mode very high speed imaging?

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***Abstract*— This work analyzes and compares performances of a burst-mode high frame rate imager architecture implementation respectively in a 2D (monolithic) and a high-density interconnect 3D stacked technology (based on the Tezzaron Cu-Cu bonding), both based on a 130nm CMOS process. This analysis makes use of a state-of-art architecture of burst mode very high frame rate imager and the good correlation between simulations and measurements of parasitic elements induced by wafer stacking obtained from a previous design performed by ISAE. An electrical model is developed for each implementation leading to simulations. The 3D technology implementation demonstrates a clear benefit in terms of frame rate increase due to a decrease of the pixel bus load and a limitation of the power consumption.**

***Index Terms*—CMOS Image sensors, 3D stacked technology, burst mode, high frame rate imager, frame rate.**

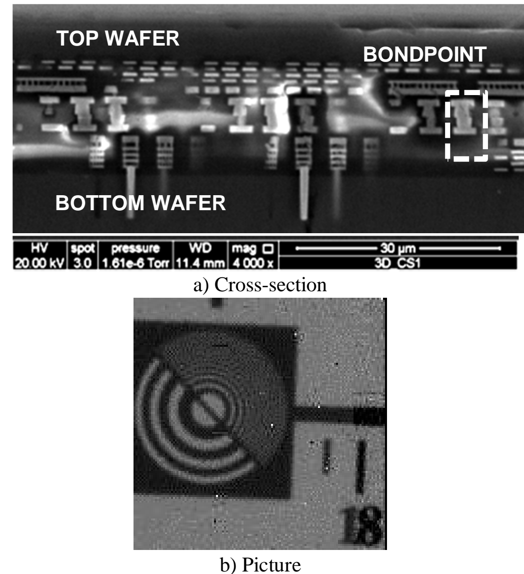
I. Introduction

For the past several years, it has been expected that 3D integration technologies will have a wide use for numerous applications where high integration density is required [1]. The use of high-density interconnect 3D technologies appears especially attractive when pixel requires dedicated resources for readout such optically and electrically shielded in-pixel storage node as in [2] and/or specific pixel level processing (CDS, thresholding,…).

It allows both topological constraints (fill-factor limitation) to be relaxed leading to enhanced electro-optical performances and the use of much reduced operating frequency pixel circuits. As an example, an array of 10bit in-pixel ADC (1 bondpoint per pixel) was implemented in high-density interconnect 3D-stacked technology [3] (Tezzaron Cu-Cu bonding of CMOS 130 nm wafers) as illustrated in Fig. 1 by the cross-section of the circuit and the obtained picture. This 3D technology allows high-density interconnects with a bond point size of 3.4µm and a minimum pitch of 5µm.

However the adoption, along the past years, of 2D Backside-Illuminated (BSI) technologies for imaging reduces the benefit of the high-density interconnects 3D integration by providing an increased optical aperture. Nevertheless, electrical constraints issues from applications using a large amount of in-pixel resources , such as burst- mode very high frame rate imagers [4]-[5] requiring a large amount of memory resources, cannot be solved only with BSI technologies.

In this work, we analyze and compare performances of burst-mode high frame rate imager architecture implementations respectively in a 2D (monolithic) and a high-density interconnects 3D stacked technology, both based on same 130nm CMOS process. For the 3D case, it makes use of the good correlation between simulations and measurements of parasitic elements induced by wafer stacking obtained from



a) Cross-section

b) Picture

Fig. 1: From [3] : This 128² CMOS image sensor with a 10bit in-pixel ADC and a 3T photodiode backside illuminated is manufactured with a 3D-Wafer-level technology. a) MEB cross-section of the 3D stacked sensor with bondpoint connection (Cu-Cu) and b) image grabbed.

the implementation described in [3].The analyzed architecture is based on a state-of-art architecture of burst mode very high frame rate imager proposed by Tochigi [5] at ISSC.

II. 2D Architecture Modelling and Analysis

This architecture, shown in Fig. 2, is composed of a pixel array (H400xV256), an analog memory array and a readout circuit with 40 outputs split between the top and the bottom of the circuit.

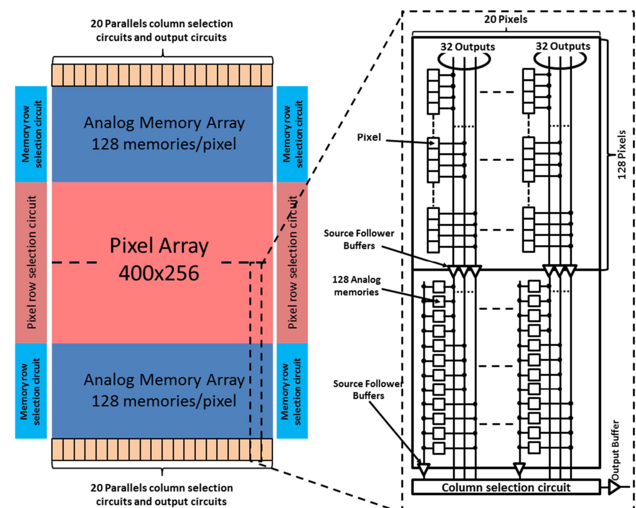


Fig. 2 : High frame rate CIS state of art architecture allowing burst mode from Tochigi [5] showing the global organization and the column readout circuit architecture.

Each pixel is associated with 128 analog memories allowing the burst acquisition mode. To sustain a high frame rate, only a few pixels (4) share their output circuits leading to multiple parallel pixel outputs bus (column bus).The pixel, working in global shutter mode with a 32µm pitch in case [5], consists of a pinned photodiode associated with a CDS circuit and an output pixel buffer circuit. This architecture, implemented in the 2D 130 nm technology, leads to the model depicted in Fig. 3 where the time requested to store a complete frame in the burst mode is given by equation (1).

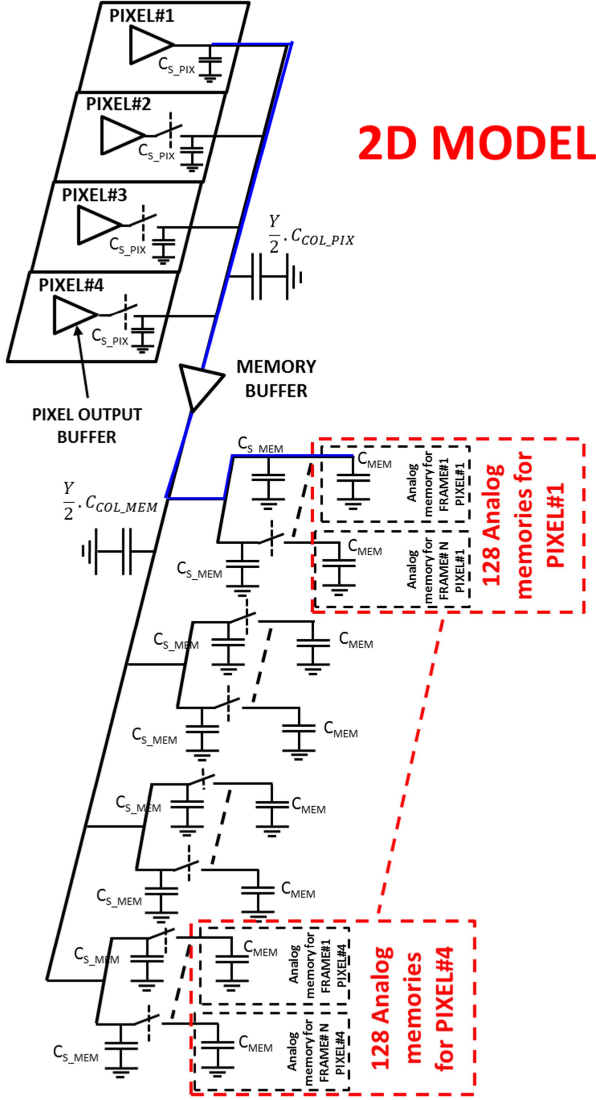


Fig. 3: Output pixel signal path allowing memory transfer time calculation for the architecture issued of [5] with a 2D CMOS technology.

This time is directly the integration time (leading to the acquisition rate) and it is composed of the in-pixel processing time, the access (T_{SEL}) time which must be taken into account as demonstrated in [6] and the memory transfer time.

$$\text{Integration time} = \text{Acquisition rate} = T_{IN\text{-}PIXEL_PROCESSING} + 4 \times T_{SEL} + 4 \times T_{MEMORY_TRANSFER} \quad (1)$$

The memory transfer time and selection time, depending on the architecture features and the technology used, are respectively shown in equations (2) and (3) with the parameters defined in Table 1.

$$T_{MEMORY_TRANSFER} = \left[\frac{Y}{2}.C_{COL_PIXEL} + 4.C_{S_PIX}\right].\frac{\Delta V1}{I_{COL1}} + \left[\frac{Y}{2}.C_{COL_MEM} + 4.N.C_{S_MEM} + C_{MEM}\right].\frac{\Delta V2}{I_{COL2}} \quad (2)$$

$$T_{SEL} = 3.\frac{1}{4}.X^2.R_{SEL}.C_{SEL} \quad (3)$$

The in-pixel processing time is chosen to 40 ns [5]. This model helps us to determine the impact of each phase in the case of a 2D 130nm CMOS process.

Name	Definition
C_{COL_PIX}	Pixel Column bus capacitance per unit of pixel pitch
C_{S_PIX}	Switch capacitance for pixel connection to column bus
C_{COL_MEM}	Memory column bus capacitance per unit of memory pitch
C_{S_PIX}	Switch capacitance for memory connection to column bus
C_{MEM}	Memory capacitance
Y, X	Pixel array row number, pixel array column number
N	Memory number per pixel (number of frame memorized)
ΔV1, ΔV2	Voltage swing to transfer from pixel output to C_{COL_PIX} (ΔV1) and from memory buffer output to C_{COL_MEM} (ΔV2). Both settled to 1V
I_{COL1}, I_{COL2}	Current required by buffers to transfer voltage drop from pixel output to C_{COL_PIX} (I_{COL1}) and from memory buffer output to C_{COL_MEM} (I_{COL2}) (worst case : slew rate limited [6]). Both settled to 100µA
R_{SEL}	Selection row resistance per unit of pixel pitch
C_{SEL}	Selection row capacitance per unit of pixel pitch

Table 1 : Parameter definitions for modelling and equations (2) and (3)

Fig. 4 shows the resulting memory transfer time and selection time as a function of the pixel size, from 16µm to 32µm and the equivalent acquisition rate for memory storage. These values are close to the Tochigi values without optimizations. This model allows us to identify the limiting phases. As can be seen on the Fig. 4, the major contributor is the memory transfer time which depends largely on the column capacitances (at pixel and memory levels).

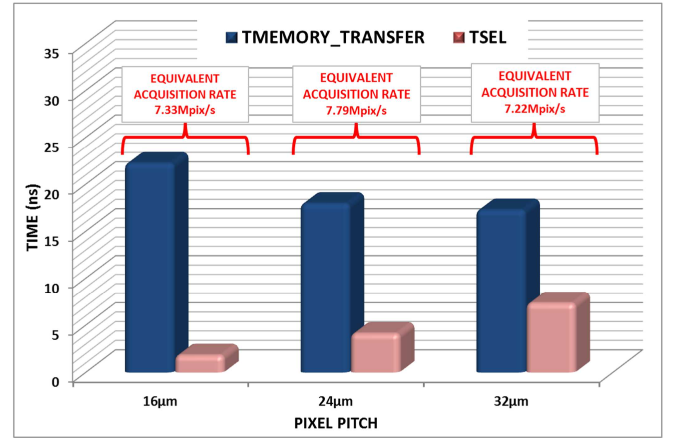
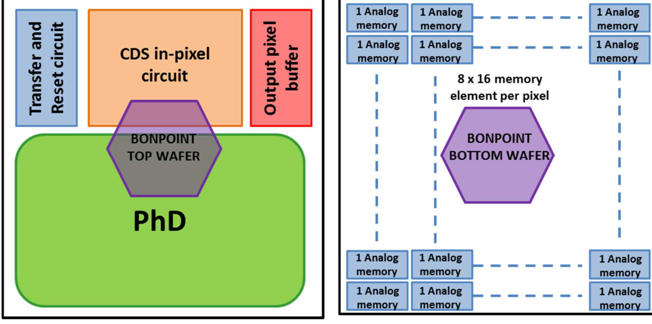


Fig. 4: Memory transfer time and selection time simulation for pixel pitch from 16µm to 32µm and for a 2D 130nm CMOS process based on extracted data from [3] (for H400xV256 format)

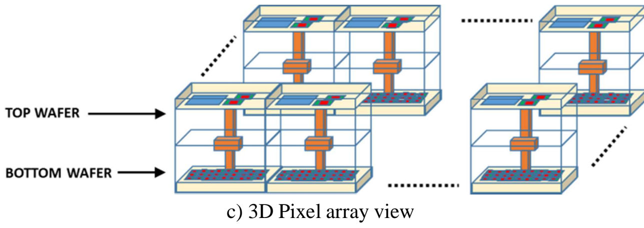
III. 3D ARCHITECTURE MODELLING AND ANALYSIS: THE BENEFITS

After an analysis concerning the partitioning of the different in-pixel functions in the frame of the 3D integration technology using high-density interconnects (3D-Wafer-level) and taking into account the optimization of the limiting elements of the integration time, a new architecture can be

defined as depicted in Fig. 5. To ensure the best partitioning the photodiode and the in-pixel CDS circuit are in the top wafer and the memory bank is in the bottom wafer (in the case of two staked wafers). If a higher number of stored frames is needed or if the pixel pitch decreases, the number of stacked wafers, containing memories, must be increased.



a) Pixel view (top wafer) b) Pixel view (bottom wafer)



c) 3D Pixel array view

Fig. 5: Organization of the pixel implemented in the 3D wafer level 130nm CMOS process with the partitioning of pixel functions on two layers. A bonpoint is needed to connect the two stacked wafers

This architecture allows a direct (single) access of the output pixel signal to the memory bank resulting in the new model shown in Fig. 6 associated to a new integration time equation (4).

$$\text{Integration time} = \text{Acquisition rate} = T_{IN\text{-}PIXEL_PROCESSING} + T_{SEL} + T_{MEMORY_TRANSFER} \quad (4)$$

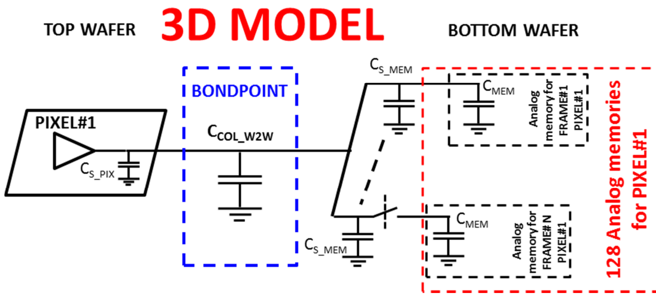


Fig. 6: Output pixel signal path allowing memory transfer time calculation for the architecture implemented in the 3D wafer level 130nm CMOS process

Equation (5) shows the new equation for the memory transfer time (no change of the selection time) and additional parameters due to the 3D-Wafer-level technology used.

$$T_{MEMORY_TRANSFER_3D} = \left[C_{COL_W2W} + C_{S_PIX} + N.C_{S_MEM} + C_{MEM}\right].\frac{\Delta V}{I_{COL}} \quad (5)$$

With C_{COL_W2W} : Capacitance from top wafer to bottom wafer (bondpoint capacitance)

ΔV: Voltage swing to transfer from pixel output to memory settled to 1V

I_{COL}: Current required by buffer to transfer voltage drop from pixel output to memory (slew rate limited case [6]) settled to 100µA

Fig. 7 shows the resulting memory transfer time and selection time as a function of the pixel size, from 16µm to 32µm and the equivalent readout speed for memory storage with the use of a 130nm 3D-Wafer-level technology. As can be seen, the memory transfer time decreases drastically leading to an increase (x3) of the readout speed for memory storage compared to the monolithic implementation.

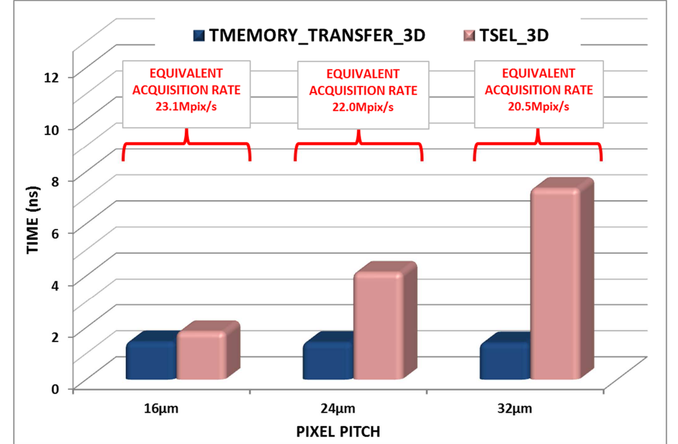


Fig. 7: Memory transfer time and selection time simulation for pixel pitch from 16µm to 32µm (for H400xV256 format) and for an implementation in a 3D wafer level 130nm CMOS process based on our experience from [3] with a buffer current of 100µA

It has to be noted that, from the 3D organization, the output pixel signal path does not depend on the pixel array format leading to an independence of the array size on the memory transfer time. This is depicted in the Fig. 8 where the memory transfer times for 2D and 3D versus image sensor format are shown. The memory transfer time for 3D implementation is constant whatever the sensor format whereas it drastically increases for the 2D implementation. This analysis is done for 128 frame memories per pixel and a 32µm pixel pitch leading to very large size requiring stitching.

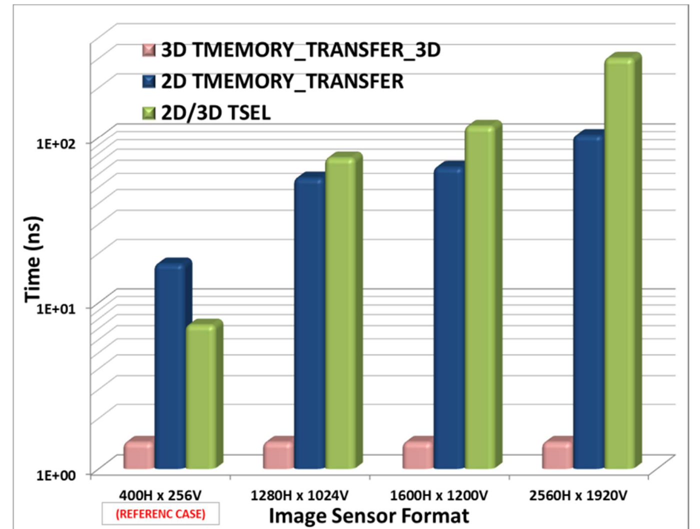


Fig. 8: Memory transfer time comparison between 2D and 3D implementation in function of the image sensor format

As can be seen, the selection time for the both implementations is the same (same row selection circuit) and **becomes the major contributor limiting the frame rate as sensor format increases**. This point is demonstrated in the Fig. 9 where, for both implementations, the frame rate decreases. However, as can be seen, the 3D implementation is still very competitive compare to 2D implementation frame rate. Indeed, the frame rate can be enhanced up to 400% depending on the sensor format.

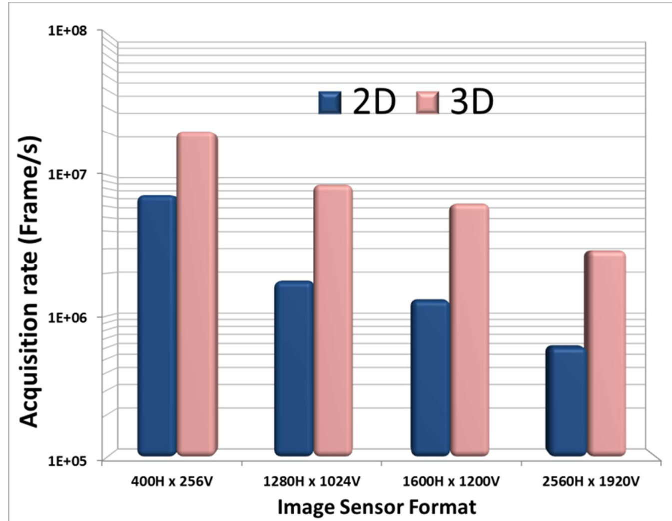


Fig. 9: Image sensor acquisition rate for the both implementations: 2D and 3D in function of the image sensor format

Fig. 10 shows the analysis results concerning the frame rate of the 2D and 3D implementation at function of the frame memory depth. A 32µm pixel pitch is taken into account and, for the 3D implementation, multiple stacked wafers are required to reach a high frame memory number.

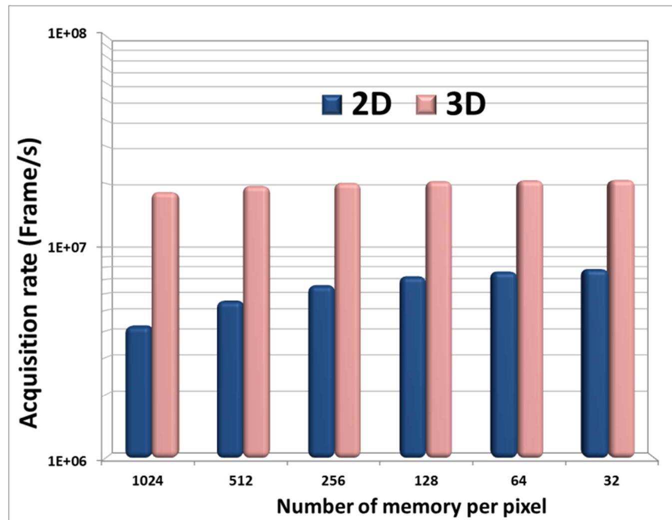


Fig. 10: Image sensor acquisition rate for the both implementations: 2D and 3D in function of the number of memory per pixel (32µm pixel pitch for H400xV256 format)

The 3D implementation show a nearly constant frame rate up to 1024 memories per pixel while the acquisition rate decreases quickly as the number of memory per pixel increases in the 2D implementation.

Another benefit is the reduced current required to transfer the pixel signal to the memory bank which is the major contributor for the whole consumption [5]. In the 2D implementation, as can be seen in the Fig. 3, two buffers are required to drive the pixel and memory column load while in the 3D implementation, due to the bus load decrease, only one buffer can be used. Hence, as depicted in Fig. 11, to reach the same acquisition rate than the 2D implementation, a lower current is needed with a decrease up to 95%.

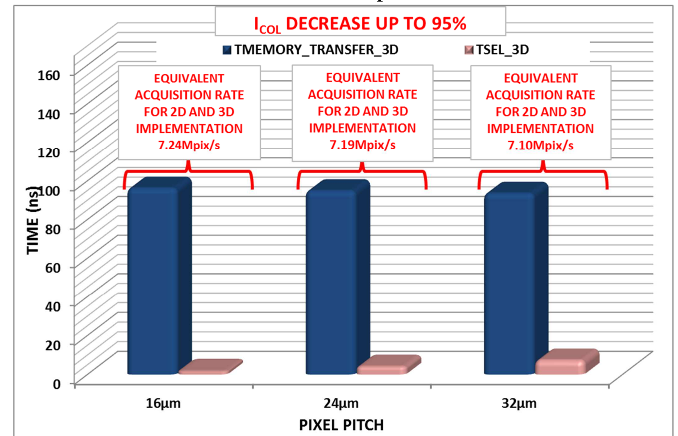


Fig. 11: Memory transfer time and selection time simulation for pixel pitch from 16µm to 32µm and for an implementation in a 3D wafer level 130nm CMOS process based on extracted data from [3] with a buffer current decrease up to 95% in order to get the equivalent acquisition rate for memory storage than monolithic implementation (for H400xV256 format)

IV. Conclusions

The two models developed in this work for the 2D and 3D implementations, based on a state-of-art architecture of burst mode very high frame rate imager proposed by Tochigi [5] and our extracted data on a high-density interconnects 3D stacked technology [3] show a drastic decrease of the pixel bus load. **Thus, the 3D technology implementation demonstrates a clear benefit in terms of frame rate increase even when the image sensor format increases and a reduction of the power consumption.**

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