A Dual-Mode CMOS Imager for Free-Space Optical Communication with Signal Light Source Tracking and Background Cancellation

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Abstract

This paper presents a dual-mode CMOS imager with free-space optical communication capability for augmented reality application. The proposed imager implements two operation modes as imaging mode and communication mode on a single sensing array. In imaging mode, the sensing pixel output raw image data based on the conventional integration-and-readout operation. In communication mode, the location of the target signal light source is defined automatically by proposed tracking mechanism. Then, the modulated light signal is extracted from the selected region-of-interest (ROI) in a real-time photocurrent sensing and summation operation. Background cancellation scheme is also implemented to enhance the signal-to-noise ratio (SNR) performance under a limited signal swing. The dual-mode function is realized by a compact pixel structure with four transistors (4-T). A 64×64 pixel array prototype chip with 7.6×7.6 um^2 pixel pitch and 45% fill factor has been designed and fabricated in 0.18um CMOS technology. The measurement results demonstrate a 120fps image capture in imaging mode, and a tracking time of 20μs with a -3dB bandwidth of 6MHz in communication mode.

I. Introduction

Image sensor communication (ISC) is a technology that does optical wireless communication which has gained a lot of attention recently [1]-[3]. Several approaches for ISC have been proposed and discussed [4]-[7]. The ISC technology is essential for free-space optical communication because its capability of implementing smart functions such as tracking and background cancellation, for finding the signal light source and cancelling the undesired background information, respectively.

This paper proposes a dual-mode imager with ISC capability for augmented reality application. Fig. 1 shows the operation concept. As the scene is captured by the dual-mode imager, the image is reconstructed in imaging mode. In communication mode, it starts with a region-of-interest (ROI) tracking of the signal light source; and then the modulated light signal is extracted from the selected region. By interleaving these two operation modes, the image with specific information on corresponding location is obtained as augmented reality.

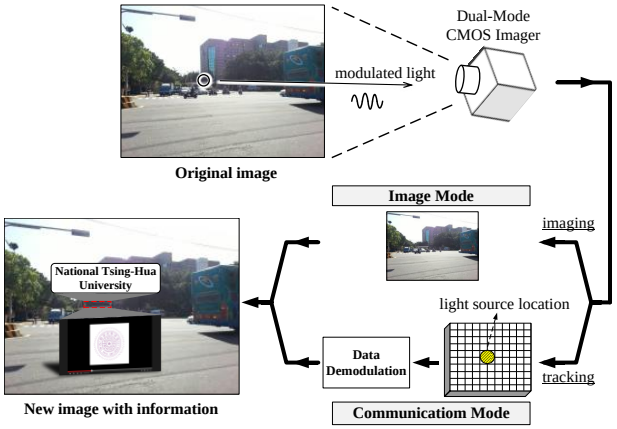


Fig.1 Operation concept of the proposed dual-mode imager

In this paper, a 64×64 pixels dual-mode CMOS imager for free-space optical communication is proposed. A compact pixel structure with 4 transistors [7] is adopted for the dual-mode operation. The conventional integrated-and-readout operation and programmable current summation is achieved in the proposed compact active pixel structure. By utilizing the same pixel for imaging and communication signal sensing instead of separated ones, the area efficiency and sensitivity performance are improved by 2 times for both modes.

In imaging mode, the image-induced photocurrent is integrated and readout to output the raw image data after correlated double sampling (CDS) operation. In communication mode, the location of the target signal light source is defined by the two-dimensional current projection and comparison with tunable thresholds. Then the data-modulated photocurrent in region-of-interest (ROI) of signal source is summed up and converted to voltage in real time by the following trans-impedance amplifier (TIA). The buffered-direct injection (BDI) interface circuit with DC background feedback and cancellation is applied before TIA to improve the bandwidth and available signal swing of AC communication signal.

The outline of this paper is as following. In Section II, the architecture and the circuit of the imager is described. Then, the measurement results are presented in Section III. Finally, the conclusions are drawn in Section IV.

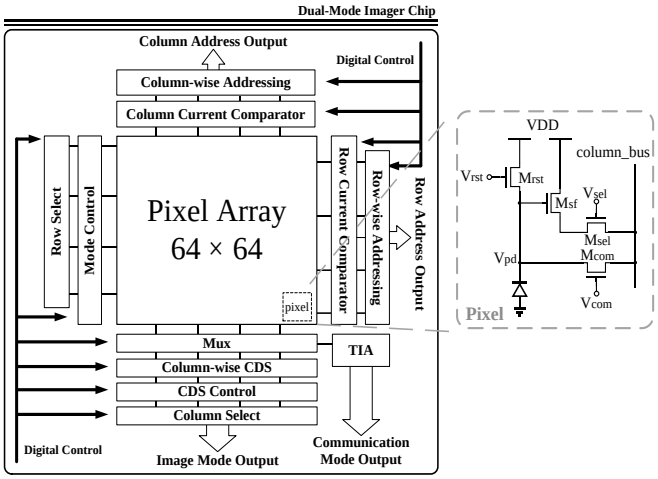


Fig.2 Block diagram of the proposed dual-mode imager

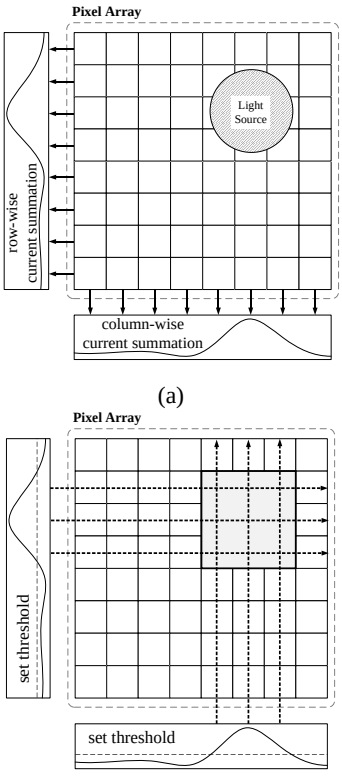


Fig.3 Signal light tracking (a) column-wise and row-wise current summation (b) set the threshold and defined the region

II. Architecture and Circuit Implementation

A. Chip overview & circuit implementation

Fig. 2 shows the system architecture of the proposed dual-mode imager. The prototype chip consists of a 64×64 pixel array, correlated double sampling (CDS) circuit, current comparators, trans-impedance amplifier (TIA) and digital control circuit. The dual-mode pixel [7] with 4 transistors achieves a fill factor of 45% in 7.6um×7.6um pitch. The CDS operation is implemented for in-pixel threshold offset cancellation in image mode. Mux is used to wire together the selecting columns for current summation in communication mode. The current comparator is implemented for ROI tracking function by comparing the current projection in two dimensions (row and column wise) with a tunable threshold.

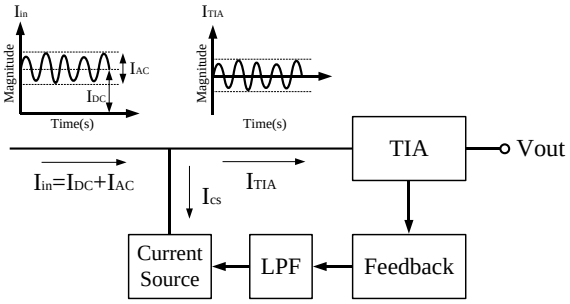


Fig.4 Operation concept of background cancellation

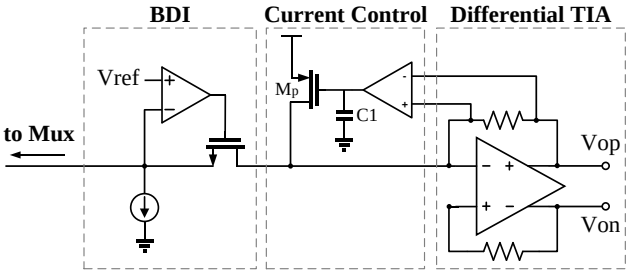


Fig.5 TIA with background cancellation circuit

B. Signal light tracking

Fig. 3 shows the operation concept of ROI tracking function of signal light source. In communication mode, the location of signal light source can be realized by the proposed tracking mechanism. With the signal light source illuminated at the pixel array, Fig. 3(a) shows the row-wise and column-wise signal intensity profile by summing up the signal current in the row and column directions, respectively. The location of light source is then defined by applying current comparisons in both directions to generate the corresponding X-Y addresses with a tunable threshold as shown in Fig. 3(b). The X-Y addresses are then fed back to enable the corresponding ROI of signal source directly with a tracking time less than 20μs.

C. Background cancellation

Fig. 4 shows the operation concept of background cancellation. The input current I_{in} is a DC (I_{DC}) + AC (I_{AC}) signal where I_{DC} is the background level and I_{AC} is the modulated data signal. By sensing the signal from TIA block and feed it back to control a current source (I_{CS}) after the low pass filter (LPF) block, the DC portion I_{DC} is subtracted out by I_{CS} and only the AC signal residue I_{TIA} = I_{AC} is passed to TIA and amplified.

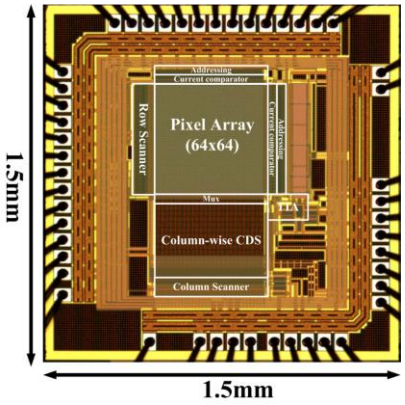
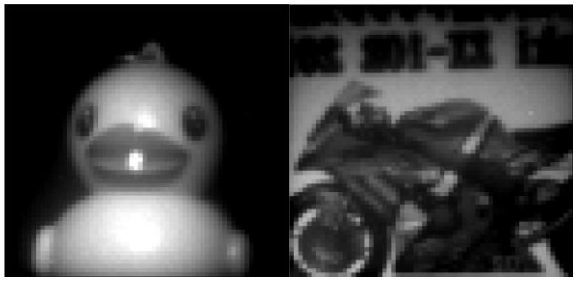
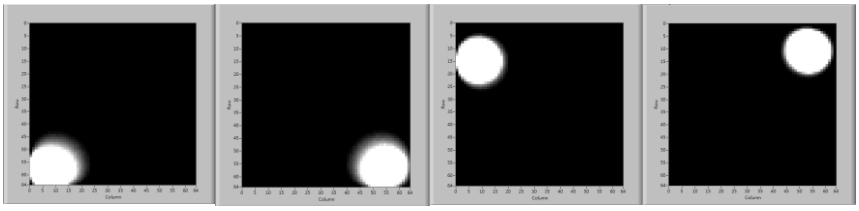


Fig.6 Micrograph of the fabricated chip

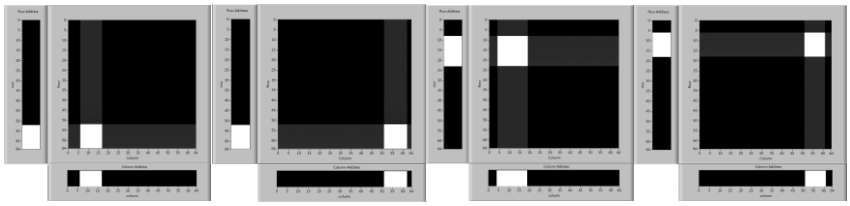


(a) (b)

Fig.7 The captured images from the prototype chip



(a) (b) (c) (d)



(e) (f) (g) (h)

Fig.8 Light source located at (a) lower left (b) lower right (c) upper left (d) upper right; (e) ~ (h) corresponding tracking results

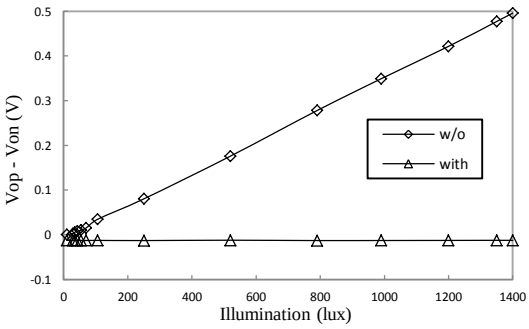


Fig.9 Measured TIA output wi/wo background cancellation

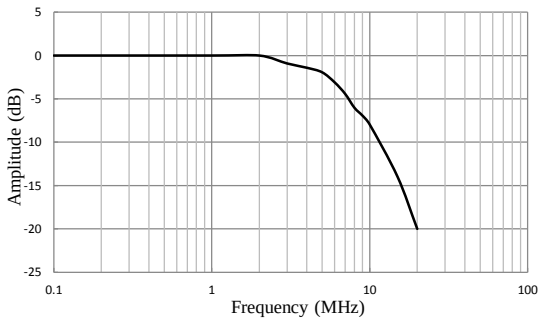


Fig.10 Measured frequency response in communication mode

Fig. 5 shows the circuit implementation of signal current readout in communication mode with BDI, TIA, and background cancellation. The TIA block is a differential current-to-voltage conversion circuit with BDI current buffer and background cancellation function for DC blocking. The buffered-direct-injection (BDI) input stage provides a low input impedance to increase the effective bandwidth. The background (DC) level is sensed by the voltage difference of TIA's resistor with a low-pass filtering function implemented by an off-chip capacitor C1 (in current control block). A voltage-control-current-source (Mp) feedback loop is applied to subtract out the DC current level and achieve the background cancellation. By fully utilization of available swing for effective modulated (AC) signal, the SNR performance can be improved with a larger TIA gain.

III. Experimental Results

Fig. 6 shows the microphotograph of fabricated chip in TSMC 0.18μm 1P6M standard process. The sensing array is 64×64 with a pixel size of 7.6μm×7.6μm and a fill factor of 45%. The total chip occupies an area of 2.25mm^2 (1.5mm × 1.5mm).

TABLE I

Performance summary and comparison

Reference	[4]	[5]	[6]	[7]	This work
Technology	0.35μm CMOS	0.35μm CMOS	0.18μm CMOS	0.18μm CIS	0.18μm CMOS
Array size	128×128	320×240	640×240 (image cell) 640×240 (LPR cell)	320×480 (image cell) 320×480 (LPR cell)	64×64 (dual-mode cell)
Pixel pitch (μm^2)	26×26	7.5×7.5	7.5×7.5	7.5×7.5	7.6×7.6
In-pixel transistors	25	4	8	6	4
Fill factor	13.4%	N/A	20%	N/A	45%
Frame rate	30fps	30fps	60fps	60fps	120fps
Tracking time	N/A	N/A	N/A	15ms	<20μs
Bandwidth	4850bit/ID	1.1kfps/ID	1MHz	2.5MHz	6MHz

Fig. 7 shows the captured images in imaging mode in 120fps. Fig. 8 shows the signal light source tracking result. Fig. 8(a)~8(d) show the captured images of light source located at lower left, lower right, upper left, and upper right, respectively. Fig. 8(e)~8(h) show the ROI tracking results corresponded to Fig. 8(a)~8(d). In Fig. 8(e)~8(h), the lower and left panels show the comparator outputs in column and row directions of current projection, respectively; and the central panel shows the allocated ROI window.

Fig. 9 shows the measurement result of TIA output level with and without background cancellation. It shows the TIA output voltage sustains constant with background cancellation instead of increasing according to the input illumination.

Fig. 10 shows the measured frequency response in communication mode with a -3dB bandwidth of about 6MHz. Table I shows the performance comparison of the prototype with the state-of-the-art designs.

IV. Conclusion

This paper presents a 4096 pixels dual-mode CMOS imager for free-space optical communication with signal light source tracking and background cancellation capabilities. The dual-mode function is realized by a compact pixel structure with four transistors (4T) with a fill factor of 45% in a pitch of 7.6um×76.um. The prototype achieves a frame rate of 120fps in imaging mode; and a signal source tracking time under 20μs, a -3dB receiver bandwidth of 6MHz, and background cancellation function in communication mode. The proposed dual-mode CMOS imager is suitable for using in VLC system, such as indoor optical communication and augmented reality system.

Acknowledgment

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