Toward 10 Gfps: Factors Limiting the Frame Rate of the BSI MCG Image Sensor

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1. 1Gfps- to 1Tfps-imaging technologies

In 1996, Shiraga,et al. developed a 100 Gfps camera system for laser fusion research by sweeping an electron beam bundle in a streak tube in a direction slightly slanted to a grid of holes on a metal light shield in front of the photoelectron conversion layer[1]. The year 2014 was an epoch-making year for ultra-high-speed imaging. Three reports on 100 Gfps to 1 Tfps imaging were presented: (1) a 100 Gfps camera system with a streak camera and random-dot illumination[2], (2) a 1 Tfps imaging apparatus using chirping and detaching a short laser pulse and multi-spectrum imaging[3], and (3) a 1 Tfps imaging method consisting of femtosecond laser illumination, picosecond-accurate detectors and mathematical reconstruction techniques, though this is not consecutive imaging[4].

In practice, multi-framing cameras for burst-imaging at about 1 Gfps are available. The camera splits an incident light beam with a mirror set to make the same images as the incident one, sends them to built-in multi-high-speed gating cameras, and gates the cameras in turn at an interval of about 1 ns. The fundamental problem of the camera system is that the light incident to each gating camera reduces proportionately to the inverse of the number of the built-in cameras. Therefore, the sensitivity is less than 1/N of that of the built-in camera, where N is the number of the built-in cameras. Higher sensitivity is crucial in ultra-high-speed imaging. Other methods also have disadvantages, such as lower spatial resolution, bulky systems, and lower sensitivity.

On the other hand, no solid-state image sensor has allowed for imaging at the frame rate more than 1 Gfps. Recently, Mochizuki, Kagawa et al. presented a CMOS imager with groups of multiple pixels, each operated with different shuttering patterns, which stores compressed consecutive images. Solving the inverse problem of the compressed image data provided burst images at the frame rate of 200 Mfps[5].

We proposed a structure of a 3D-stacked image sensor consisting of a BSI MCG image sensor[a] chip and a driver chip with in-situ ROXNOR[b] drivers, which enables burst imaging faster than 1 Gfps with a 100% fill factor[6]. To achieve a higher frame rate, the limiting factors of the frame rate of the sensor chip are analyzed in this paper. The performance of the ROXNOR driver chip is analyzed in the sister paper[7]. The test chip is under process in IMEC.
(Notes: a) Backside Illuminated Multi-Collection-Gate image sensor, b) A driver consisting of Ring Oscillator with XNOR circuits)

2. BSI MCG Image Sensors

Fig. 1 shows the structure of a BSI image sensor with in-situ storage in each pixel on the front side. To avoid direct intrusion of leftover electrons after photoelectron conversion in the bulk silicon layer, a thick p^-/n^- double epi-layer was developed: To prevent migration of generated signal electrons to the in-situ storage of each pixel on the front side, a shaped p-well was introduced. Fig. 2 shows a pixel model of a hexagonal MCG image sensor on the front side. Fig. 3 shows an example of a Monte Carlo simulation on paths of the signal electrons to one of the collection gates, A.

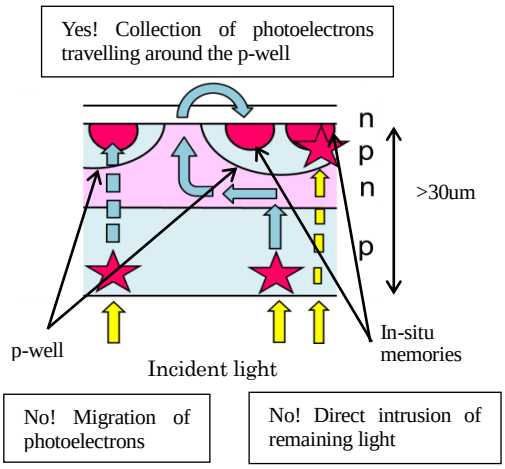


Fig. 1 The pnpn-structure of a BSI ISIS[6]

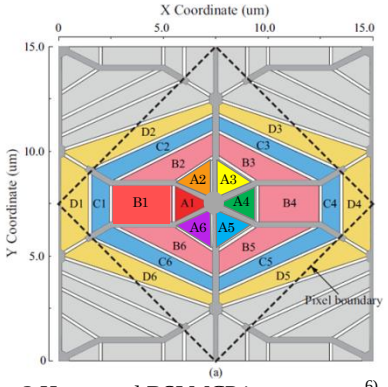


Fig. 2 Hexagonal BSI MCP image sensor[6]:
A1: Drain gate; A2-A6: Collection gates;
B1: Drain; B2-B6: Storage gates;
C: Barrier gates; D: Transfer gates

3. Limiting factors of the frame rate

Table 1 shows the limiting factors of the frame rate of the 3D-stacked BSI MCG image sensor. For the sensor chip, the frame rate is dominated by an electronic factor - the travelling time distribution of signal electrons from the generation sites to one of the collection gates, and an electric factors limiting the operation speed of the collection gates, i.e., the amplitude of the driving voltage of the collection gates and the capacitance and the resistivity along the route from the interface to the driver chip to each collection gate.

Table 1 limiting factors of the frame rate of the 3D-stacked BSI MCG image sensor

sensor chip	distribution of travel time of signal electrons (electronic factors)	segments	S1	thickness of the backside hole layer/wave length	thickness of backside Boron implanting
			S2	field between back/front sides	front/backside voltages
				chip (depletion layer) thickness	
			S3	position of incident light on the backside plane of a pixel, design of P-well, size of a pixel	
			S4	field between back/front sides, thickness of P-well	
			S5	voltage differences of collection/storage gates, size of gates	
	operation rate of collection gates (electric factors)	collection gate area		Collection-gate size, thickness and material of dielectric layer	
		diving voltage delivery		RCL along the delivery route	
interface	RC delay	parasitic capacitance and resistivity at contact points for stacking			
driver chip	requirement from sensor chip	load		capacitive load, operation voltage swing	
		stability		Voltage and timing in a driver and among drivers	
	power consumption	individual		number and size of transistors, parasitic capacitance and resistance	
		total		number of the driver (areal ratio of one driver unit to one pixel)	
Other effects	dark current due to the mechanical stress at stacking, process node (size effect, mask availability, materials (e.g., GaAs CCD), temperature (heat generation and release)				

4. Minimizing the range of travelling time of signal electrons in the sensor chip

The temporal resolution limited by the electronic factor is defined by $k\sigma$, where k and σ are respectively a constant and a standard deviation of the electron travelling time as shown in Fig. 4. For example, when $k < 2$, a sum of two overlapped Gaussian distributions with the distance of $k\sigma$ does not have two distinguishable peaks, and when $k = 6$, mixing of signals is almost negligible. In this paper, the temporal resolution of 4σ is employed. Each electron path consists of five segments as shown in Fig. 3 and summarized in Table 1. The segments S1, S3 and S5 are the main sources to increase σ. While the random motion of electrons seems significant in the segment S2 as shown in Fig. 3 (a), it is actually smoothed out during travelling in a strong field in the depleted bulk silicon layer as seen in Fig. 3 (b). The segment S1 is in the hole accumulation layer at the backside, S3 is around the p-well, and S5 is the path under the p-well after the electrons collected to the center hole of the p-well. The increase in the standard deviation σ in the segment S1 is due to a pure diffusion, and those in the segments S3 and S5 due to a combination of diffusion by a random electron motion and distance distributions of generation sites to the pixel center (S3) and to a collection gate (S5). The travel time distribution is analyzed in Fig. 5.

The segment S1 can be effectively reduced by introducing a very thin highly-doped backside Boron layer. The effect of the segment S3 can be mitigated by guiding incident light to the backside of each pixel center as shown in Fig. 6. Then, the random motion in the segment S5 finally remains as the main source of delay in the travelling time.

The Monte Carlo simulation has provided a very useful result. As shown in the table in Fig. 5(c), the standard deviation σ for the incident light to the pixel is almost constant, from 0.0428 ps to 0.0448 ps, independent of the depth (thickness) of the epi-layer. Therefore, the temporal resolution 4σ is 171 ps to179 ps (<180 ps),

We are now focusing on observation of the electron movement in the layer under the p-well, S5, to further reduce the temporal resolution with 3D Monte Carlo simulations. The results shown in Fig. 5 were obtained for the case where the high driving voltages VCH of a collection gate and the voltage of the neighboring storage gate are the same. Introducing a voltage deference between the two gates further reduces the temporal resolution to 100 ps.

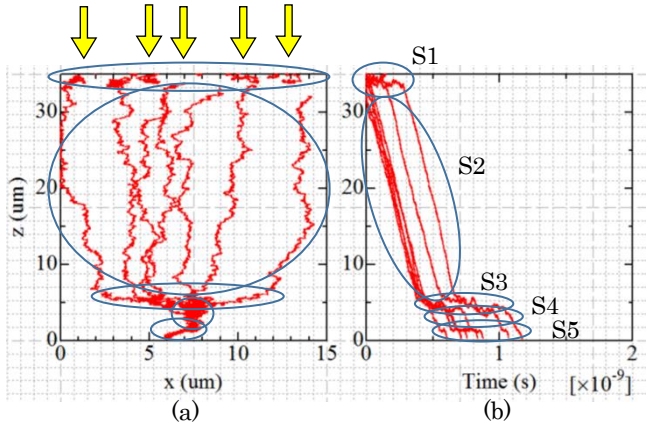


Fig. 3 Monte Carlo simulation of motion of signal electrons[6)]
(a) Trajectories, (b) Travel time vs. distance (depth)
S1: Random motion in the backside hole accumulation layer,
S2: Drift in the depletion layer, S3: Roundabout around p-well,
S4: Vertical movement in the p-well hole,
S5: Horizontal movement from a collection gate to a storage gate

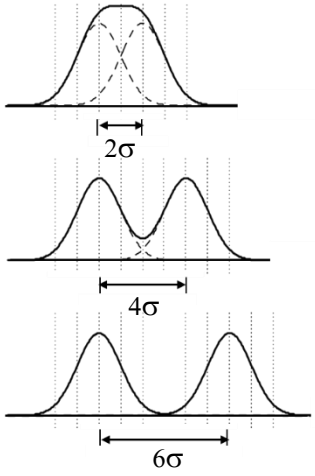


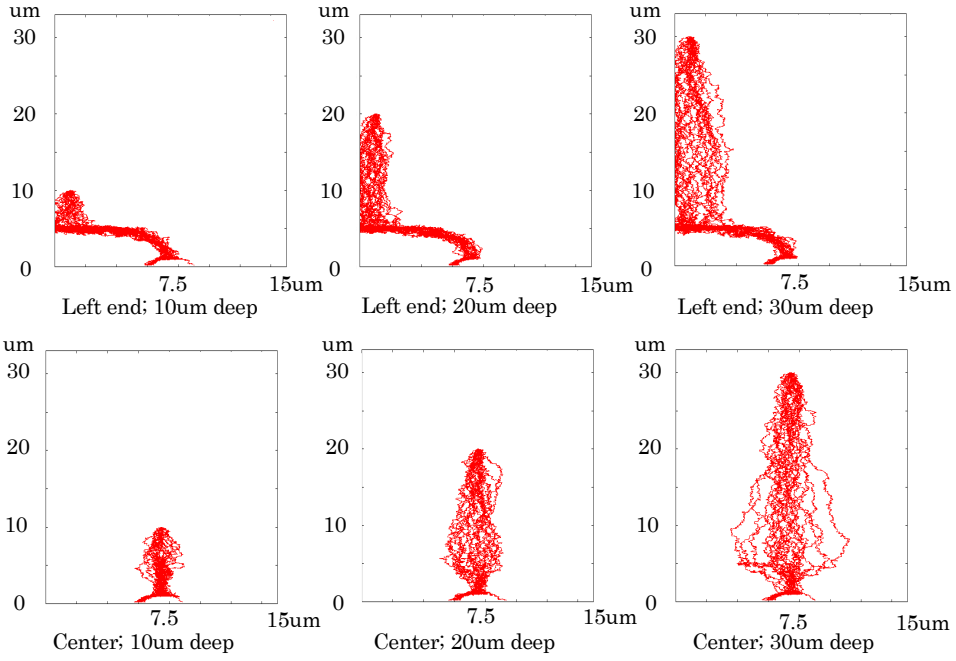
Fig. 4 Overlapped Gaussian distributions
σ: Standard Deviation; 4σ is employed in this paper; the theoretical resolution limit for a single image capture is about 2σ.

To guide incident light to the center of a pixel at the depth of 10 um or less, an effective combination of a microlens and a light guide is necessary as shown in Fig. 6. The sensor structure is seemingly similar to a conventional front-side image sensor. However, to achieve a frame rate less than 1 ns, the driver circuit must be placed very close to each pixel. So, the structure must be a BSI one with the driver chip stacked to the front side.

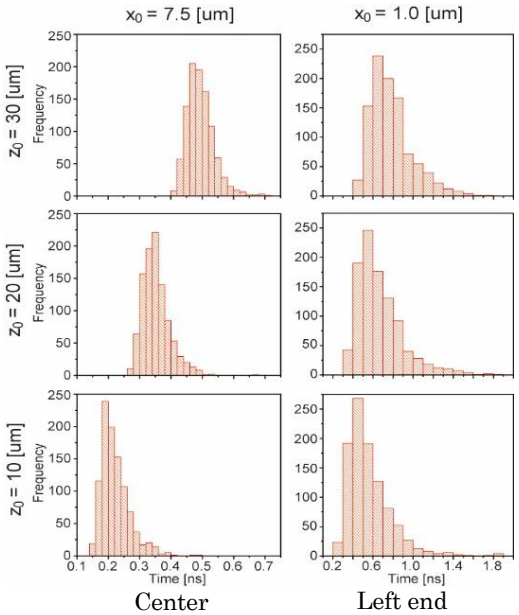
5. Operation rate vs. Functionality of the driver

The driving voltage goes around the drain gate and the multi-collection gates A1 to A6 in Fig. 2, which evoked a driver structure with a rotational motion as shown in Fig. 7. In the figure, a soliton ignited by an external trigger runs on a sash-like collection gate. A similar concept was materialized for visualization of laser fusion in U.K. An S-shaped electrode was placed behind a photoelectron conversion layer of an MCP-type image intensifier, which achieved a frame interval of 5 ps. The rotational structure can also be made with a ring-oscillator. The highest frame rate for the driver may be provided by a circuit with a ring oscillator and capacitors after each invertor to release pulsed driving voltages. However, the controllability and the functionality of these driver structures are low.

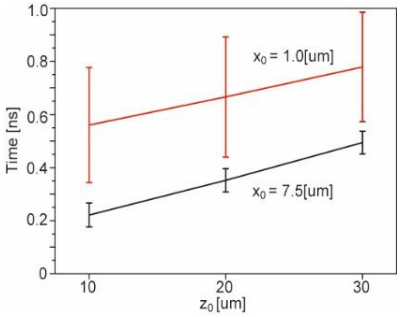
We proposed a ring oscillator with an XNOR circuit straddling each invertor and a switch before each invertor as shown in Fig. 8. We named the circuit a ROXNOR driver. When the switches are on, the ROXNOR drivers operate at the highest operation rate in synchronization by PLL circuitry. In the case, the pulse width is defined by either the response of the invertor, which depends on the bias voltage to the invertors, or the response of the XNOR circuit, which mainly depends on the output voltage to operate the collection gates. For a lower frame rate, the operation rate of the circuit is controlled by the switches. The details of the circuit is explained in the sister paper[7].



(a)



(b)



	X_0=1.0[um]	X_0=7.5[um]
Z_0=10[um]	0.56 ns (SD 0.217 ns)	0.22 ns (SD 0.0448 ns)
Z_0=20[um]	0.67 ns (SD 0.227 ns)	0.35 ns (SD 0.0434 ns)
Z_0=30[um]	0.78 ns (SD 0.206 ns)	0.49 ns (SD 0.0428 ns)

(c)

Fig. 5 Travel time distribution wrt generation sites of signal electrons
(a) Trajectories
(b) Frequency distributions
(c) Average and standard deviation σ

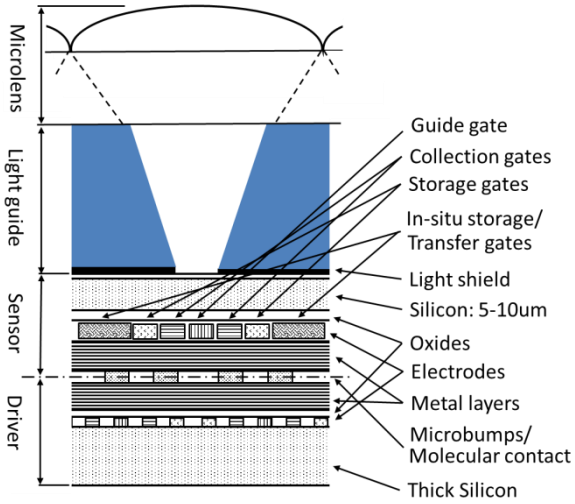


Fig. 6 A pixel of 3D-stacked BSI MCG image sensor with a microlens and a light guide

By removing S1 to S3 in Fig. 3, the temporal resolution can be reduced to less than 180 ps.

A group of pixels can be driven by a localized ROXNOR driver at about 160 ps[6), 7)].

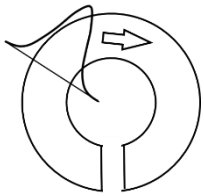


Fig. 7 An image of a rotational driver circuit

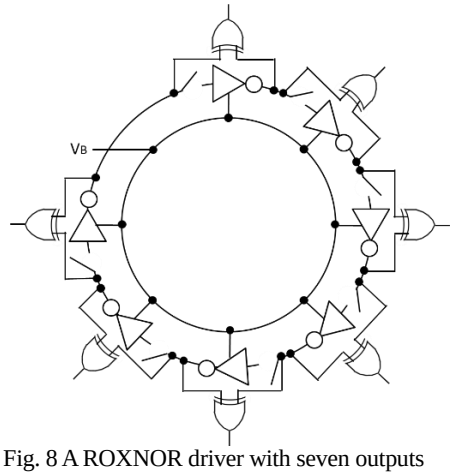


Fig. 8 A ROXNOR driver with seven outputs

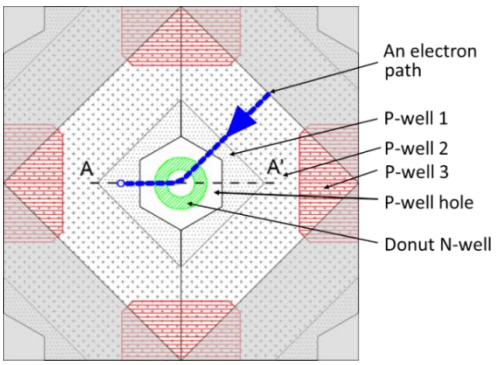
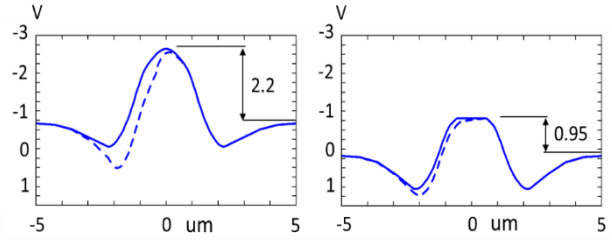


Fig. 9 P-wells of a pixel of the MCG BSI image sensor with a deep N-well

The gate layout is shown in Fig. 2. A signal electron generated at a pixel boundary can reach to A1 and, then, B1 (in the case, a storage gate) for the difference of the voltages to the collection gates dV = 0.5 V (VCH = -1.5 V to A1 and VCL = -2.0 V to A2-A6).



(a) Without a donut N-well (b) With a donut N-well

Fig. 10 Channel potential profiles along the horizontal center line near the pixel center

In these examples, a higher voltage VCH is applied to A1and VCL is applied to A2-A6 in Fig. 2. Potential depressions appear at +2 um and -2 um due to spaces between electrodes. However, in a deeper layer, the depressions are smoothed out, which guides signal electrons to a collection gate and, then, to a neighboring storage gate.

——: (a) VCH = -3.5 V, VCL = -3.5 V; (b) VCH = -1.5 V, VCL = -3.5 V (dV = 2.0 V)

– – : (a) VCH = -2.0 V, VCL = -2.0 V; (b) VCH = -1.5 V, VCL

6. Matching the sensor and the driver

Matching performance of the sensor and the driver is essential. A preliminary analysis showed that, when the MCGs are operated with the voltage swing of 3.3 V, the ROXNOR circuit drives them with the pulse width of 1.4 ns, and, when the driving voltage swing is reduced to 1.2 V, the pulse width reduces to 160 ps. To employ the 1.2-V drive, the MCG should be driven with the voltage swing of 0.5 V with a safety factor. It is achieved as shown in Figs. 9 and 10 by simply introducing a donut-shaped N-well to reduce a potential barrier at the center, enabling imaging at 6.25 Gfps (1/160 ps) with the driver. As previously stated, the temporal resolution of the sensor is less than 180 ps (1/5.56 Gfps). Introduction of the XNOR circuit and the switch to the driver slightly reduced the frame rate in compensation for the higher functionality. However, the operation rate is well matched to the temporal resolution of the sensor.

[References]

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