

A 25 Mpixel, 80fps, CMOS Imager with an In-Pixel-CDS Global Shutter Pixel

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Introduction

This paper describes a 25 megapixel global shutter imager with in-pixel-CDS capability, designed to serve various high-speed machine vision applications. High resolution sensors with global shutter [1] have been presented previously, typically with 5T pixels which enable global shutter capability but suffer from inferior noise performance and shutter efficiency. While various methods have been proposed to perform correlated double sampling in global shutter pixel architectures [2, 3, 4, 5, 6], these pixels were not previously implemented in 35mm optical formats and resolutions beyond 20 million pixels.

Combining voltage based CDS pixels, such as the in-pixel-CDS described previously [3], with high resolution, large area image arrays is not a trivial effort. Voltage based CDS pixels impose severe requirements on the pixel array supplies, control signal conditioning and timing. Not only does the 7T+2C pixel implemented here require considerably more complicated timing control than a 5T pixel, the sampling operations on the S/H capacitors in the pixel also put a severe strain on the pixel supplies and substrate. Any non-uniformity in timing or any disturbance of the substrate or the pixel supplies leads to non-uniformity, scene dependency and many other artifacts.

For this 25 Megapixel imager, the pixel was shrunk to 4.5 μ m. A pixel read-noise of less than 9e⁻ was obtained, which resulted in 12e⁻ temporal noise for the complete imager, including the ADC noise. By introducing appropriate storage node implants and dedicated photodiode integration, the global shutter efficiency was improved to 5000:1 compared to the prior work [3], despite the reduction in pixel size.

This paper describes some of the artifacts encountered during the evaluation of the early prototypes and the subsequent precautions taken to mitigate these effects in a successful 2nd cycle of learning. In the lab, making use of the flexible timing control provided by the configurable sequencer [1], timing control for the pixel has been optimized, not only to ensure uniform images, but also to avoid the black-sun artifact which was not addressed in prior work [3].

First the row patterns introduced by the global sampling of the reset values in the pixel will be discussed. The effect of slope control and rolling operations will be explained. Next an interesting dark current effect resulting from pixel and column pre-charging is revealed. Third, a solution is proposed to deal with the well-known 'black-sun' effect in the in-pixel-CDS pixel.

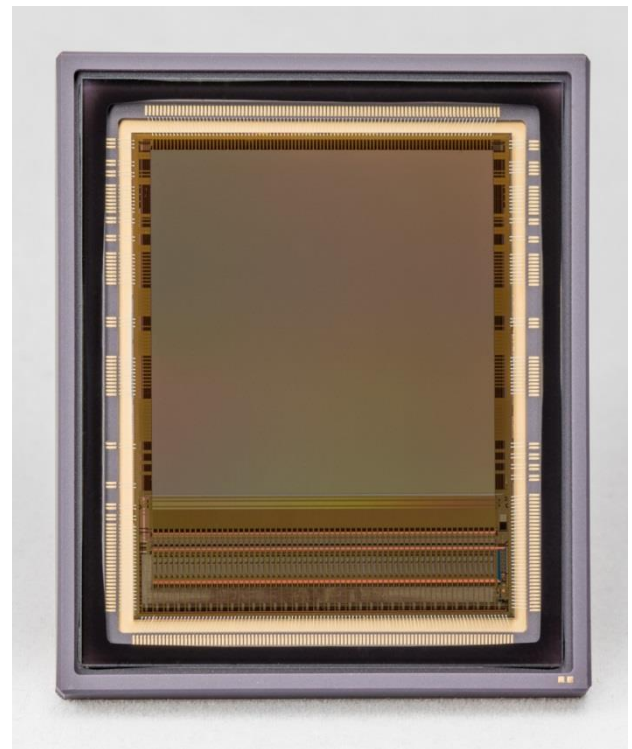


Figure 1: Sensor photograph

Pixel Reset Sampling Introduces Row FPN

For sampling of the global reset value in the S/H stage in the pixel, the AC coupled capacitor in the pixel (Figure 2) is used by turning OFF the calib switch. Prior to sampling, the capacitor is connected to Vdd through the calib-side terminal. Turning OFF the calib switch, however causes kickback on Vdd and as a result of different delays in the row drivers, every line will sample Vdd at a slightly different moment in time. This results in line-to-line offset differences which show in the image as row FPN.

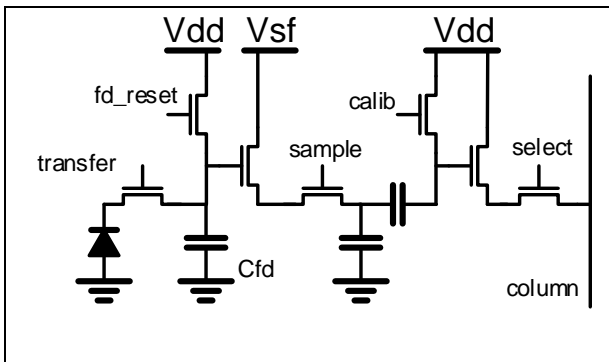


Figure 2: Pixel Schematic

This effect can be mitigated by introducing slope control on the row drivers. This both reduces the kick back on Vdd and the relative difference in timing between the drivers by spreading out the sampling operation over time.

In a simplified model (Figure 3), the slope of the row driver is determined by an NMOS current source. The NMOS current source is connected to the local substrate and as a consequence the current peaks induced during transients will cause the substrate to come up relative to the ideal ground. The severity depends on the relative distance to the nearest bondpad and the associated resistances.

Similarly, the NMOS bias voltage will initially be pulled upwards. The speed at which the NMOS source recovers depends on the resistance and hence the distance to the bondpad, while the speed at which its gate recovers depends on the distance to the current source drivers. The difference in timing results in an interesting profile as shown in Figure 4.

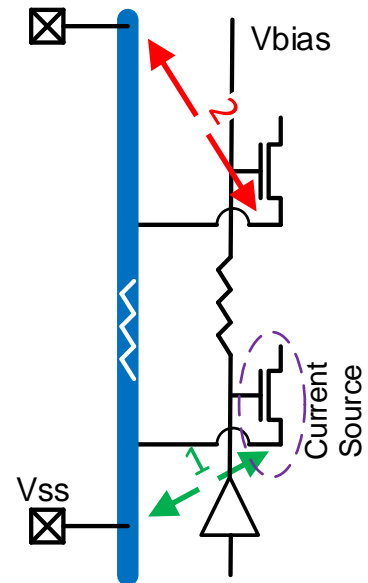


Figure 3: Simplified Row Driver Model

Around row 1500, the sensor has a bondpad and the NMOS gate and source recover at about the same rate, since the distance to the driver and the distance to the nearest pad are such that the two effects more or less cancel. It can be seen that changing the slope control has a limited impact.

Around row 3500, the row driver has another pad. The effects cancel less and the impact of the slope control is more pronounced. The problematic behaviour is located around rows 0-500. For those rows the distance to the pad is large and the distance to the driver is short. As a result the slope control has a significant impact.

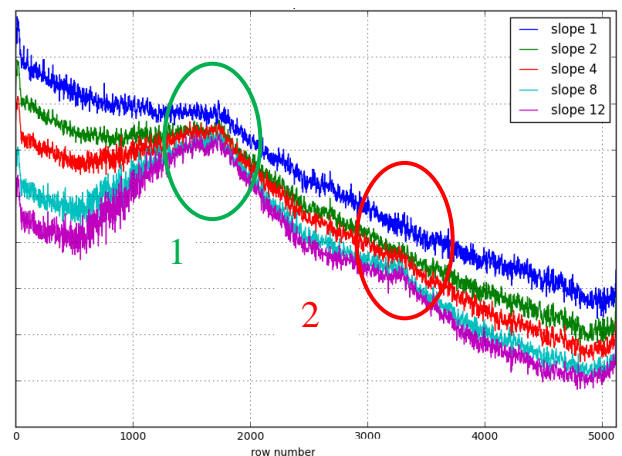


Figure 4: Row Patterns

Rolling the Global Operation

Another way to mitigate the impact of the global pixel reset is to spread the sampling in time by rolling the operation. As a traditional rolling operation would be too slow, multiple lines are still addressed at simultaneously. Making use of the flexibility designed into the row driver circuits and the sequencer, the array is virtually broken up in vertical segments of 64 lines each.

First, the first line of each segment is addressed, (line 0, 32, 64, ..) then the second line etc....

It can be seen from Figure 5 that the location dependency is removed. Since the first set of lines being addressed still suffer from a transient effect as seen in the blue curve, the 'roll' is executed twice (green curve) to remove this effect. The remaining effect is a small gradient resulting from the storage node leakage.

Since gradients are far less visually disturbing, and can be easily calibrated, this is not a concern. The smaller segments in the figure show that the effect is reproducible. Moreover, the leakage is highly uniform and largely temperature independent as a result of which, calibration is straightforward.

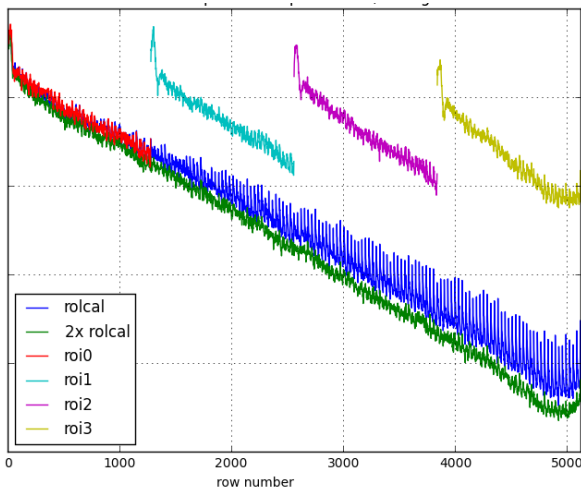


Figure 5: Row Averages

Pixel Discharge Introduces Dark Current Patterns

In order to remove memory effects on the storage node in the pixel, the storage node needs to be pulled to a low voltage (first SF can only charge 'up'). It was found that this operation, essentially pulling local diffusions to ground, injects charge in the substrate which is collected as dark current by the photo-diode. Reducing the discharge time

and/or discharging to a value slightly higher than V_{ss} mitigates the effect.

Furthermore, the column is discharged to V_{ss} on every read from the array [7]. Due to the high power consumption and large area, the substrate potential varies across the die. More in particular, within the pixel array, the substrate is slightly higher than V_{ss} . Close to the pads the columns are discharged to ground and as a result, charge is injected during every line, and is subsequently picked up by the photodiodes. This results in a dark current pattern as shown in Figure 6. The brighter columns show up where the discharge potential has the lowest resistance path to ground. Changing the discharge value to a potential slightly higher than V_{ss} , resolves the issue.

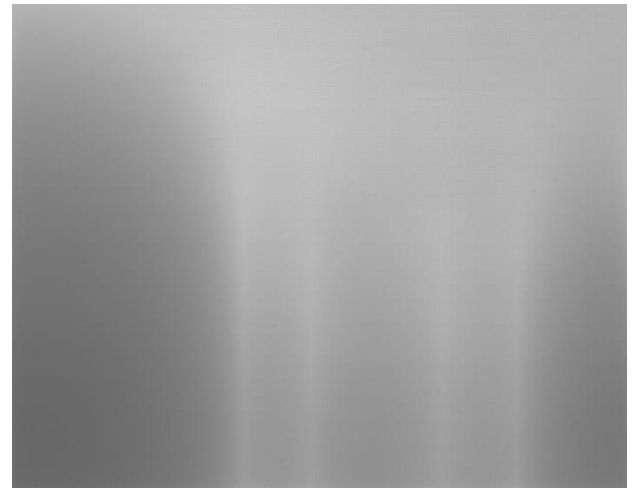


Figure 6: Dark Current Image

Black Sun

Black Sun or Reverse Saturation, is a well known effect where the pixels' response inverts at increased illumination. The typical mitigation actions applied for other pixels cannot be applied here because the "R-S" operation is implemented inside the pixel. Therefore, it is imperative to avoid R dropping too low when it gets sampled during the global operation.

This is accomplished by setting an intermediate discharge value for the storage node just before sampling the reset value as shown in Figure 7. Since the source follower can only charge upwards, this is sufficient to ensure the reset value cannot go lower than the pre-defined threshold. As can be seen from Figure 8 the proposed timing operation eliminates the reverse saturation effect completely.

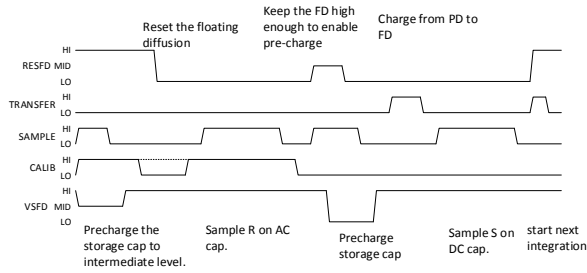


Figure 7: Anti Black Sun timing

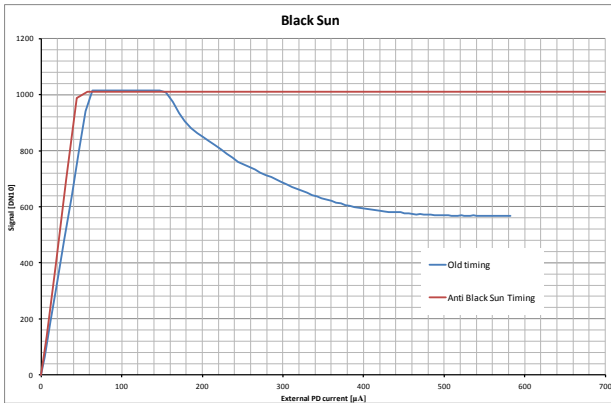


Figure 8: Oversaturation response

Summary

Global shutter effects in a high resolution CMOS sensor were discussed. Several pitfalls have been identified and possible solutions were offered to mitigate the effects of global operations on the image array. The performance characteristics of the 25 Megapixel sensor discussed in this paper are summarized in Table 1.

Table 1: Performance Summary

Resolution	5120x5120
Frame rate	80 fps
Pixel type	7T + 2C
Pixel size	4.5µm
Temporal noise	12e-
LFW	10ke-
Shutter Efficiency	5000:1
Row FPN	0.2%
PRNU	0.7%
Power Consumption	4W

[1] C. Esquenet et al., “A 26.2Mpixel, 74fps, Global Shutter CMOS Imager with 20Gb/s Interface for Multi Object Monitoring”, *IISW 2011*

[2] J. Bogaerts et al, “High Speed 36 Gbps 12Mpixel Global Pipelined Shutter CMOS Image Sensor with CDS”, *IISW2011*

[3] Y. De Wit, T. Geurts, “A Low Noise Low Power Global Shutter CMOS Pixel Having Single Readout Capability and Good Shutter Efficiency”, *IISW2011*

[4] J. Solhusvik et al., “A 1.2MP 1/3” Global Shutter CMOS Image Sensor with Pixel-Wise Automatic Gain Selection”, *IISW2011*

[5] B. Wolfs et al., “3.5 µm Global Shutter Pixel with Transistor Sharing and Correlated Double Sampling”, *IISW2013*

[6] S. Velichko et al., “Low Noise High Efficiency 3.75µm and 2.8µm Global Shutter CMOS Pixel Arrays”, *IISW2013*

[7] Bart Cremers, et al., “A 5 Megapixel, 1000fps CMOS Image Sensor with High Dynamic Range and 14-bit A/D Converter” *IISW2013*