A 14-bit, 33-Mpixel, 120-fps Image Sensor with DMOS Capacitors in 90-nm/65-nm CMOS

T. Yasue[1], K. Kitamura[1], T. Watabe[2], H. Shimamoto[1], T. Kosugi[3], T. Watanabe[3],
S. Aoyama[3], M. Monoi[4], Z. Wei[5] and S. Kawahito[5]
[1]NHK Science and Technical Research Laboratories,
1-10-11 Kinuta, Setagaya-ku, Tokyo 157-8510, JAPAN
TEL: +81-3-5494-3226, *E-mail: yasue.t-gm@nhk.or.jp*
[2]NHK Engineering System Inc., Japan,
[3]Brookman Technology, Inc., Japan
[4]Toshiba Corporation Semiconductor & Storage Products Company, Japan
[5]Shizuoka University, Japan

Abstract – **We fabricated a 33-Megapixel and 120-fps CMOS image sensor with 14-bit analog-to-digital converters (ADCs) using depletion-mode MOS (DMOS) capacitors. The DMOS capacitor has high capacitance density, whereas its capacitance depends on input voltage. Hence it has been not thought to be suitable for ADCs. We used two-stage cyclic ADC architecture with a split-sampling-capacitor method to reduce the differential non-linearity (DNL) of ADC. As a result, the fabricated image sensor exhibited a DNL of +0.95/-0.80 LSB, realizing genuine 14-bit resolution.**

1. Introduction

The emerging demand for highly realistic moving pictures is strengthening a sweeping trend for high-resolution and high-frame-rate video systems. The ITU-R has standardized video parameters for ultra high definition TV (UHDTV) [1]. The full-specification video signal stated in these international standards is prescribed to have a 7,680(H) × 4,320(V) pixel count, 120-Hz frame frequency with progressive scanning, 12-bit tone reproduction, and a wide color gamut. In this paper, a 33 Mpixel 120 fps CMOS image sensor with a 14-bit column parallel ADC is presented. In consideration of the 0.45 gamma correction determined by the standards, a 14-bit ADC is needed to generate a full-specification video signal. However, previously developed image sensors for UHDTV have up to 12-bit resolution [2-4]. The most demanding task was designing an ADC that simultaneously fulfilled the requirements for high-accuracy, high-speed operation, small layout area and low power consumption. This sensor uses a two-stage cyclic ADC with depletion-mode MOS (DMOS) and is fabricated by 90-nm/65-nm (90 nm for analog circuits including the pixel area and 65 nm for digital circuits) CMOS technology. DMOS capacitors have superior capacitance density, but are difficult to use in ADCs because of the dependence of capacitance on applied voltage. We tried to overcome this difficulty by applying the

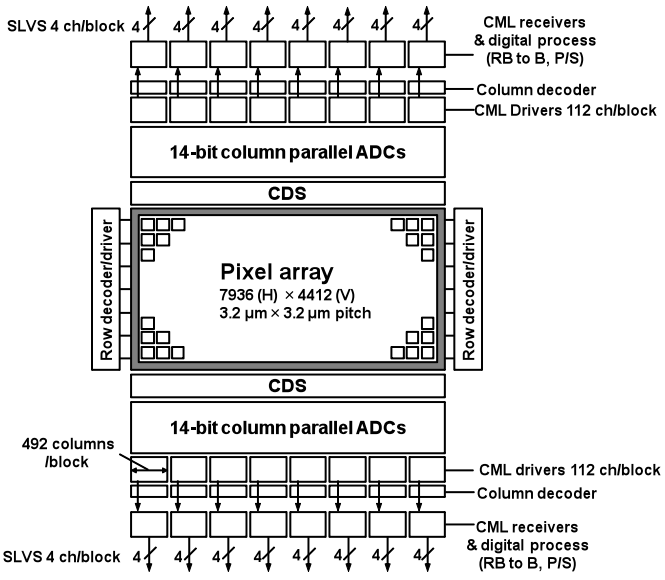

Fig.1 Block diagram

split sampling capacitor structure to the cyclic ADC.

2. Architecture of the image sensor

Fig. 1 shows a block diagram of the sensor we developed. The sensor has 7,936(H) × 4,412(V) pixels with a 3.2-μm pitch including optical black and dummy pixels. The readout circuits, (which consist of a correlated double sampling (CDS) with an analog gain amplifier, a 14-bit ADC, latches, horizontal scanners, current mode logic circuits, digital process circuits, and scalable low voltage signaling (SLVS) drivers), are located on the top and bottom of the pixel array. The column pitch is 6.4 μm. This sensor has 64 parallel 996.8-Mbps SLVS output ports to achieve an aggregate data rate of 63.8 Gbps.

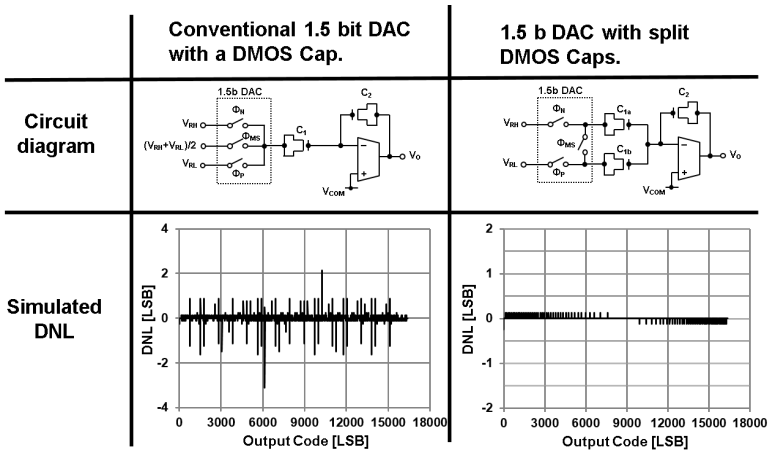

Fig.2 Circuit diagrams and simulated DNL of the 14-bit cyclic ADCs

Fig.2 compares the proposed cyclic ADC circuitry with DMOS capacitors and the conventional one, and shows simulated differential non-linearity (DNL) calculated with the input voltage dependency of the capacitance we used in this image sensor [5]. The DMOS capacitor we used for this image sensor shows 0.26 % variation in the capacitance in the input voltage range. In the conventional cyclic ADC, three reference voltages are applied to the 1.5-bit DAC. Because of the dependence of capacitance on applied voltage of DMOS, the simulation results show large DNL of +2.1/-3.1 LSB at 14-bit precision. On the other hand, the proposed ADC uses an architecture in which DMOS sampling capacitor C_1 is split into C_{1a} and C_{1b} to generate a three-state reference voltage determined by a 1.5-bit encoded feedback signal from two input voltages, V_{RH} and V_{RL}. The dependence of capacitance on applied voltage in DMOS capacitors in this spit-capacitor method causes homogeneous reference voltage error at each decision level, resulting in very small DNL of +0.125/-0.125 LSB at 14-bit precision.

We applied this new split-capacitor architecture with DMOS for a 14-bit two-stage cyclic ADC. The architecture of the two-stage cyclic ADC is shown in Fig. 3. The two-stage cyclic ADC consists of two pipelined cyclic ADCs. The pipelined and parallel operation of the two ADCs effectively reduces conversion time and power consumption. In our design, the first-stage cyclic ADC operates for five cycles, and the second stage cyclic ADC operates for nine cycles, so that an overall 14-bit resolution is obtained from the ADC.

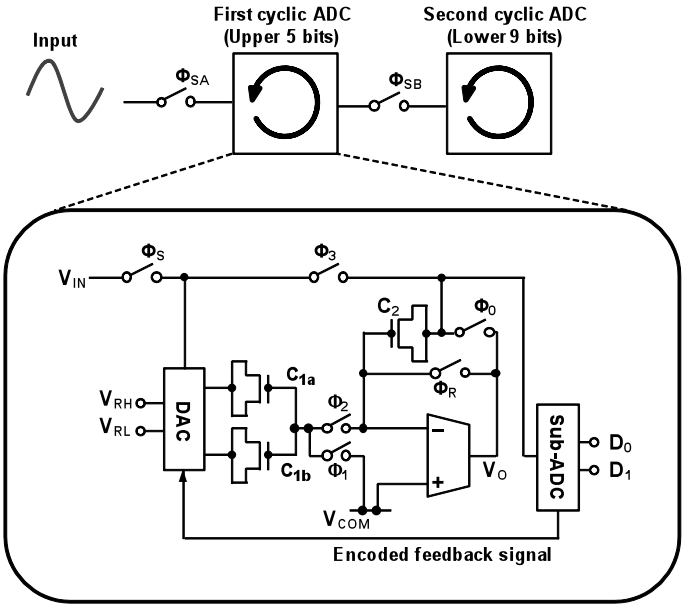

Fig.3 Architecture of the two-stage cyclic ADC with split sampling capacitor ADCs

3. Measured results

Measured DNL and integral non-linearity

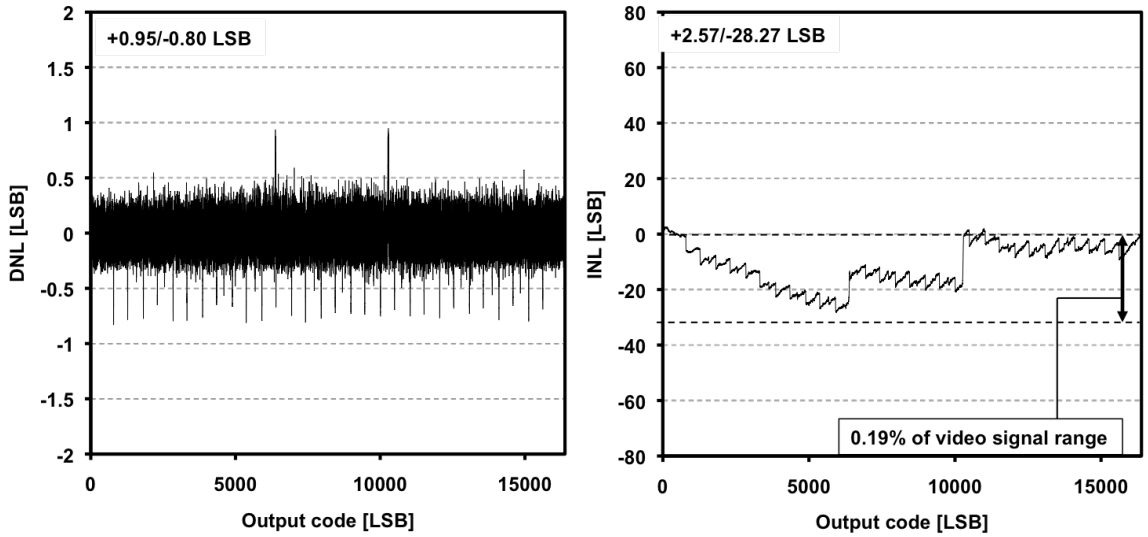

Fig.4 Measured DNL and INL of the fabricated image sensor

(INL) are shown in Fig. 4. The implemented ADC exhibits the DNL of +0.95/-0.80 LSB and the INL of +2.58/-28.27 LSB. This DNL value means there is no missing code or defection of monotonic increase in the whole ADC range. Additionally, variation of the INL is about 0.19 %, which is less than that of the in-pixel source follower. The errors, particularly the two large steps in the INL plot, can further be corrected by using digital correction circuits outside the image sensor. The DNL is more important than the INL, because missing code or a defection of monotonic increase notably degrades image quality and is difficult to correct.

The performance of the image sensor is detailed in Table 1. Thanks to 90-nm/65-nm technology, both quantum efficiency and conversion gain are increased and measured sensitivity is 3.57 V/lx-s, which is 2.3 times higher than that of a previously reported 33-Mpixel, 120-fps image sensor [2]. The conversion gain of the floating diffusion amplifier is 61 μV/e^-, and the readout noise is 5.2 e^-_{rms} under an analog gain of 3.5. The full well capacity of the photo diode is about 15,300 e^-. Consequently, the dynamic range of the sensor is about 69 dB. The total power consumption of the sensor is only 3.2 W. The adoption of SLVS and a 1.2-V power supply for the digital circuit contribute to suppress power consumption.

Process	90 nm / 65 nm 1P5M CIS
Chip size	30 mm (H) × 26 mm (V)
Power supplies	1.2 V (digital), 2.8 V/3.8 V (analog)
Number of active pixels	7680 (H) × 4320 (V)
Number of total pixels	7936 (H) × 4412 (V)
Pixel size	3.2 μm × 3.2 μm
Pixel type	2.5-Tr two-shared pixel (pinned PD)
Frame rate	120 fps (maximum)
Optical format	1.7 inch (Super 35)
ADC resolution	14 bit
ADC DNL	+0.95/-0.83 LSB
ADC INL	+2.57/-28.27 LSB
Conversion gain	61 μV/e^-
Full well capacity	15300 e^-
Sensitivity	3.57 V/lx-s
Random noise	5.2 e^-_{rms} (gain=3.5) at 120 fps
Power consumption	3.2 W at 120 fps

Table 1 Imager performance

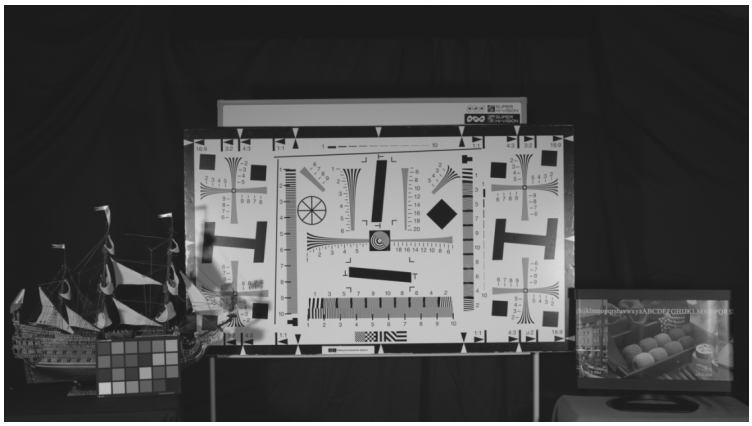

Fig.5 Captured image

Figs. 5 and 6 show an image captured from the fabricated image sensor and a die photograph, respectively. The die has dimension of 30.0mm (H) × 26.0mm (V). Owing to the adoption of DMOS and nanofabricated 90-nm/65-nm fabricating process, the layout area of the two-stage cyclic ADC was 6.4 μm(H) × 1,900 μm (V).

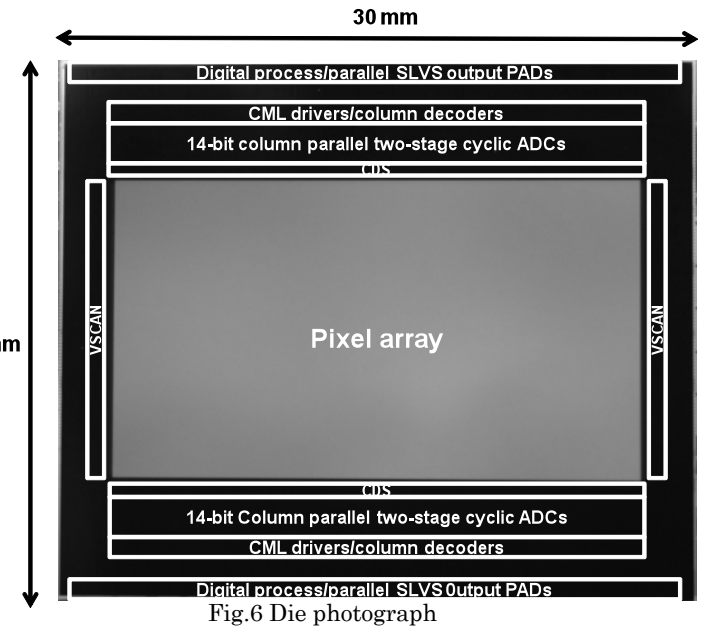

Fig.6 Die photograph

4. Conclusion

We fabricated a 33-Mpixel, 120-fps CMOS image sensor that uses 14-bit two-stage cyclic ADCs for full-specification UHDTV video. By using a split-sampling capacitor method, fabricated image sensor realizes the DNL of +0.95/-0.80 LSB in 14-bit precision with the DMOS capacitor. The measured sensitivity was 3.57 V/lx-s, which was significantly improved from our previous image sensor, while curving the increase in readout noise. Furthermore, the power consumption was as low as 3.2 W, owing to the adoption of SLVS and 1.2-V power supply for digital circuits.

Reference

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