Piece-Wise-Linear Ramp ADC for CMOS Image Sensor and Calibration Techniques

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***Abstract* – In this paper, a 10-bit digital Correlated Double Sampling (CDS) high-speed CMOS Image Sensor designed in 65nm BSI technology for a 1.1µm pixel is proposed. The readout architecture has been developed to read a 13Mpix sensor (4248 x 3216) at 55frames/s, requiring a row time of 5.5µs. The readout is based on a Piece-Wise Linear (PWL) ramp generator implementing an I/C structure. Two innovative calibration techniques for output data linearization are investigated.**

Keywords – CMOS image sensor, Piece-wise-linear ramp, Digital Correlated Double Sampling, Calibration.

I. INTRODUCTION

CMOS image sensor pixel array resolution continues to increase along with a demand for increased frame rate. In order to achieve such performances, readout performance must be improved, keeping within limits dictated by layout constraints and the power budget. Ramp ADC looks to be more suitable for small pixel than cyclic or SAR (successive Approximation Register) ADC [1] [2]. Moreover digital CDS allows to perform best-in class Vertical Fixed Pattern Noise (VFPN) as mentioned in [3]. Nevertheless there are limitations of increasing the clock frequency of the ripple counter in the case of a linear ramp ADC: power consumption can be increased, while a shorter LSB in the time domain brings a requirement for better noise performance. It has been proposed in the past to take advantages of the photon shot noise to speed up the AD conversion by using a non-linear ramp or multi-ramp multi-slope technique [4] [5] [6]. In section II the architecture used to generate a PWL ramp is described. Section III highlights the major issues related to the PWL ramp ADC. Then section IV discusses calibration techniques.

II. PWL RAMP ARCHITECTURE

The PWL ramp generator is based on an I/C architecture using an array of 11-bit thermometric current sources and a column-distributed integration capacitance (Figure 1). The latter is based on a metal fringe capacitance using M1 to M3 layers to ensure linearity. A thermometric current sources array has been preferred for linearity performance too. Among the 11-bit input data, 8-bit are dedicated to control the analogue gain from 0.25 to 16. 3 additional bits are employed to enable trimming for lot to lot mismatch of the fringe capacitances and the mismatch of the integration current. In order to ease the digital reconstruction, the ramp ratio between two consecutive segments has to be an accurate power of 2. For typical case, the ramp generator allows to generate slew rate in the range of 30mV/µs – 0.5V/µs with 1mV/µs step. As explained in [7], the use of a buffer prevents smearing issues caused by a ramp distortion when many comparators simultaneously change state. The I/C ramp generator shown in Figure 1 is controlled with the timing diagram in Figure 2. The switches SWOFFSET and SWRESET respectively allow to create an offset before starting the ramp and to reset the integration capacitance. Due to non-correlated kTC noises occurring during the reset phases, the integration capacitance has to be large enough to prevent a drop of the line noise performance.

$$\sqrt{\frac{2.k_B.T}{C}} < \frac{1}{10}.\text{Random\_Noise}$$

$$C > \frac{2.k_B.T}{\left(\frac{\text{Random\_Noise}}{10}\right)^2}$$

As the two reset phases are uncorrelated, the regulator on Figure 1 which generates the reference reset voltage needs to have a high Power Supply Rejection Ratio (PSRR) to prevent line noise. In a PWL ramp generator, distortion at the knee points has to be as low as possible to minimize the voltage range to be linearized. A fast current source such as current steering structure or the solution proposed in [8] is a good way to perform sharp knee point.

III. ADC LINEARITY

To ease the linearization processing, the ramp ratio between two consecutive segments is a power of 2. In a linear ramp ADC, it is well-known the comparator delay depends on the ramp slope (Figure 3) and is mismatched overall the ADC array. Due to the use of several segments in the PWL ramp, the comparator delay is responsible for non-constant offset over the full input range. It is why digital CDS allows to compensate only one segment of the

PWL ramp. As shown in Figure 4, digital CDS accurately linearizes the first segment corresponding to low light conditions. Nevertheless high distortion occurs at the knee points and processing has to compensate it. Assuming the use of 2 or 3 segments, the calibration technique has to be flexible enough to process the output data column by column. There are 2 major reasons: the first one is the finite bandwidth of the ramp buffer smoothing the ramp knee point; the 2nd reason is related to the modulation of the comparator delay when the PWL ramp slew rate moves from a given value to a new one. Calibration techniques must manage the data reconstruction around each knee point and column by column.

IV. CALIBRATION TECHNIQUES

Two different solutions are discussed: a first one based on an interpolation of the distortion and the second one by measuring the non-linearity through extra conversions stored in a lookup table. Recent paper discussed calibration techniques for PWL ramp ADC [9]. In the latter, a reference voltage swept step by step is used to generate a lookup table to get a linear 14-bit data. The calibration processing has been divided in 2 parts: the 1st focuses on the compensation of the linear segments to remove the offset due to the comparator delay, the 2nd focuses on compensating the non-linearity at the knee points.

The reconstruction of the linear segments with the compensation of the comparator delay can easily be implemented by using digital CDS. Indeed the output data for the 1st segment is automatically calibrated. However the calibration technique has to manage the calibration of the segments #2, #3…. The proposed idea consists of adapting the digital CDS to determine the difference of delay between slew rate #1 and other slew rates. As illustrated on Figure 5, the differential delay is extracted for grounded ADC input by using the slew rate #1 for the first ramp and the other slew rate for the second ramp. This digital data is then used by the processing to compensate the comparator delay as explained on Figure 4. Furthermore this calibration data has to be applied column by column in order to correct the delay variations due to mismatch over PVT conditions. The extracted delay is shown on Figure 7.

The compensation of the non-linearity at the knee points can be made in several ways. Two solutions were investigated: the 1st focuses on an interpolation while the 2nd solution consists of digitizing the non-linearity in a given voltage range as shown on Figure 6. A 3rd solution based on the combination of the two previous solutions can be considered.

As regards the interpolation, 3 rules have to be accounted for: The continuity between the linear segments and the interpolated segment, the continuity of the derivate and a scaling factor depending on the differential delay previously extracted. The latter includes information about the readout bandwidth responsible for the non-linearity to be compensated. For example, a polynomial fit for column to column compensation can be used. Regarding the solution based on the resistive ladder, it allows to convert the non-linearity in a short voltage range depending on the analogue gain. This conversion is performed in one or several row cycles. Before storing data in a lookup table, ADC outputs are filtered to reduce the temporal noise. Nevertheless the linearization is globally applied and consequently is sensitive to the column mismatch. Actually the two previous solutions can be merged. Indeed an interpolation can be run on the results got with the resistive ladder in order to extract the parameters of the fit (polynomial coefficients for instance).

Figure 7 shows the result of a 2-segments PWL conversion with a ratio by 4. The 4 curves correspond to the raw data, the raw with a factor 4 (and offset for continuity), then a 3-segments curve with reconstruction accounting the boundary conditions (linear segment #1 and #2, and non-linear part), and finally the reconstructed data. Figure 8 compares the DNL performance and highlights the enhancement of the linearity after calibration.

V. CONCLUSION

A 13Mpix BSI CMOS image sensor (Figure 9) implementing a PWL ramp generator based on I/C structure has been developed to evaluate the performance of linearization techniques. I/C structure allows to perform ramp generation with sharp knee points, which minimizes distortion and non-idealities before and after calibration. Moreover 5.5µs row time has been reached with DNL results after calibration exhibiting +/-0.5 LSB.

VI. REFERENCES

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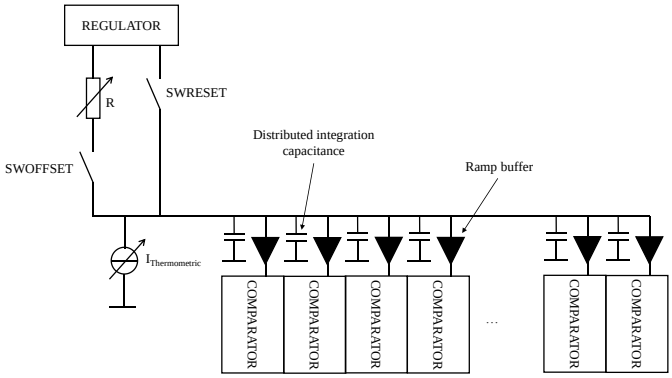

Figure 1: Schematic of the I/C ramp generator

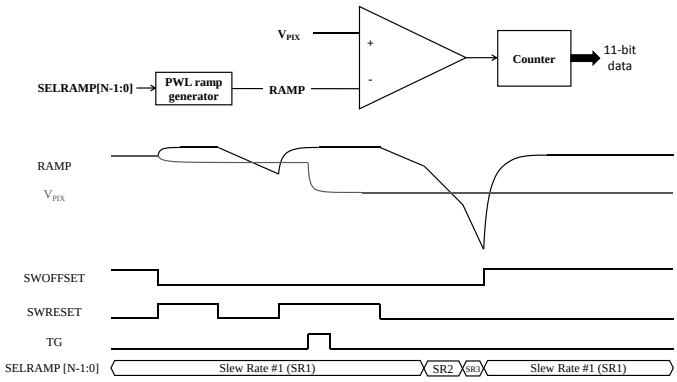

Figure 2: Timing diagram of the I/C ramp generator

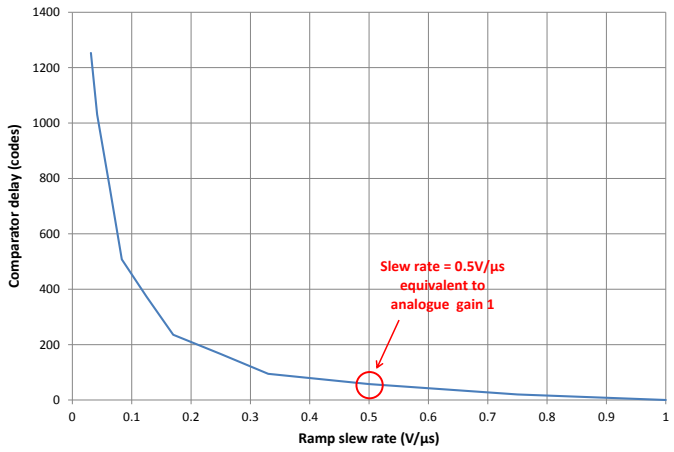

Figure 3: Comparator delay versus ramp slew rate

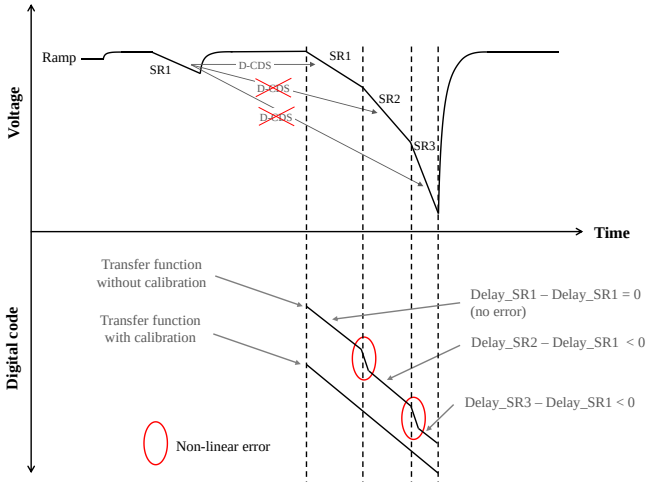

Figure 4: Conversion errors introduced by the comparator

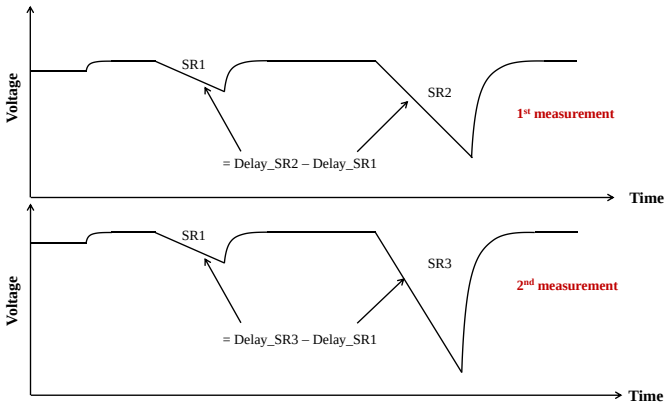

Figure 5: Additional conversions for ADC linearization with grounded ADC input

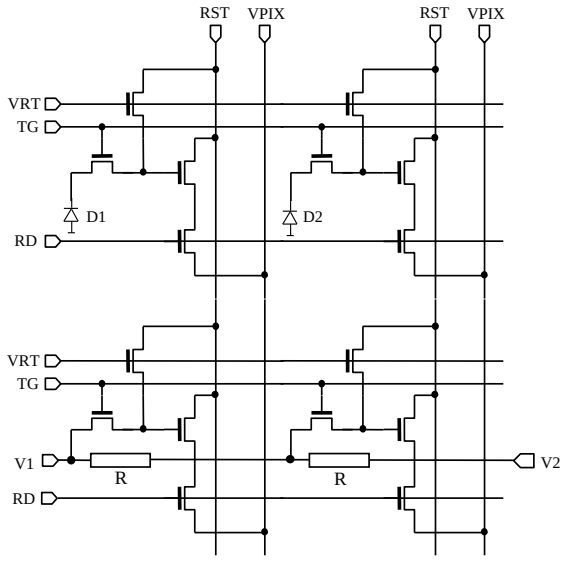

Figure 6: Dummy pixel with horizontal resistive ladder

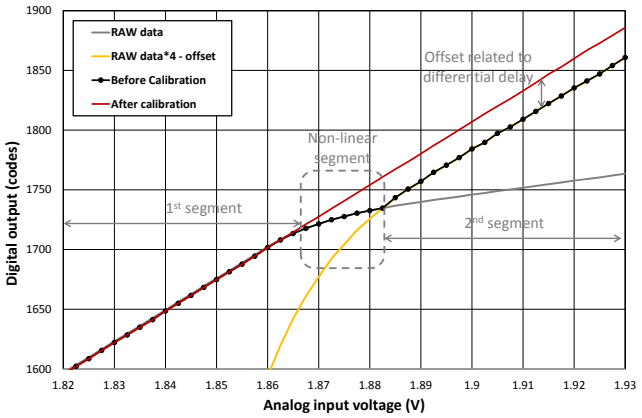

Figure 7: Data along the linearization processing (raw data, raw data x4, before and after calibration data)

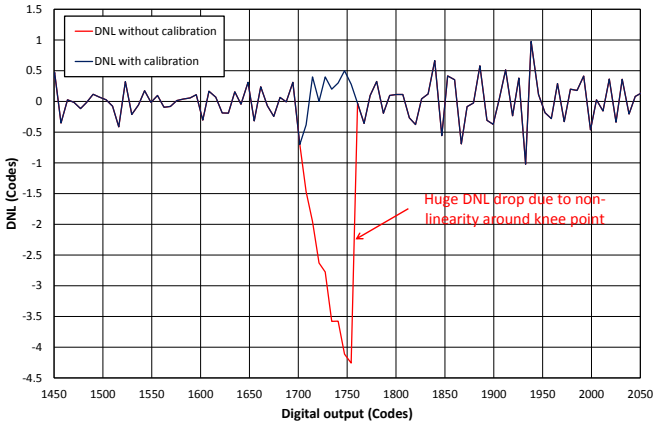

Figure 8: DNL before and after calibration

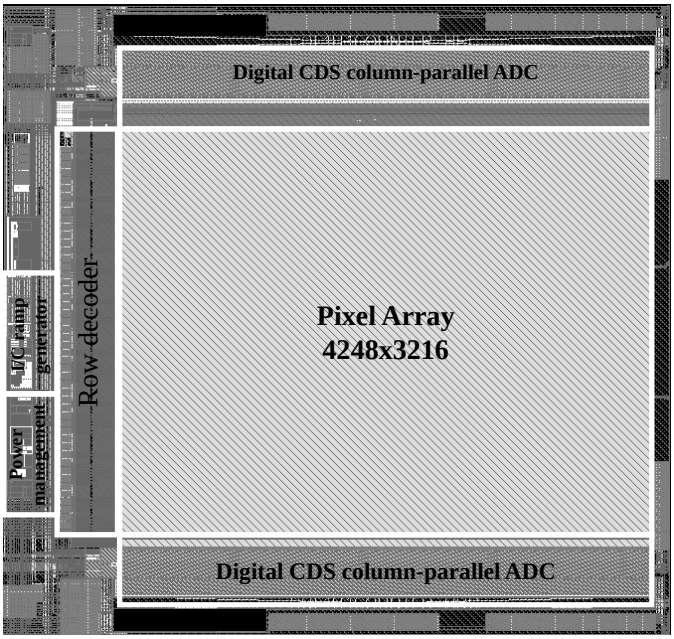

Figure 9: Chip microphotograph