

# A 305ns Conversion-Time, 13-bit All-Digital Column Analog-to-Digital Converter for CMOS Image Sensors in 180nm Technology

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**Abstract**—A new analog-to-digital converter for CMOS image sensors is proposed which utilizes multiple parallel shifted ramps and a noise-shaping gated ring oscillator (GRO). This architecture is aimed at combining high-speed, low-noise and low-power performances, simultaneously with simple and uniform global single-slope ramps. The high speed performance is achieved by the phase-delay counting of the GRO and the overlapping shift of the ramps. In order to achieve low noise, multiple single-slope ramps are applied at the comparator input to average the input noise, and a local GRO, whose phases can be memorized, is placed at the digital backend to achieve a 1st-order quantization error shaping. For 13-bit resolution, the total conversion time is 305ns in 180nm CMOS technology. Since the proposed A/D converter is mostly composed of digital circuits, it can be considered as an all-digital approach which owns better performances in more scaled CMOS technologies.

## I. Introduction

High-speed imagers are gaining more and more interests in scientific, industrial and consumer applications due to their capabilities to detect fast-moving objects. Furthermore, in consumer applications such as in smart-phones, high frame rate cameras are becoming a trend due to their capability to record slow-motion videos. The ADC is a major building block in imagers which has a great impact on the noise and on the frame rate. By using a pipelined readout method [1], the frame rate is directly proportional to the ADC speed.

In IISW 2011, it took a 12-bit pipelined cyclic column ADC 1.92 $\mu$ s to convert both the reset and signal levels of a pixel [2]. Therefore, the equivalent conversion time is 960ns. In IISW 2013, work on a 3<sup>rd</sup>-order incremental sigma delta [3] significantly improved the conversion speed by achieving a 12-bit conversion in 450ns. In addition, an amplifier is placed in every column to improve the noise performance in [2], the low noise conversion in [3] is achieved by utilizing the multiple sampling characteristics of a sigma-delta ADC.

Continuing the high-speed and low-noise trend, we propose a new analog-to-digital converter for CMOS image sensors which utilizes multiple parallel shifted ramps, phase-delay counting and the 1<sup>st</sup>-order noise-shaping property of a gated ring oscillator (GRO). The conversion speed is promised to be drastically improved by combining the two ideas of overlapping ramps and phase-delay counting. Whereas the multiple sampling effect by the multiple ramps together with the 1<sup>st</sup>-order quantization error shaping enhances the noise performance. These characteristics will be discussed in details in following sections.

## II. Multiple Single-Slope Sampling Conversion

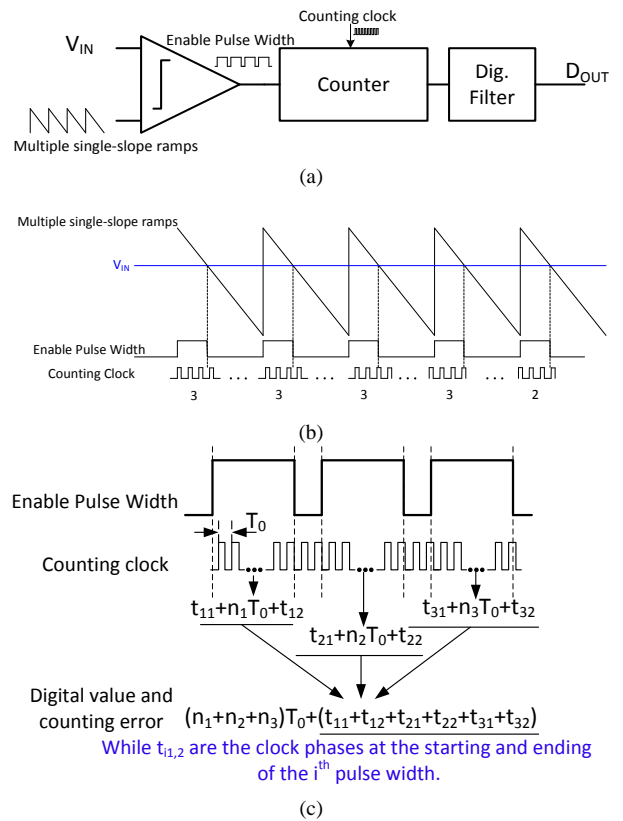


Fig. 1(a) Conventional multiple single-slope sampling conversion block diagram, (b) multiple single-slope sampling timing diagram, and (c) accumulated counting errors.

Fig. 1(a) shows the basic block diagram of the conventional multiple single-slope sampling conversion, in which multiple ramps are applied to the comparator input to average the input temporal noise [4]. The global multiple single-slope ramps are compared with the pixel output voltage  $V_{IN}$  to generate a series of enable pulse widths at the output of the comparator. Then, the counter digitizes those pulse widths by a counting clock. Fig. 1(b) shows the timing diagram of the conventional multiple single-slope sampling conversion in Fig. 1(a). The digital result representing the input  $V_{IN}$  after the conversion is the sum of all the digital values of the pulse widths. As shown in Fig. 1(c), while the digital output value is determined as  $(n_1+n_2+n_3)$  the counting errors are accumulated as  $(t_{11}+t_{12}+t_{21}+t_{22}+t_{31}+t_{32})$ , where  $n_i$  is the

counting value of the  $i^{\text{th}}$  pulse width, and  $t_{i1}$ ,  $t_{i2}$  are the starting and stopping phase errors in the  $i^{\text{th}}$  pulse width, respectively. Since these errors by the counting during the pulse widths are correlated with each other because the pulse widths are almost at the same size and are periodically repeated, the final quantization error after the digital filtering is rather the accumulation of these counting errors than the average of them. Therefore, the overall counting error is not suppressed and the ADC resolution is not significantly increased as the number of single-slope ramps is increased. As a result, only the input thermal noise of the ADC is reduced in this method.

### III. Noise-shaping Counting Principle

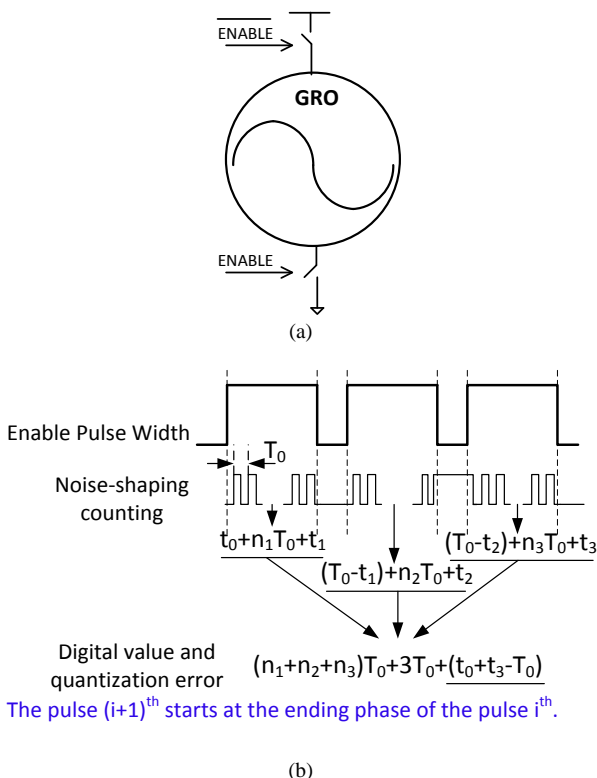


Fig.2 (a) Block diagram of a gated ring oscillator with enable/disable option, (b) Noise shaping counting principle for the quantization error by memorized phase.

In the conventional single-slope ramp A/D conversion, a global reference clock is used as the counting clock. Therefore, it is quite difficult to achieve a very high counting speed because of the challenges in the clock distribution system over thousands of columns. That's why a column-level gated ring oscillator (GRO) is a high speed approach which is free from such a complicated clock distribution system. On the other hand, if the counting GRO is dedicated to each column ADC, its phases can be easily utilized for counting purpose, which promises to boost up the conversion speed. This property will be discussed in the next section. In this section, another useful characteristic named as the 1<sup>st</sup>-order counting error shaping of a column-level GRO is discussed.

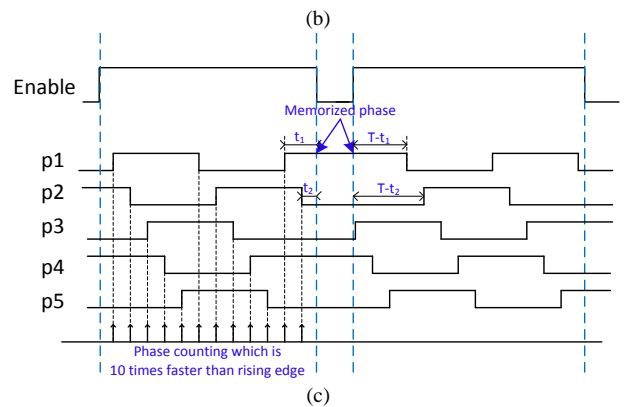
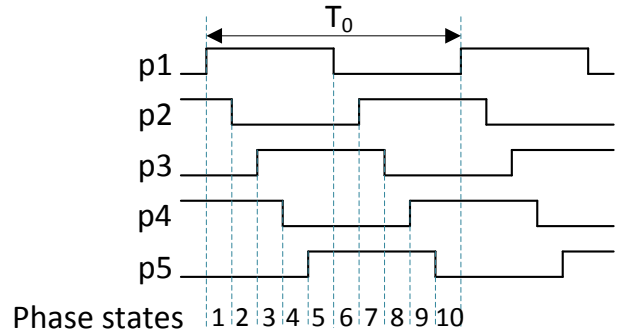
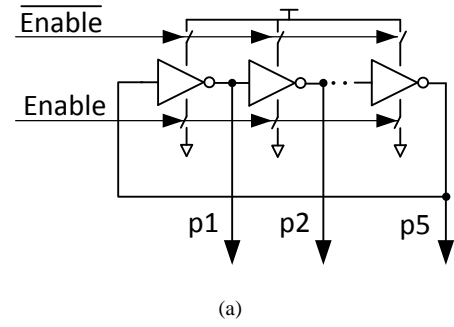


Fig.3 (a) A 5-delay-stage GRO, (b) Phase states within one period of the GRO to increase the conversion speed 10-time faster, and (c) Noise shaping principle for the quantization error by memorized phase counting.

Fig. 2 (a) shows the block diagram of a gated ring oscillator with the enable/disable pulse control, which is equivalent to the enable pulse width in Fig. 1 (b), and Fig. 2 (b). It means that, instead of feeding the pulse widths to the counter as shown in Fig. 1 (a), these pulse widths take part as the GRO enable/disable pulse. The GRO enable/disable principle is simple that, by connecting the GRO with the power supply and ground, the GRO oscillates, and by disconnecting the GRO from the power and ground, the GRO phases stop and freeze there until the moment the GRO is connected to the power and ground again. This phase memorizing property is because of that if the GRO is disconnected from the power and ground, there is no charging or discharging action changing the phases of the GRO nodes, and when the GRO is connected to power and ground, the GRO starts oscillating again from the frozen phases before [5]. Since the phase starts at the

memorized phase of the former enable pulse, there is no accumulation of phase counting errors as in Fig. 1 (c).

Fig. 2 (b) shows the timing diagram of the noise shaping counting principle by the phase memorizing property. Since the GRO phase of next pulse width starts at the stopped phase of the former pulse width, the total phase error after multiple pulses will be subtracted to each other and the final phase counting errors is determined as  $(t_0+t_3-T_0)$  after 3 consecutive pulse widths, and as  $(t_0+t_N-T_0)$  after N consecutive pulse widths, where  $t_0$  is the starting phase error of the 1<sup>st</sup> pulse width counting, and  $t_3$ ,  $t_N$  are the stopping phase errors of the 3<sup>rd</sup> and the N<sup>th</sup> pulse widths, respectively. Both of these values are in the scale of the single pulse width counting error. Therefore, a 1<sup>st</sup>-order phase counting error shaping is achieved, or in other words, not only is the thermal noise averaged, but also the quantization noise is suppressed as well with this noise-shaping counting principle.

#### IV. Phase Counting Principle

In order to achieve a very high speed conversion, another counting type, rather than the conventional rising/falling edge counting, is utilized. Since a GRO consists of multiple delay stages whose outputs generate many phases. And these phase values are to compose phase states of the GRO. If these phase states are used for counting in stead of the rising edge of any GRO node, the speed is promised to be much increased.

Fig. 3 (a) shows a 5-delay-stage GRO with the enable/disable option. Fig. 3 (b) shows the phase behavior of 5 GRO nodes (p1, p2, p3, p4, p5) in Fig. 3 (a). It is clearly shown that, within one clock cycle  $T_0$  of the GRO frequency, there are 10 phase states. If these 10 phase states are utilized for counting rather than one single rising edge with period of  $T_0$ , the conversion speed can be 10-time faster with the same GRO power consumption.

Additionally, Fig. 3 (c) shows in detail how the speed is improved by utilizing both the GRO phase counting and the 1<sup>st</sup>-order noise shaping property explained in Fig. 2 (b). If a phase delay is 195ps, each single-slope ramp lasting for 200ns will be equivalent to a 10-bit resolution. Therefore, for this phase-delay counting method, it takes 1.6us in order to achieve 13-bit resolution, while such 13-bit conversion is estimated to last for 16us if a 512MHz global counting clock is used. The frequency of 512MHz is equivalent to the rising edge period  $T_0$  of the above 5-delay-stage GRO. It can be easily realized that the conversion speed promises to be improved with more advanced CMOS technologies, in which phase delay can be implemented to be some 10ps and even less.

Fig. 4 shows the block diagram of a multiple single-slope ramp A/D converter utilizing 1<sup>st</sup>-order noise-shaping GRO. The comparator part is similar to that in the block diagram in Fig. 1 (a). Whereas the Time Distributor block in Fig. 4 generates the enable/disable pulses of the GRO. In order to count based on the GRO phases, the most straightforward way is to count the rising edges of every GRO node as in Fig. 4. However, this approach is very power and area inefficient. A

possible method is to use only one counter as the coarse counter to count a certain GRO node, and the phase delay states are captured by registers and detected by a phase state logic.

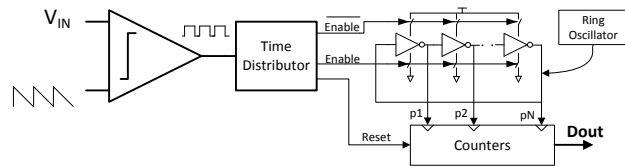


Fig. 4 Block diagram of a multiple single-slope phase-delay counting A/D converter utilizing 1<sup>st</sup>-order noise-shaping GRO.

#### V. Multiple Parallel Shifted Ramps

Although the phase-delay counting increases the conversion speed 10 times faster than the rising-edge counting, the conversion time value of 1.6us for 13-bit resolution is not the desired value. Therefore, the idea of multiple parallel shifted ramps is proposed to achieve a faster conversion. Fig. 5 shows the timing diagram of two cases, the one on the top is the multiple single-slope phase-delay counting explained above, and the one below is the idea of multiple parallel shifted ramps to achieve the conversion time value of 305ns for 13-bit resolution. For the case on the top, each single ramp last for 200ns, which is equivalent to a 10-bit resolution if the delay value is 195ps. In order to achieve a 13-bit conversion, this ramp should be repeated 8 times and the total conversion time is 1.6us.

It can be easily realized that, in the proposed multiple parallel shifted ramp idea, 8 ramps are compressed in the way that they overlaps each other. These ramps are arranged with 15ns timing distances from a ramp to the next one. The timing of 15ns here is twice the period of the global reference clock. As a result, the total conversion time for 13-bit resolution is reduced to 305ns.

Differently from the case of non-overlapping ramps on the top, where the digital output value can be easily determined by  $(N_1+N_2+...+N_8)$ , in the proposed idea, since the ramps are overlapped, the digital output calculation is a little more complicated. As clearly shown in Fig. 5, the digital output value of  $V_{IN}$  can be determined as  $(D_1+D_2+...+D_8-d_1-d_2-...-d_8)$ , where  $d_1, d_2, ..., d_8$  are the phase-delay-counting values of the small generated pulse widths, and  $D_1, D_2, ..., D_8$  are the phase-delay-counting values of a number of the slow reference clock periods. Usually, we have  $D_1=D_2=...=D_8$ , thus, for simplicity, only  $D_1$  is mentioned here.  $D_1$  is the digitized timing from the starting point of the 1<sup>st</sup> ramp to the first rising/falling edge of the slow reference clock right after the moment the 1<sup>st</sup> ramp crosses the input voltage  $V_{IN}$  level. The rising or falling edge is selected to make sure that the widths of these generated pulses are not too narrow. One simple method to match  $D_1$  and  $d_i$  values is to lock the frequency and phases of the fast GRO with the slow reference clock. The locking operation can be handled by a delay-locked loop (DLL) at the beginning of some consecutive conversion periods. The parallel ramps need to be calibrated in order to make sure their slopes not to vary much to each other. Since the ramp

non-ideality is a global issue rather than a column-level one, the errors caused by ramps can be easily calibrated by doing conversions of reference levels before the real conversions.

Additionally, from Fig. 5, it can be easily realized that the GRO is enabled in narrow pulse widths, which are all smaller than one slow reference clock period. Therefore, the maximum GRO enable time is  $8T_{SL}$ , where  $T_{SL}$  is the slow reference clock period, whose value is supposed to be 7.5ns. Therefore, during the conversion time of 305ns, GRO is enabled in 60ns at most, which is equivalent to 20%. That's how the power is saved with the multiple parallel shifted ramp idea.

## VI. Conclusions

A novel ADC with multiple parallel shifted ramps has been proposed for high-speed and low-noise imagers. By using phase-delay counting rather than rising/falling edge counting, the counting speed is improved by a factor of 10. In addition, by the multiple parallel shifted ramp idea, a very high conversion speed of 305ns for a 13-bit conversion can be achieved. The proposed ADC has the capability to reduce the thermal noise of the pixel source follower and that of the ADC itself due to the averaging effect of the multiple ramps. The quantization noise is 1<sup>st</sup>-order shaped to enhance a high resolution conversion as well. Furthermore, the generated narrow enable-pulse widths keep the GRO deactivated for more than 80% of

the total conversion time reducing the power consumption. Since the only analog component of the proposed A/D converter is the comparator's input amplifier, this architecture is mostly digital, allowing for even better performance in more scaled CMOS technology.

## Acknowledgment

This work has been supported by the IWT HiPerCim project.

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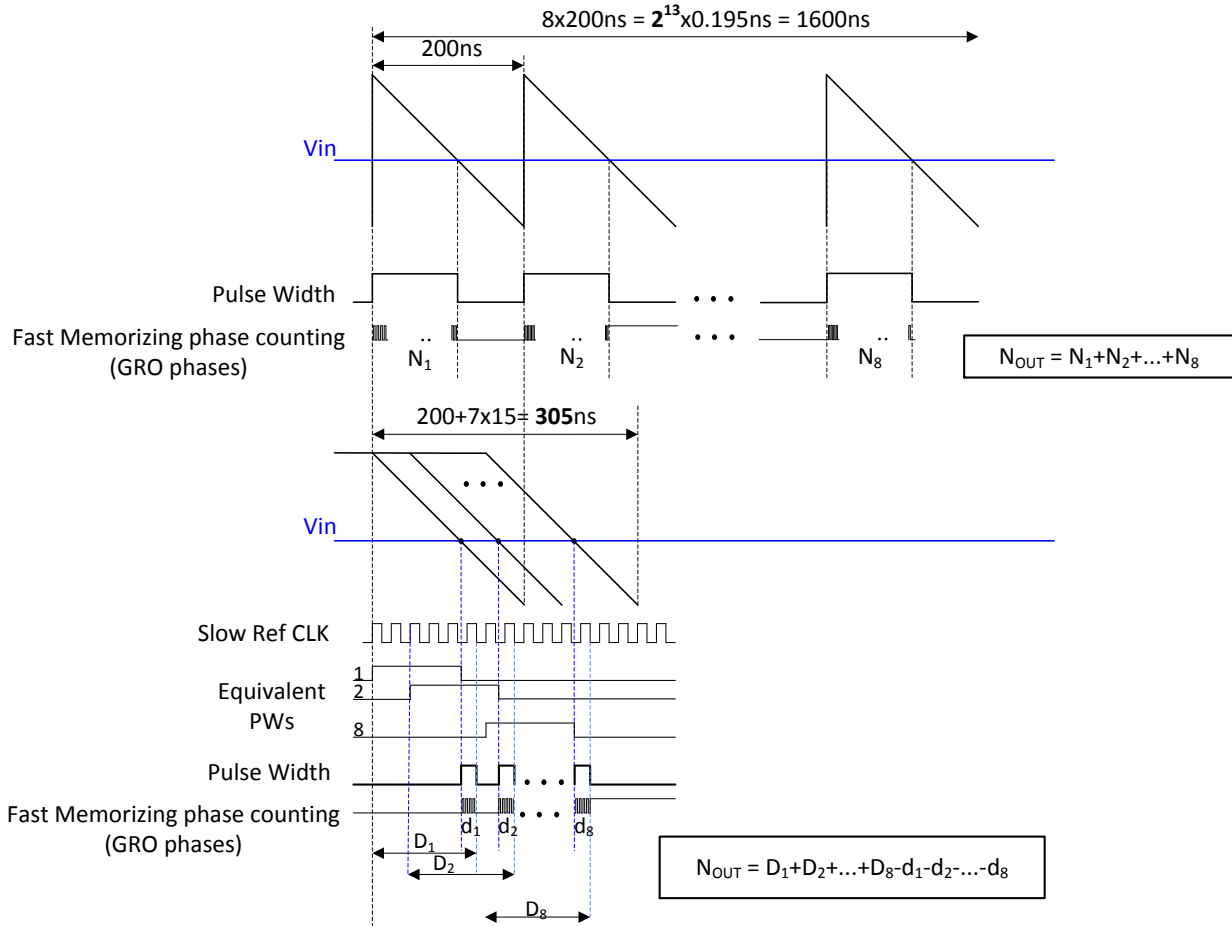


Fig. 5 The Multiple Parallel Shifted Ramp Idea Timing Diagram