High-Speed, High Sensitivity 25 Mega Pixel CMOS Image Sensor with Column Parallel 12 bit Hybrid ADC Architecture

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Abstract – **A high-speed, high sensitivity 1/2.1-inch 25 Mega pixel (5760x4320) Back Side Illuminated (BSI) CMOS image sensor with column parallel 12bit ADC is developed. Hybrid ADC architecture with SAR/RAMP is adopted for 46frames/s at full resolution and 4.85us row timing. The FD (Floating Diffusion) boosting readout is achieved by TX (Transfer Gate) high coupling. Such TX-coupled FD readout allows 4100e$^-$ of linear full well and 5.3e$^-$/second of dark current. The CDS (Correlated Double Sampling) is integrated twice, before and after column parallel ADC, in order to mitigate the noise, including structural noises. The readout noises are 3.7e$^-_{rms}$ at 1x analog gain and 2.2e$^-_{rms}$ at 8x analog gain. No visible structural noise is observed. The power consumption is optimized through circuit optimization and dynamic power management of clock gating. In the full resolution (5760x4320), the power consumption is 685mW at 46frames/second and 550mW at 30frames/second. 16 output interface lanes are implemented for the high speed frame rate. The sensor has been fabricated and being sampled.**

I. INTRODUCTION

As outdoor activities and sports activities become a part of our daily routine, a camera that can capture a fast moving motion is highly required. Not only the still image capture, but also video capture is an important aspect for high speed applications. In order to address the limitation of image blur and motion distortion in such applications, a high speed and high sensitivity image sensor becomes essential. The column parallel pixel readout of CMOS image sensor allows such applications with good noise performance and low power consumption. With the increased resolution and speed, the readout architecture needs to be revisited to overcome the limitations.

This paper presents a high-speed, high sensitivity 1/2.1-inch 25 Mega pixel (5760x4320) Back Side Illuminated (BSI) CMOS image sensor with column parallel 12bit ADC's. Hybrid ADC architecture with combined SAR/RAMP is used for 4.85uS row timing and power optimization. We present the design highlights and results of performance measurement of the product in the following order: in Section II, the sensor architecture, operation and circuitry are presented, in Section III, the measurement results of the pixel and circuitry are described, and in Section IV, the conclusion of the paper is presented.

II. SENSOR IMPLEMENTATION

The image sensor is packaged with iBGA^{TM} (imager Ball Grid Array) as shown in Figure 1. The total 121 pins are assigned in the package, but most of them are configured as power connections for optimal thermal management. The package size is 11x11mm^2 and the die size is 8.41x9.3mm^2. The metal shield along with blue CFA covers the non-active pixel array area for efficient blockage of light.

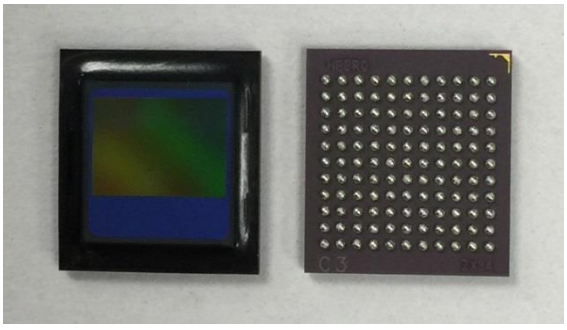

Figure 1 – Image Sensor in iBGA package

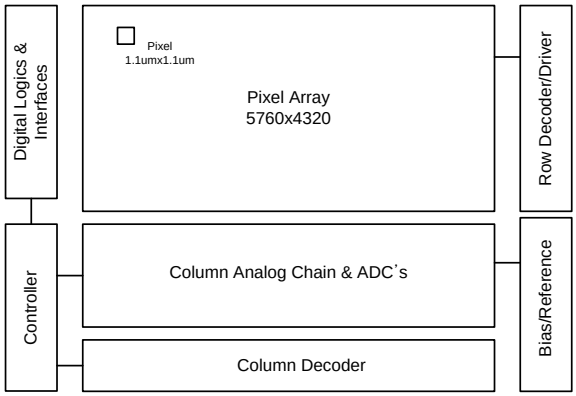

Figure 2 - Block Diagram of the sensor

The overview of the block diagram is shown in Figure 2. The image sensor consists of a 5760x4320 pixel array, row decoder/drivers, column parallel analog gain/ADCs & column decoder, bias/reference generator, digital logic control and serial interfaces. The column parallel analog chain contains SF pixout block, programmable gain amplifier, hybrid SAR/RAMP ADC and column memory, as shown in Figure 3. The programmable gain amplifier is the switched capacitor amplifier, whose gain can be adjusted by the ratio of the input and feedback capacitors. The column memory is the customized memory located per column to store the digital data from the column parallel ADC and ready for serial transfer from the column blocks to the digital logic block. Additional blocks and switches are located in the column in order to assist sub-sampling modes and noise reduction operation. There are also control digital buffers, bias analog buffers and ramp generator outside the column.

The main block of the analog column circuitry is the hybrid SAR/RAMP ADC. The concept of the hybrid SAR/RAMP ADC is illustrated in Figure 4.

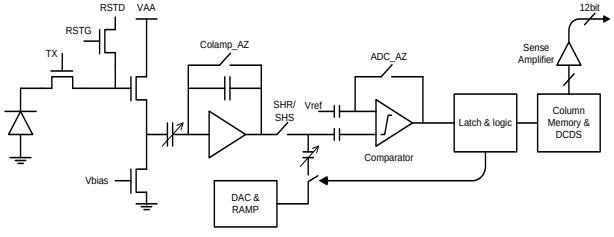

Figure 3 - Column Parallel Analog Chain

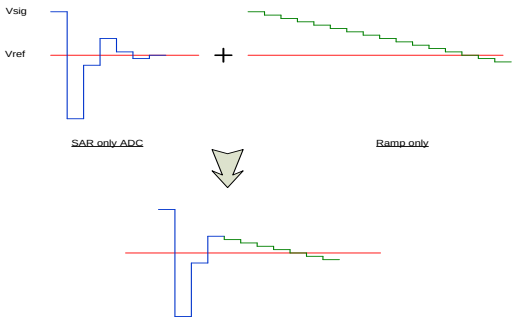

Figure 4 - ADC Architecture with SAR/RAMP

First, the SAR converts the input signals for upper bit portions, and then the RAMP converts the lower bit portions. The SAR conversion benefits with the conversion time and speed, especially with 12bit conversion. The RAMP conversion benefits with tolerance of accuracy along with CDS. In order to address the offset between the SAR and the RAMP stages, the over-range conversion of the RAMP is adopted. Extra bit counts for the RAMP conversion is used to correct the potential offset between the stages. This division of the SAR and RAMP conversion portion can be dependent on the speed and the power for the applications. For this particular implementation, 6bit SAR and 5bit (7bit) RAMP conversions are used respectively for 10bit (12bit) mode operations. The two ADC conversions are required for the digital correlated double sampling (DCDS). The CDS is integrated twice, before and after column parallel ADC, in order to mitigate the noise, including structural noises. The subtraction of data in the DCDS occurs in the column memory to optimize the analog area by reducing one set of readout memories.

In order to achieve the high speed of 46fps with full resolution, the row timing needs to be

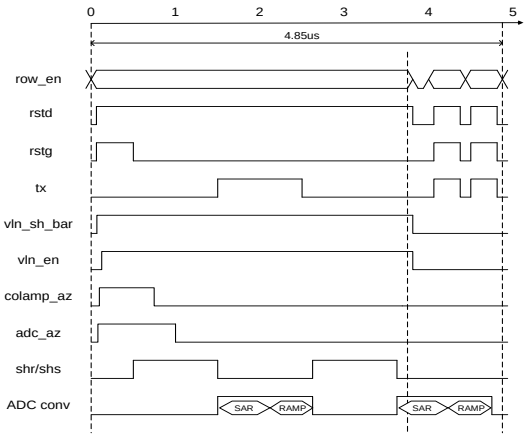

Figure 5 – Row Timing Diagram

optimized carefully. During the 4.85uS of row timing (Figure 5), two ADC conversions for SHR and SHS occur in parallel with pixel signal settling, analog gain, pixel signal transfer and even with two pixel shutters. Each ADC conversion consists of SAR and RAMP conversions after SHR/SHS sampling for reset and signal data. With the overlapped operations, the layout needs to be addressed carefully to minimize the coupling capacitances between the block and routings.

In order to permit the high resolution and frame rate operation, the digital data processing also embraces the slicing concept of parallel processing architecture. At every clock cycle, 8 pixels from the image sensor are preprocessed through digital correction block for noise reduction, or enhancing the signal level with digital gain. 8 pixels output from digital correction block are grouped into 4 slices with 2 pixels per slice. These 4 slices are processed in parallel to correct the bad pixels, lens shading effect or define the final display window by image scaling. To maintain the high speed throughput, the output image is transferred through MIPI interface on 8 lanes with bandwidth of 1.2 Gbps per lane or HISPI^{TM} interface on 16 lanes with bandwidth of 1 Gbps per lane.

Various sub-sampling modes such as horizontal and vertical skipping/binning (i.e. 2x2 and 3x3) are implemented in analog and digital domains. In the analog domain, the sub-sampling modes are supported by pixel summing, source follower binning and column amplifier binning.

The pixels are conventional 4T active pixel sensor, but without Row Select (RS). The pixel selections are made by controlling the FD level through RST transistor with RSTG and RSTD. A pixel operation using FD boosting readout was introduced. The FD boosting readout is achieved by TX high coupling without additional elements. Such TX- coupled FD readout allows more increase of FW capacity even if PD pinning voltage is higher than FD minimum voltage, which is in correspondence with FD voltage when PD electrons are fully transferred into FD after TX toggling.

	Unit	
Read Noise @1x analog gain	e-	3.7
Read Noise @8x analog gain	e-	2.2
Linear Full Well	e-	4100
Dark Current	e-/s @60C	5.3
Sensitivity	e-/lux.sec	3700
Conversion Gain	uV/e-	128
Power Supply Voltage	V	2.6, 1.8, 1.14
Pixel Array Size		5760x4320
Max. Frame Rate	fps	46
Power Consumption	mW@46fps	685
	mw@30fps	550

Figure 6 – Table of Measurements

III. RESULTS

The high linear full well capacity (4.1Ke-) and low dark current (5e-/s at 60C) are achieved with the TX coupled FD boosting. The main chip characteristics are summarized in Figure 6. The measurements were collected with the chip operating at 46frames/s (internal clock at 170 MHz) and ADC running with 10b accuracy. The readout noises are 3.7e-$_{rms}$ at 1x analog gain and 2.2e-$_{rms}$ at 8x analog gain. No visible structural noise was observed. The power consumption is optimized through circuit optimization and dynamic power management of clock gating. In the full resolution (5760x4320), the power consumption is 685mW at 46frames/s and 550mW at 30frames/s.

The die micrograph is shown in Figure 7. The active imaging region is 6.3mm(H)x4.8mm(V), compatible with 1/2.1-inch optical format. A sample image at

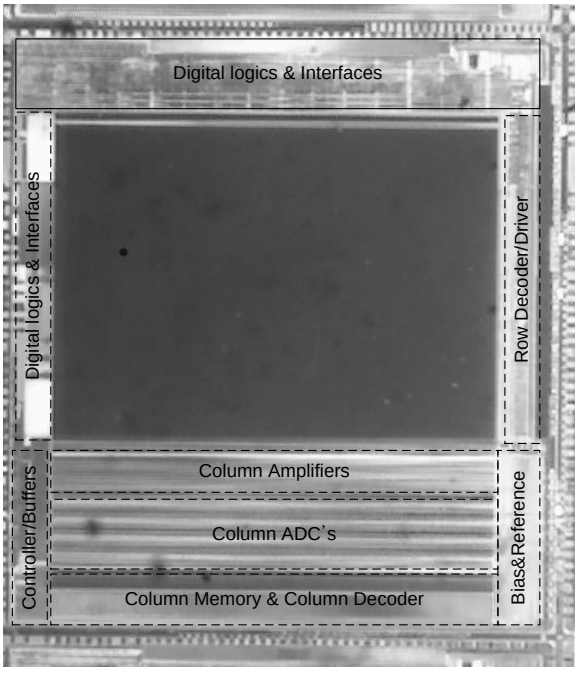

Figure 7 - Die Micrograph

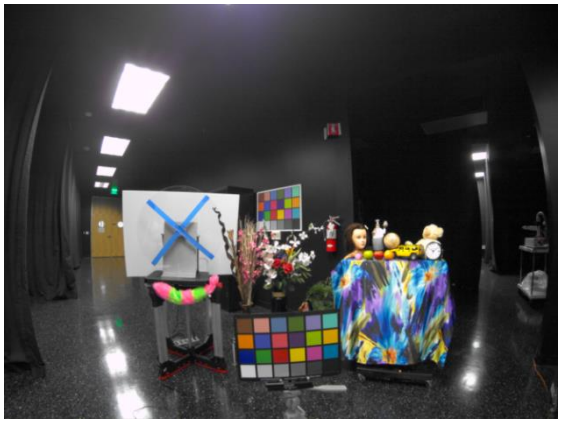

Figure 8 – Sample Image with wide angle lens. 25Mp with 46fps

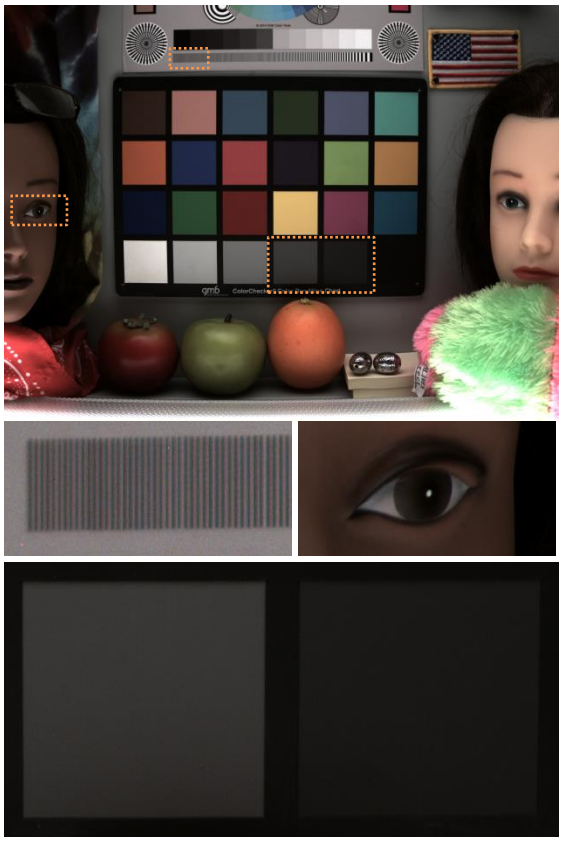

Figure 9 – Sample Image at 130lux. Magnified views: (1) Resolution test, (2) Eye, (3) Macbeth charts with N5 and N3.5 patches

46frames/s with 10 bit is shown in Figure8. It is with wide angle lens for the action camera applications. Figure 9 shows a sample image at 130lux with X1 gain and 120ms integration time. As shown in the magnified views of Figure 9, the details of the resolution are well kept. With Macbeth chart N5 and N3.5 patches, the noise performance is illustrated. Along with various conditions in the scene, the image quality with the high speed was well maintained.

IV. CONCLUSIONS

We presented a 1/2.1-inch, 25 Mega Pixel CMOS Image Sensor with higher frame rate of 46 FPS, high sensitivity of 2.2e-rms. High speed serial video output (16L HISPI^{TM} and 8L MIPI), 8-data paths, row timing of 4.85us are used to achieve the higher frame rate. A 1.1um BSI pixel with 12-bit Hybrid (SAR/RAMP) ADC was used to achieve high sensitivity. The read out noise are 3.7e-$_{rms}$ at 1x analog gain and 2.2e-$_{rms}$ at 8x analog gain. No Visible structural noise was observed. The circuit optimization and dynamic power management of clock gating are used for power reduction. In the full resolution (5760x4320), the power consumption is 685mW at 46frames/s and 550mw at 30frames/s. This chip also supports various sub-sampling mode including 3x3 skip/bin mode to enable 4k30 video mode, 1080p60 video.

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