Preliminary Experiment for Precise and Dynamic Digital Calibration for Two-Stage Cyclic ADC Suitable for 33-Mpixel 120-fps 8K Super Hi-Vision CMOS Image Sensor

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***Abstract*— An ADC operation and signal processing scheme in the error measurement mode has been developed to determine error coefficients. A preliminary experiment was performed by using an ADC test circuit to verify the scheme's effectiveness for precise and dynamic digital calibration. The calibration process was performed by using the evaluated values of error coefficients in the proposed way, and the results demonstrated that the nonlinearity of the ADC was successfully improved by compensating for errors caused in the ADC due to capacitor mismatch, finite gain and incomplete settling of the amplifier, and offset. The DNL and INL were improved to +0.49/−0.72 LSB from +0.39/−1 LSB and +4.7/−1.4 LSB from +5.8/−2.9 LSB, respectively. These results show that the proposed method is promising for achieving precise and dynamic digital calibration.**

Keywords—Digital calibration, Cyclic ADC, Super Hi-Vision, 33-Mpixel, 120-fps, CMOS image sensor

I. INTRODUCTION

We have been researching and developing a digital calibration technique [1][2] for a two-stage single-ended cyclic ADC suitable for a 33-Mpixel 120-fps 8K Super High-Vision CMOS image sensor [3][4] to improve the nonlinearity of the ADC by correcting errors generated in the ADC. We demonstrated its effectiveness by a simulation [5][6] and implementing an experimental chip [7]. The technique needs to accurately determine error coefficients that define the quantity of errors caused in the ADC. Therefore, the error coefficients must be determined by measuring the ADC output directly. This technique not only makes the digital calibration process more precise but also enables it to perform in the dynamic operation mode. However, the error coefficients have so far been determined on the basis of estimation from the design parameters of the ADC [7]. Therefore, we proposed a new ADC operation and signal processing scheme to determine them by measuring the ADC output code including the errors and performed a preliminary experiment by using the ADC test circuit to verify its effectiveness for precise and dynamic digital calibration.

II. DIGITAL CALIBRATION ALGORITHM

Figure 1 shows a schematic diagram of the 2-stage cyclic ADC with 12-bit resolution. The single-ended cyclic ADC with internal reference and a return-to-zero (RTZ) digital-signal feedback technique [8] is used in each stage of the ADC. Each stage uses 1.5-bit architecture, which generates 3-state redundant binary (RB) codes expressed with two decision levels (2 bits). The ADC consists of a single-ended amplifier, two capacitors (sampling capacitor C_{sA} and feedback capacitor C_{fA} for the first-stage ADC (ADC_1), and C_{sB} and C_{fB} for the second-stage ADC (ADC_2)), sub-ADC with two comparators, switch transistors, and DAC with a decoder. Sampling capacitor C_{sA} is divided into C_{s1A} and C_{s2A}, and C_{sB} is divided into C_{s1B} and C_{s2B} for generating internal reference with high accuracy [8]. 12-bit resolution is achieved by converting the first 4 bits of conversion in ADC_1 and the last 8 bits of conversion in ADC_2 within the period of 1.85 μs, which means a sampling rate of 540 kS/s.

The cyclic ADC has four operating phases: reset, sampling, amplification, and feedback. The most significant bit (MSB) is output in the sampling phase, and the other lower bits are obtained by repeating the amplification and feedback phases in a cyclic way.

In each cycle of the A/D conversion, errors are caused by capacitor mismatch between C_{sA} and C_{fA} and also C_{s1A} and C_{s2A} for ADC_1; capacitor mismatch between C_{sB} and C_{fB} and also C_{s1B} and C_{s2B} for ADC_2; finite gain and incomplete settling of the amplifier; and offset caused by the charge injection and the clock feedthrough from the transistor switches [5-7]. These errors degrade the differential nonlinearity (DNL) and integral nonlinearity (INL) of the ADC, which in turn degrades the bit resolution. To compensate for the errors and improve the output characteristics of the ADC, the digital calibration

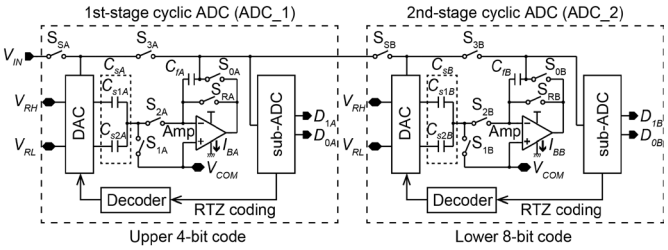

Fig. 1 Schematic diagram of two-stage cyclic ADC with 12-bit precision.

algorithm is applied to the two-stage cyclic ADC. During the A/D conversion, the errors mentioned above are accumulated in all cycles and the resulting error is calculated as a function of error coefficients and digital output codes. For example, the input-referred error code due to the finite amplifier's gain error E_{fg_t} after 12-bit A/D conversion is expressed as

$$E_{fg\_t} = -e_{fgA}\left(\sum_{i=2}^{3}(i-1)D(i)2^{-i} + 3\sum_{i=4}^{11}D(i)2^{-i}\right) - e_{fgB}\left(\sum_{i=5}^{11}(i-4)D(i)2^{-i}\right) \quad (1)$$

where e_{fgA} and e_{fgB} denote the finite amplifier's gain error coefficient of ADC_1 and ADC_2, respectively, and $D(i)$ denotes the output RB code for the i-th cycle of the operation. The error codes due to other error terms are calculated in the same way. The calibrated final output D_{calib} is obtained by subtracting the summation of the total number of error codes due to all error terms E_{sum} from the digital output code, as expressed below

$$D_{calib} = \sum_{i=1}^{12} D(i-1)2^{-i} - E_{sum} \quad (2)$$

Although digitized output without errors is desirable for accurate calibration, the algorithm will still work well if the errors are small enough.

III. Error Coefficients Determination Algorithm

To determine the error coefficients that describe four kinds of errors mentioned above by measuring the ADC output code, ADC operation principle is changed from that in the normal A/D conversion mode. Figure 2 shows the relationship between the operation phase and the output timing of the digital code in the normal A/D conversion mode and error measurement mode. In the normal A/D conversion mode, MSB is output in the sampling phase, and the lower bits are output after every amplification phase. In this case, DAC is controlled by the digital output code. On the other hand, a signal containing an error coefficients term is sampled in the sampling phase and the first amplification phase as the output voltage of the amplifier. The voltage is converted into the digital code as MSB, so the output timing of the digital code is delayed by one step more than that in the normal A/D conversion mode. To achieve the error measurement operation, configuration of DAC is modified from that in the ADC operated only in the normal A/D conversion mode by adding switches S_X and S_{ER} as shown in Fig. 3. The switches in the DAC are controlled independently of the digital output code in the sampling phase and the first amplification phase to obtain MSB and controlled by the digital output code the same as that in the normal A/D conversion mode to obtain the lower bits.

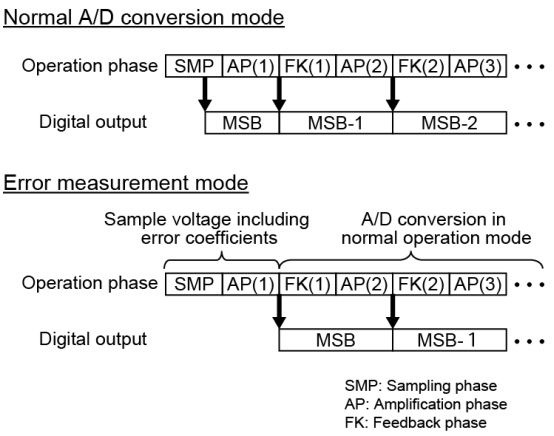

Fig. 2 Operation phase and output timing of digital code in normal A/D conversion mode and error measurement mode.

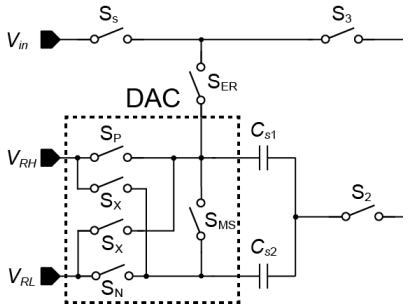

Fig. 3 Schematic diagram of DAC in ADC test circuit.

We prepare four different kinds of operation mode of the ADC in the error measurement mode to obtain the error coefficients by controlling the DAC operation and voltage applied to V_{in} terminal. Table 1 details the control of the switches and the voltage applied to V_{in} terminal in SMP and AP(1) phases shown in Fig. 2. Outputs of the amplifier in the first amplification phase include the error coefficients with a different manner in each mode. For example, when the upper and lower limits of the A/D conversion V_{RH} and V_{RL} are set to V_r and 0, respectively, the output of the amplifier in the first amplification phase of mode 1 is expressed as

$$V_{out} = \left\{\frac{1}{2}\left(1 - e_{fg} - e_{st} + e_m + e_{ms}\right) + e_{off}\right\}V_r \quad (3)$$

where e_{fg} denotes the error coefficient mentioned above,

Table 1 Control of switches and voltage applied to V_{in} terminal in SMP and AP(1) phases shown in Fig. 2.

Operation mode	SMP phase					AP(1) phase					V_{in}	Output code
	S_P	S_N	S_{MS}	S_X	S_{ER}	S_P	S_N	S_{MS}	S_X	S_{ER}		
Mode 1	ON	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	ON	V_{RL}	X_{m1}
Mode 2	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	ON	V_{RL}	X_{m2}
Mode 3	OFF	ON	ON	OFF	OFF	OFF	ON	ON	OFF	ON	$(V_{RH} + V_{RL})/2$	X_{m3}, X_{m3}'
Mode 4	OFF	ON	ON	OFF	OFF	OFF	ON	ON	OFF	ON	V_{RL}	X_{m4}

e_{st} denotes the settling error coefficient (e_{stA} for ADC_1 and e_{stB} for ADC_2), e_m denotes the capacitor mismatch error coefficient between sampling and feedback capacitors (e_{mA} for ADC_1 and e_{mB} for ADC_2), e_{ms} denotes the capacitor mismatch error coefficient between two divided sampling capacitors (e_{msA} for ADC_1 and e_{msB} for ADC_2), and e_{off} denotes the offset error coefficient (e_{offA} for ADC_1 and e_{offB} for ADC_2). The output including the error coefficients as expressed in (3) is sampled and converted into digital code in the cyclic A/D conversion process. After the A/D conversion is completed, the error caused during the A/D conversion process is added to the ideal digital output code. Therefore, the output in the digital domain is expressed as

$$X_{m1} = \frac{1}{2}\left(1 - e_{fg} - e_{st} + e_m + e_{ms}\right) + e_{off} + E_{sum} \qquad (4)$$

where X_{m1} denotes the output in the digital domain after 12-bit A/D conversion and E_{sum} denotes the total error in the digital domain caused during the A/D conversion process that is expressed by the error coefficients and the digital output code, the same as in (2). ADC_1 and ADC_2 are operated independently in the four operation modes shown in Table 1 to obtain four kinds of output code expressed in the same way as (4) (X_{m1A}, X_{m2A}, X_{m3A}, X_{m4A} for ADC_1 and X_{m1B}, X_{m2B}, X_{m3B}, X_{m4B} for ADC_2). As for ADC_1, the settling error coefficient of ADC_1 operated in connection with ADC_2 to transfer the residue output of amplifier in ADC_1 to ADC_2 must be sampled to denote the settling error coefficient e_{stAB} [5][6]. This is performed in operation mode 3, and output code of X_{m3}' including e_{stAB} is obtained. Five equations obtained for ADC_1 and four equations obtained for ADC_2 give the solution for all the error coefficients considered in the equations.

IV. Calibration Performance

The ADC test circuits were implemented in 0.18-μm CMOS technology to verify the effectiveness of the proposed method for determining the error coefficients for digital calibration. A chip micrograph of the test circuits is shown in Fig. 4. The test circuit has a capacitance and bias current in the ADC_1 smaller than those in the ADC implemented in the existing image sensor to evaluate the digital calibration performance.

The verification is done in accordance with the process flow shown in Fig. 5. The left chart shows the flow for digital calibration process, and right chart shows the flow to determine the error coefficients by error measurement operation mentioned in chapter III. To verify the characteristics of the calibrated output, sine wave is input to extract DNL and INL from the code density measurement.

Tables 2 and 3 list the measured digital output code X_{m1}, X_{m2}, X_{m3}, X_{m3}' and X_{m4} in each operation mode of error measurement and calculated error coefficients of the ADC_1 and ADC_2, respectively. The raw data of e_{fgA} + e_{stA} and e_{fgA} + e_{stAB} was calculated to be a negative value for ADC_1, which is inconsistent with the definition (e_{fg} = $(C_s+C_f+C_i)/(C_fG_0)$; C_i and G_0 are an input capacitance and gain of the amplifier, respectively). Therefore,

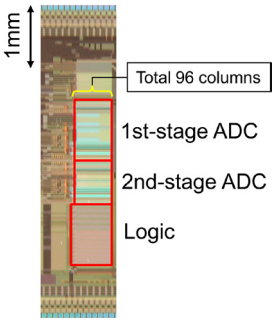

Fig. 4 Chip micrograph.

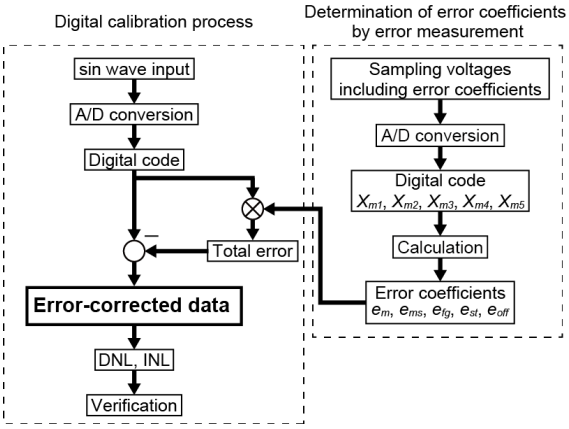

Fig. 5 Process flow of digital calibration.

Table 2 Measured output code of ADC in each operation mode of error measurement.

Output code		Measured value
ADC_1	X_{m1A}	0.512343
	X_{m2A}	0.513809
	X_{m3A}	0.497641
	X_{m3}'	0.504024
	X_{m4A}	0.008903
ADC_2	X_{m1B}	0.521193
	X_{m2B}	0.520467
	X_{m3B}	0.505625
	X_{m4B}	0.020635

Table 3 Error coefficients calculated from measured output digital codes shown in Table 2.

Error coefficient		Calculated value
ADC_1	e_{mA}	4.892×10^{-3}
	e_{msA}	-1.442×10^{-3}
	$e_{fgA} + e_{stA}$	$*1.106 \times 10^{-3}$
	$e_{fgA} + e_{stAB}$	$*1.274 \times 10^{-2}$
	e_{offA}	8.449×10^{-4}
ADC_2	e_{mB}	8.826×10^{-3}
	e_{msB}	7.285×10^{-4}
	$e_{fgB} + e_{stB}$	3.864×10^{-3}
	e_{offB}	7.451×10^{-3}

* Absolute values of the raw data calculated from output code shown in Table 2

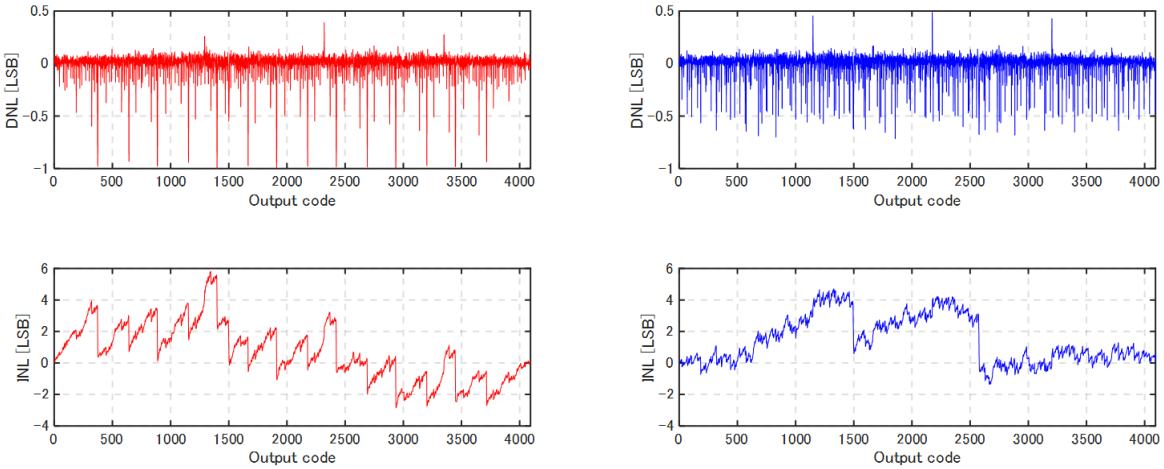

Fig. 6 (a) DNL and INL of measured data (before calibration) and (b) DNL and INL of the error-corrected data (after calibration).

absolute values of the raw data were calculated as error coefficients $e_{fgA} + e_{stA}$ and $e_{fgA} + e_{stAB}$. The cause of the inconsistency needs to be investigated.

In accordance with the process flow of the digital calibration shown in Fig. 5, the error-corrected data is calculated by subtracting the calculated total error from the output. Figure 6 shows the differential nonlinearity (DNL) and integral nonlinearity (INL) of the ADC before and after calibration. The DNLs before and after calibration were +0.39/−1 LSB and +0.49/−0.72 LSB, and the negative peaks down to −1 are improved, which means the missing codes are restored. The INLs before and after calibration were +5.8/−2.9 LSB and +4.7/−1.4 LSB, which also show an improvement due to the calibration process. The negative jump of the INL exists at fifteen output codes before calibration, which means a nonlinearity of the output characteristics. On the other hand, it decreases to exist at only two output codes after calibration. These two codes are equivalent to the threshold voltage applied to the comparators in the ADC, so they are more likely to show nonlinear characteristics than other output codes.

The calibration results demonstrate that the proposed ADC operation and signal processing scheme in the error measurement mode determines the error coefficients accurately in order to be able to process the precise and dynamic digital calibration.

V. Summary

An ADC operation and signal processing scheme was developed to determine error coefficients, and a preliminary experiment was performed by using the ADC test circuit to verify the proposed scheme's effectiveness for precise and dynamic digital calibration. The calibration process was performed by using the evaluated values of error coefficients in the proposed way, and the results demonstrated that the nonlinearity of the ADC was successfully improved by compensating for errors caused in the ADC due to capacitor mismatch, finite gain and incomplete settling of the amplifier, and offset. The DNL and INL were improved to +0.49/−0.72 LSB from +0.39/−1 LSB and +4.7/−1.4 LSB from +5.8/−2.9 LSB, respectively.

These results demonstrate that the proposed ADC operation and signal processing scheme in the error measurement mode is promising for achieving precise and dynamic digital calibration.

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