Backside illuminated 84 dB global shutter image sensor

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ABSTRACT

We present a backside thinned CMOS active pixel image sensor with 20x20 µm² global shutter pixels. Full well charge is > 500,000 e- and read noise is 27 e- RMS, resulting in a dynamic range exceeding 84 dB. The sensor employs a dual gain global shutter pixel, wherein the pixel signal is read out by two separate gain channels. The global shutter pixel employs four in-pixel storage capacitors and 13 nMOS transistors. This pixel preserves good shutter efficiency in combination with backside thinning. The sensor is backside thinned to increase QE. Two BSI configurations are being developed, targeted to the UV (270-400 nm) and visible (400-800 nm) wavelengths. The backside thinning flow is based upon SOI wafers, and an Al2O3 anti-reflective coating is employed for backside passivation and low reflectance.

1. INTRODUCTION

We report in this paper on a 1 MPixel backside thinned CMOS image sensor intended for “high-flux” space applications, such as Earth Observation. This chip is developed for the European Space Agency (ESA) as a demonstrator of the capabilities of CMOS. Requirements for the CIS are a large dynamic range (>84 dB) and full well charge (>400,000 e-) in combination with global shutter and backside illumination (BSI) to achieve a QE of 50% between 270 and 400 nm, and 75% between 400 and 800 nm. Global shutter, BSI and dynamic range requirements are conflicting requirements. Typical CMOS image sensors with a high dynamic range use a 4-T rolling shutter pixel, which achieves the lowest read noise. Global shutter pixels have increased read noise. The combination of a global shutter with backside thinning is also problematic, since the in-pixel signal storage node may not be affected by light. These issues have been solved by a new dual gain pixel structure with in-pixel voltage-domain sampling of reset and signal levels.

2. IMAGE SENSOR ARCHITECTURE

Figure 1 shows a block diagram of the image sensor. The sensor is designed in a 0.18 µm 4 layers metal CIS process. Since it is a demonstrator chip, the architecture is kept simple. The two output busses per column are coupled to a column gain stage which performs a first CDS step and samples the residual {Signal – Reset} in the column stage. There are 2048 column amplifiers for the 1024 pixel columns, and these are split into four blocks of 512 columns. Each of these blocks connects to an output stage via a multiplexer. The output stage performs a second CDS step and buffers the signal to go off-chip to an AD converter. If required, the outputs can be multiplexed to 2 output channels.

The sensor is clocked with external control signals and runs at 16 fps at full resolution. An on-chip register bank can be used to control gain settings in the readout path and various bias settings.

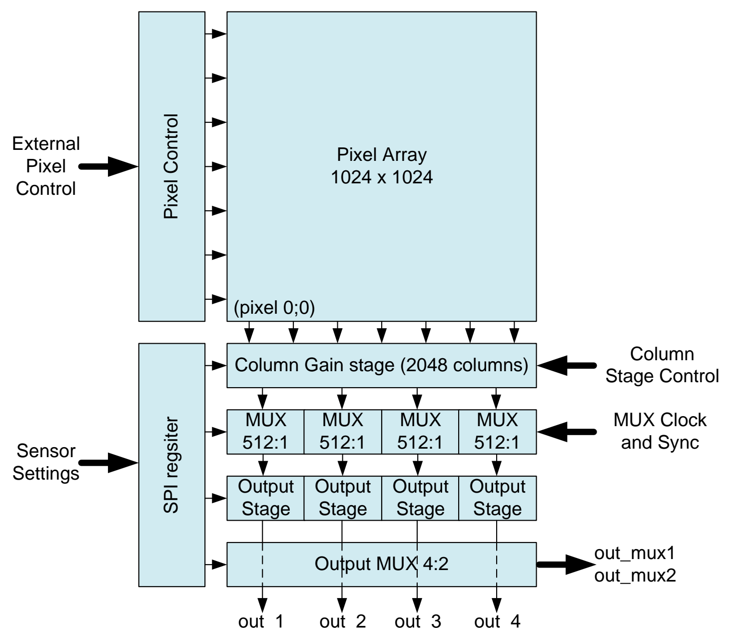

Figure 1: block diagram of the image sensor

3. PIXEL STRUCTURE

The solution proposed here for achieving a high dynamic range combined with global shutter is a pixel with a dual gain output: from a single exposure, the CIS outputs for each pixel a high gain signal which is used for the low light levels, and a low gain signal used for the highlights. When the high gain signal saturates, the value of the low gain signal can be used. Such dual gain structures have been proposed before. In [1] the signal of the pixel was split into a high gain and low gain signal at the column level. This amplifies however also the pixel source follower noise in the

high gain channel. In [2] the signal was split into high and low gain signals inside the pixel, before the in-pixel source follower, hereby avoiding increased noise contribution of the pixel source follower in the high gain channel. But this is reported for a rolling shutter pixel structure only. In the reported global shutter image sensor, the photocharge is sampled two times (once with high gain and once in low gain), and stored on in-pixel storage capacitors.

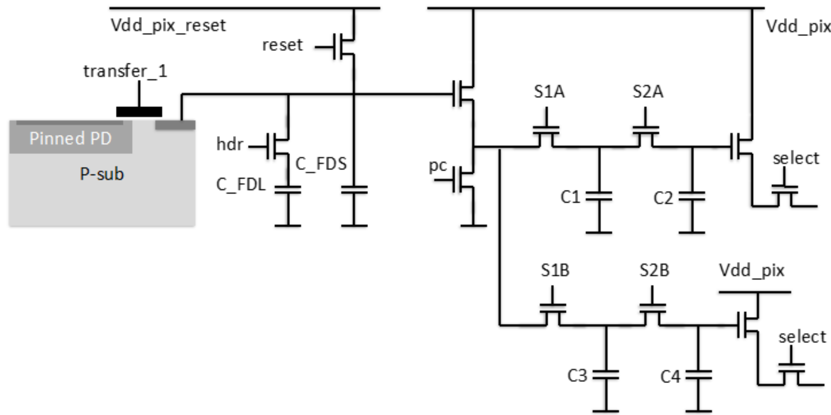

Figure 2: schematic of the dual gain global shutter pixel

Figure 2 shows the schematic of the pixel. The left part shows the photodiode and charge sense amplifier. Conversion gain can be switched through the HDR transistor, which adds the capacitor C_FDL to the sense node. When the switch is disabled, the sense node capacitance is C_FDS, which is only parasitic capacitance. A source follower with its load transistor PC buffers the sense node and the signal is then stored into two storage sections. Each storage section contains two capacitors (C1/C2 and C3/C4). C1/C2 stores high gain signals, and C3/C4 stores low gain signals. C2 and C4 store the reset level of the sense node in high gain and low gain mode respectively. C1 and C3 store the signal levels after charge transfer in high gain and low gain modes.

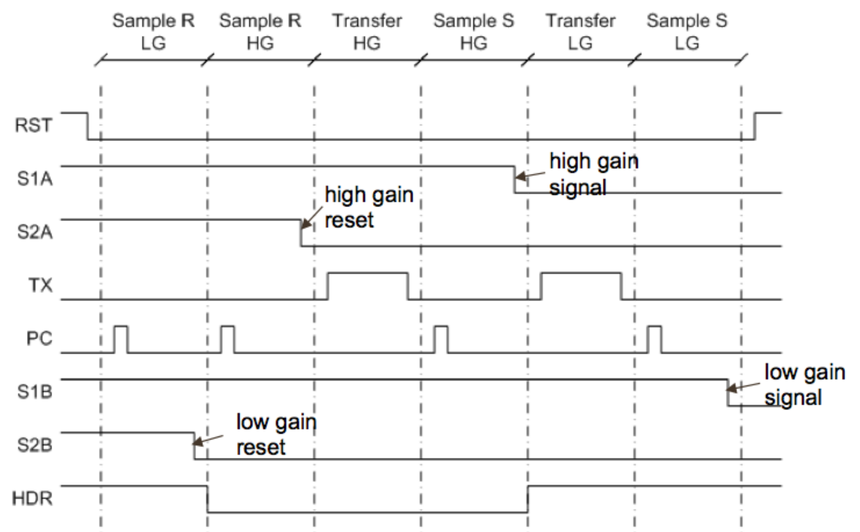

Figure 3: timing of the pixel during global sampling at the end of exposure

Figure 3 shows the timing of the pixel at the end of the exposure time. These pulses are applied synchronously on all pixels of the array, for the global shutter operation. First the reset switches off, and the reset level for the low gain signal of the sense node is sampled on C4 via switches S1B and S2B. Then transistor HDR switches off, and the reset level for the high gain signal is sampled on C2 using switches S1A and S2A. Then transfer gate TX is pulsed for a first time and the signal is sampled on C1 using switch S1A. Transistor HDR is switched off at this moment, so the sense node capacitance is C_FDS. In case of a small charge packet, all photocharges (q_{photo}) are transferred from the pinned photodiode to the sense node, causing a voltage drop C_FDS * q_{photo}. In case of a large charge packet, the sense node reaches a voltage level below the pinning voltage of the pinned photodiode. The high gain channel is then saturated. After sampling of the high gain channel, the HDR switch is switched on and the sense node capacitance increases to C_FDS+C_FDL. This capacitance is large enough to handle the entire charge packet of a saturated photodiode without saturation. Then the transfer gate is pulsed a second time. All charges are transferred to the sense node, causing a voltage drop {C_FDS+C_FDL}* q_{photo} which is sampled on C3 via switch S1B. In case when the charge packet is small, the same charge packet is sampled (but with a low gain) on C1 as was sampled on C3 with high gain.

Readout of the pixel array happens row-by-row. When a row is selected, the reset levels stored on C2 and C4 are put on the two column output busses of the pixel and sampled in the column amplifier. Then switches S2A and S2B are pulsed. This shares charge of C1 and C2 and C3 and C4 respectively. The output busses now output (Vreset+Vsignal)/2 of the high and low gain channels, which are sampled in the column amplifier. The column amplifier subtracts both samples taken, resulting in {Vsignal – Vreset}/2. The column amplifier will further apply the required gain to match its output signal to the subsequent voltage range of the readout chain, including the ADC.

4. MEASUREMENT RESULTS ON FSI SENSORS

Table 1 lists the pixel performance parameters measured on FSI devices. The conversion gains for high and low gain channels are 13 and 1.5 µV/e- respectively. The temporal noise in each of the readout channels is determined by the kTC noise of the sample capacitors C1/C2 (or C3/C4) and the thermal, 1/f and RTS noise of the in-pixel source followers [3].

The photodiode is split into 4 sub-diodes to improve charge transfer. Measured lag is better than < 0.1%. The sample capacitors for the high gain channel are made by NMOS transistors in inversion. This offers the densest capacitance (5 fF/µm^2). To save pixel area for the photodiodes itself, the 150 fF capacitors for the low gain channel are made by metal-isolator-metal (MiM) capacitance with a density of 1 fF/µm^2. These capacitors cover the photodiode, which is not an issue because of the backside illumination of the final detector.

Table 1: measured pixel performance parameters

	High gain channel	Low gain channel
In-pixel capacitors	2x MOS 150 fF	2x MiM 150 fF
Conversion gain	13 µV/e-	1.5 µV/e-
Full well charge	57700 e-	510000 e-
Noise (pixel output)	27 e- RMS	233 e- RMS
Dynamic range	66.6 dB	66.8 dB
combined	85.6 dB	
Dark current @ 25ºC, frontside illuminated	6000 e-/s	

Both the MiM and MOS capacitors do not collect any photocharges from the substrate. This is important for the backside thinned device, since such collection would cause lower shutter efficiency or a high parasitic light sensitivity of the global shutter pixel. The small amount of photocharges that can be collected on the capacitors through the source or drain junctions of the switches S1A, S2A, S1B and S2B have equal effects on the signal and reset samples and are also subtracted away through the correlated double sampling of the readout chain. In earlier reported small 5.5 µm single gain global shutter pixels with such voltage-domain sampling stage, we measured a parasitic light sensitivity of < 1/25,000 [5]. This corresponds to a shutter efficiency of 99.996%. Shutter efficiency has not been measured yet on these sensors (see later), but is expected to be better due to the relatively smaller parasitic collection area.

Figure 4 plots the signal-to-noise ratio against input signal in electrons. The shot noise is dominant at the high gain channel before saturation of that channel. At saturation, the low gain channel can take over. The shot noise is 240 e- at saturation of the high gain channel. The total temporal noise in the low gain channel is then 334 e- RMS (240 e- shot noise and 233 e- dark noise). This causes a SNR drop of 2.8 dB.

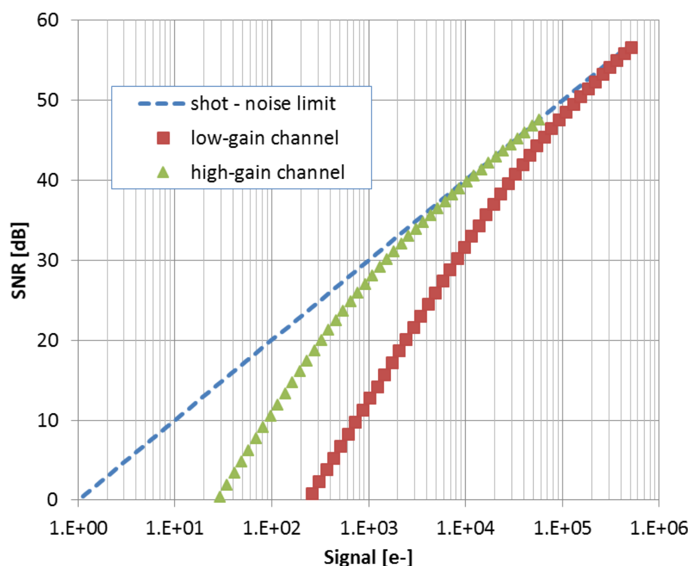

Figure 4: signal-to-noise ratio versus input signal for both channels

5. BACKSIDE THINNING

Backside illumination is required to reach the requested quantum efficiencies of 50% between 270 and 400 nm, and 75% between 400 and 800 nm. As mentioned before, this also allows using the frontside surface for MiM sample capacitors. A QE of 75% at 800 nm also requires a minimum required thickness of 20 µm. This will adversely influence the MTF and crosstalk for short UV wavelengths. Therefore, It was decided to make separate devices optimized for the UV (270-400 nm) and the visible (400-800 nm) band. This also allows optimizing the anti-reflective coating (or ARC) for the specified wavelength band.

The backside thinning flow is based upon SOI start material and is similar as the process described in [5]. The CMOS circuits are processed on SOI wafers on which an epitaxial layer of 3 or 10 µm is grown (3 for UV and 10 for devices for the visible band, more than 10 µm epitaxial growth was not possible). After CMOS processing, a carrier wafer is attached at the frontside by adhesive wafer bonding, and the backside of the wafer it grinded and etched up to the buried oxide layer of the SOI. The use of the buried oxide layer at etch step allows to achieve good thinning uniformity across the wafer. Then the buried oxide layer itself is etched away. To passivate the backside surface, and also as an anti-reflective coating, a layer of Al_2O_3 is deposited. The Al_2O_3 layer features negative fixed charges, which creates a hole accumulation layer at the Silicion-Al_2O_3 interface. This layer is used to passivate the backside surface. Thermally generated electrons at the interface recombine with the holes and do not contribute to the dark current in the photodiodes. As a final step, the bond pads are opened (from the backside), after which the wafer can be diced and assembled by wire bonding.

The SOI processing created a specific issue. First images of SOI processed image sensors showed a large amount of hot clusters, even before backside thinning. These clusters were large in amplitude and got larger at higher pixel array power supply and at lower temperature. An important increase of the power consumption of the pixel array was also observed. The temperature behavior pointed to a different mechanism than the classical thermal generation of dark or leakage currents, such as caused by crystal defects, or interstitials from contamination through contaminants that create mid-bandgap interface states. Emission microscopy revealed near infrared (NIR) emission of light at pixels present at the hot clusters. The large white clusters are thus caused by self-absorption of the emitted photons. Detailed microscopic analysis showed that the source of emission was one of the two n+/p junctions which was operated at the highest potential in the pixel, namely the drain junctions of the reset transistor and of the source followers [4]. Electroluminescence in silicon of photons with energy above the silicon bandgap can be explained by hot carriers present in strong electric fields. We expect that certain impurities in the silicon are present inside the strong electric fields of the reverse biased n+/p junctions and reduce the breakdown voltage. This causes avalanche breakdown, and the hot carriers create NIR photoemission during breakdown.

In standard bulk wafers these impurities are collected by a gettering layer located deep inside the wafer. Due to the buried oxide layer, this mechanism cannot be used in SOI wafers. Instead some impurities are collected by the phosphor present in the n+ diffusions and limit the breakdown voltage of the junction.

This issue has been fixed and dark cluster-free images have been demonstrated on front-side illuminated devices processed on SOI. A second lot of SOI devices has been processed and FSI measurements show that the high defectivity seen in the first lot has been eliminated. However, after backside processing and assembly, the sensors exhibit higher than expected power consumption and malfunctioning. The cause is currently being investigated. First results point towards an issue in the wire bonding process. Unfortunately this issue will delay the final characterization of the detectors in BSI configuration including quantum efficiency, dark current, MTF, etc.

6. Conclusions

A CMOS image sensor with global shutter, and dual gain per pixel has been developed. The combined dynamic range exceeds 84 dB. The global shutter is compatible with backside thinning. SOI wafers are used in the thinning flow in order to achieve good thinning uniformity across the wafer. Initial problems with photoemission due to lack of gettering of impurities have been fixed as confirmed on new FSI prototypes. Most likely, a bonding issue currently blocks the final characterization of the BSI detectors.

Acknowledgements

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