PTC Inspired Column Level Compression in Low Power CMOS Imagers

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***Abstract*—The overall power consumption of CMOS imagers is dominated by the communication layer. A number of compression techniques have been introduced in the processing layer to reduce the power consumption of the communication layer. These compression techniques use redundancy present in the spatial or temporal domain. This work presents an algorithm to compress the depth of the pixel in the digital domain. The compression scheme remains loss-less due to the presence of photon shot noise which dominates at high light intensities. Photon-transfer-curve (PTC) inspired analog-to-digital (ADC) converters, realized using bandwidth-limited micro-power comparators have an inherent non-linearity problem. This paper analyzes the said non-linearity, and proposes a solution to eliminate the non-linearity. The improved linearity results in increased conversion speed of two-step slope ADCs.**

I. Introduction

The growing demands of increased spatial, temporal resolutions and the pixel bit depth increase the amount of data handled by the communication layer of CMOS imagers [1]. Since the overall power consumption of an imager is dominated by the communication layer, various approaches have been explored in the recent past to reduce the bandwidth requirement. The conventional data compression approaches trade off the power consumption of the processing layer to reduce the power consumption of the communication layer [2,3]. Besides increased power consumption, the circuit level implementation of the conventional data compression algorithms also demand a larger chip area. Alternatively the techniques focusing on simultaneous reduction of the power consumption in communication and processing layers do not guarantee high image quality [4,5]. Most of these approaches compress the data by exploiting the temporal or spatial redundancies and the pixel bit depth has been given the least consideration. Resource-aware threshold-based information reading can be thought of as a step towards achieving compression in pixel bit depth [6]. This has been achieved with a significant loss of the low frequency information in spatial domain and is not suitable for all applications. In addition, it also does not guarantee reduction in the number of bits allocated per pixel. Logarithmic pixels are another example of compression in pixel bit depth. Fixed pattern noise limits the use of logarithmic pixels in mainstream imagers.

The conventional compression algorithms used in imagers rely more on the environment and do not exploit the device or optical properties of the image sensor itself. However, the optical properties of the image sensor have been used in imagers to overcome the inherent speed limitation of the slope ADCs [7] shown in figure 1. The conversion speed of slope ADCs can be increased by increasing the quantization step size at high light intensities. This has been justified by the increase in photon shot noise along with the increase in light intensity which can be seen in the PTC of the image sensors. The increased quantization step size at high light intensities leads to an increase in conversion speed by reducing the number of clock cycles required for an analog to digital conversion. However, these PTC inspired slope ADCs fail to use the reduction in number of clock cycles for data compression.

In this paper, we propose a PTC-inspired compression approach which is more suitable to be employed in column level slope ADCs. While the conventional PTC inspired ADCs increase the conversion speed, our proposed technique uses PTC for data compression. The proposed algorithm leads to data compression without increase in processing layer power consumption. Section II presents the proposed compression algorithm. A negative slope ramp ADC has been proposed in section III to improve the linearity of the slope ADCs using bandwidth limited pre amplifiers. Section IV concludes the paper.

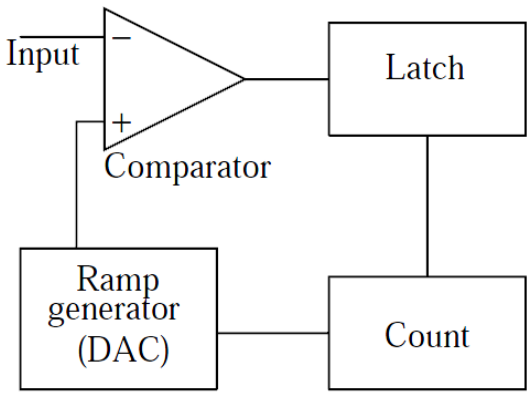

Fig. 1: Block diagram representation of a typical slope ADC

II. Proposed compression algorithm

In conventional PTC-inspired ADCs, the light intensities at which the quantization step size changes are decided by a quality factor 'r' [8]. The quality factor 'r' is the ratio of the maximum quantization noise to the photon shot-noise. The conventional PTC-inspired slope-ADCs increase the count step with an increase in quantization step size, to avoid post processing. The quantization step

S. No	Full well capacity ($\#e^-$)	Quality factor r	Digital representation		Inherent compression (%)	Dynamic range improvement (dB)
			Conventional (#bits)	Proposed (#bits)		
1	25,000	0.12	12	10	16.67	12
2	25,000	0.22	10	9	10	6
3	50,000	0.1	12	11	8.33	6
4	50,000	0.2	12	10	16.67	12
5	50,000	0.25	14	11	21.43	18

TABLE I: Compression in bit depth of pixels

size and the count step size are selected in powers of two to ease circuit design. The PTC-inspired ADCs provide compression in time domain by reducing the conversion time. However they fail in data compression, and do not contribute in reducing power consumption of the communication layer.

In our proposed approach, the counter increments by an LSB irrespective of quantization step size. As shown in figure 2, the proposed uniform counting leads to compression in the digital representation. For example, if a PTC-inspired slope-ADC requires a bit-depth of 10 for counting over 512 clock cycles, the proposed ADC will need a bit-depth of 9. Table I presents details of possible compression for a few scenarios. With pre-defined quantization steps for different regions of the ADC input, a large quality factor implies a large quantization noise compared to the photon shot-noise. Hence the quantization step size is increased for relatively low light-intensities. A similar argument holds for a PTC-inspired ADC of increased resolution with fixed quality factor and input range. The proposed approach uses photon shot-noise to enhance compression, by varying the quality factor (Table I). Additionally, conventional data-compression techniques can be applied to increase the compression ratio.

The dynamic range improvement presented in Table I has been calculated by considering a fixed word size for the PTC-inspired slope-ADC, and the proposed ADC. Reduction in word size leads to significant loss in the dynamic range of the conventional PTC-inspired ADCs. Table II quantifies the time spent at different quantization step sizes, for the same input range, for the examples considered in Table I. The rows 1, 4, and 5, in Table II indicate less time spent at low quantization steps. Both, conversion speed and data compression are higher in these cases.

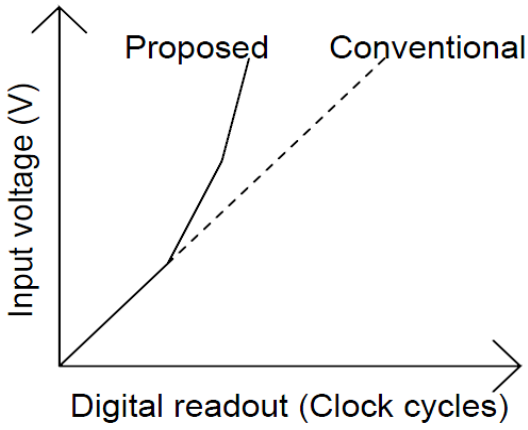

Fig. 2: Proposed readout

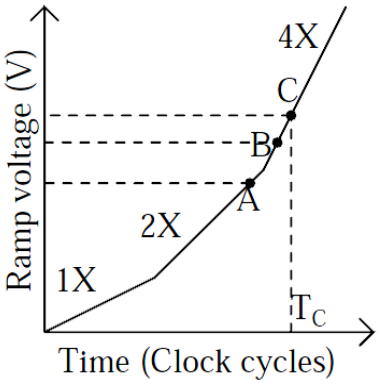

Fig. 3: Nonlinearity due to Slope dependent latency

III. Negative slope ramp ADC

A PTC-inspired slope-ADC is designed using the algorithm discussed in section II. Due to monotonicity, a voltage-mode digital-to-analog converter (DAC) is used for ramp generation. The comparator used in the ADC consists of a pre-amplifier, a regenerative latch and an SR latch. The single stage pre-amplifier includes an output auto-zeroing block to reduce offset. The pre-amplifier used in the comparator is biased in weak inversion to reduce power consumption [8]. A pre-amplifier in weak

S.No	Quantization step size				
	1X	2X	4X	8X	16X
1	142	212	424	115	-
2	169	253	88	-	-
3	407	610	618	-	-
4	102	153	306	308	-
5	17	49	49	1530	243

TABLE II: Number of clock cycles spent at different quantization levels, for the examples indicated in Table I.

inversion results in low band-width; as a result, there is a ramp-slope dependent latency. The SR latch introduces latency, in addition to the latency from the pre-amplifier. The latency in the SR-latch is caused by the limited swing at the output of the regenerative latch, which is biased with a constant current source to reduce power consumption. A ramp-slope dependent latency along with the proposed uniform counting leads to non-linearity errors, such as two different analog inputs resulting in the same digital word. Figure 3 shows hos the ramp-slope dependent latency results in non-linearity errors. For two analog inputs A and B from two different slope regions of the ramp, the ramp-slope dependent latency could result in equal conversion time, T_C. Further there could be missing codes in the ADC, as a result of reduction in latency with increase in the slope of the ramp. For example, the ramp with slopes of 1-LSB/50 ns and 2-LSB/50 ns result in latencies of 8 and 7 clock cycles respectively. In a slope ADC, latency in comparison allows the digital count to change.

A negative slope ramp is used in our design to reduce non-linearity (figure 4). The pre-amplifier is required to generate a minimum differential output voltage, so that the comparator that follows the pre-amplifier is able to make a decision. When the slope of the ramp decreases, the latency in the pre-amplifier increases. The increase in latency with the decrease in slope of the ramp ensures analog inputs A and B to result in two different conversion times T_C and T_D respectively. No missing codes are reported. However, the increase in latency with the decrease of the slope of the ramp leads to additional digital codes. The increased digital representations for a fixed input voltage range results in reduction in quantization step size. The reduction in quantization step increases the SNR in the transition region.

A 10 bit ADC was fabricated in a 180 nm technology (figure 5) and is being characterized. The ramp has three different slope regions. The bandwidth of the preamplifier is more than 50 times smaller than the clock frequency used. The simulated specifications of the designed ADC are presented in Table III. The INL and DNL improvements are specified in terms of quantization step sizes, which vary across the ramp range. The INL and DNL improvements do not consider the additional digital codes generated. A calibration scheme has been developed to include the effects of the additional digital codes in the ADC characteristics which will be published later.

Multiple ramp multiple slope (MRMS) ADCs are an example of two step PTC-inspired ramp ADCs. The best

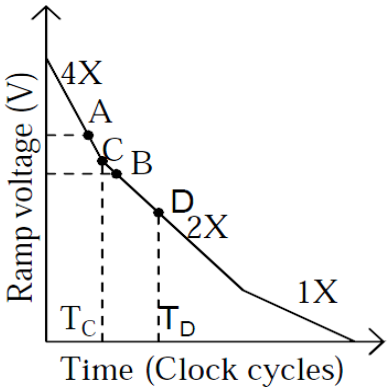

Fig. 4: Proposed negative slope reference ramp

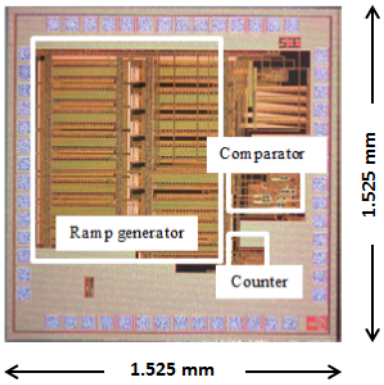

Fig. 5: Micro photograph of the fabricated integrated circuit

possible conversion speed that can be obtained in an MRMS ADC is limited by the nonlinearity present in the ADC when a positive slope ramp is used [7]. A negative slope ramp in a MRMS ADC reduces nonlinearity. With a negative slope ramp, it is possible to use multiple quantization step sizes in the ramp segments of an MRMS ADC to reduce conversion time. Table IV presents a possible scheme of quantization step size distribution for conversion speed optimization of a 12 bit MRMS ADC with a full-well capacity of 25,000 e^- and a quality factor of 0.1. Conversion speed of different slope ADCs are presented in figure 6. Single slope (SS) and PTC-inspired ramp are the conventional and PTC-inspired single step slope-ADCs whereas the remaining algorithms are of two step in nature. The modified MRMS algorithm gives similar performance compared to a multiple ramp single slope (MRSS) ADC [7] but with less number of ramp generators. The decrease in number of ramp generators reduces the power consumption significantly. Since the ramp generators are designed to handle maximum load, increasing the number of ramp generators increases the power consumption of the ramp generator block in a linear fashion. Further, an increase in the number of ramp generators also increases the complexity of the circuit, parasitic capacitances etc., which leads to a further increase in power consumption. Based on the values

Technology	180 nm
Power supply	1.8 V
ADC resolution	10 bits
Input voltage	1 V
Clock frequency	20 MHz
Counter word size	9 bits
Compression	10%
Expected INL improvement	± 1 Quantization step
Expected DNL improvement	± 1 Quantization step

TABLE III: Important specifications of the PTC-inspired ADC

Ramp segment	Conventional MRMS		Proposed MRMS	
	Slope	#LSBs	Slope	#LSBs
1	1X	256	1X	154
2	1X	256	1X,2X	258
3	1X	256	2X	308
4	1X	256	2X,4X	522
5	2X	512	4X	616
6	2X	512	4X	616
7	4X	1024	4X	616
8	4X	1024	4X,8X	1008

TABLE IV: Comparison of conventional and proposed MRMS algorithms

presented in Table IV, the proposed negative-slope ramp in MRMS ADC takes around 162 clock cycles to perform the conversion. The conversion is performed with the help of 8 ramp generators. The best possible conversion speed obtained by the MRSS ADC takes around 128 clock cycles with a need of 64 ramp generators. The results illustrate the trade-off between power consumption and conversion speed.

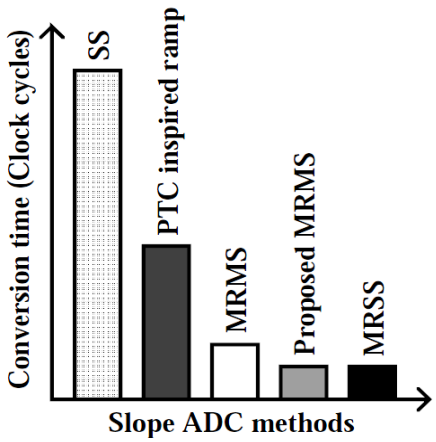

Fig. 6: Conversion speed comparison of slope ADCs

IV. Conclusion

A lossless data compression which does not increase the power consumption of the processing layer has been proposed. The designed prototype ADC is expected to give an inherent compression of 10%. With the variation in quality factor, the inherent compression can be as high as 25% for different full well capacity levels and ADC resolutions. Conventional data compression methods can be applied in addition to the inherent compression in the proposed algorithm. A negative-slope ramp ADC has been proposed to reduce the nonlinearity present in PTC-inspired ADCs, when bandwidth limited pre-amplifiers are used in comparators. The negative-slope ramp ADCs improve the DNL by at least one quantization step size in all slope regions, which leads to several LSB improvement in the INL of the PTC-inspired slope ADC. A negative slope MRMS ADC can be used to replace an MRSS ADC, with a reduction in the number of ramp generators. The conversion speed of the proposed MRMS scheme is more than 80% of the best possible conversion speed obtained by an MRSS for a 12 bit ADC, while using only 1/8 of the power consumption for the ramp generator block.

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References

[1] N. Cottini, L. Gasparini, M. D. Nicola, N. Massari, and M. Gottardi, "A CMOS ultra-low power vision sensor with image compression and embedded event-driven energy-management," *IEEE Trans. Emerg. Sel. Topics Circuits Syst.*, vol.1, no.3, pp. 299-307, Sep. 2011.

[2] W. D. Len-Salas, S. Balkir, K. Sayood, N. Schemm, and M. W. Hoffman, "A CMOS imager with focal plane compression using predictive coding," *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2555-2572, Nov. 2007.

[3] A. Bandyopadhyay, J. Lee, R. Robucci and P. Hasler, "A 80μW/frame 104 $\times$ 128 CMOS imager front end for JPEG compression, *in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS'05)*, May 2005, pp. 5318-5321.

[4] C. Posch, D. Matolin, and R. Wohlgenannt, "A QVGA 143 dB dynamic range frame-free PWM image sensor with lossless pixel-level video compression and time domain CDS, *IEEE J. Solid-State Circuits*, vol. 46, no.1, pp. 259-274, Jan. 2011.

[5] Y. Oike, and A. E. Gamal, "CMOS image sensor with per-column ADC and programmable compressed sensing," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 318-328, Jan. 2013.

[6] Y. M. Chi, U. Mallik, M. A. Clapp, E. Choi, G. Cauwenberghs, and R. Etienne-Cummings, "CMOS camera with in-pixel temporal change detection and ADC, *IEEE J. Solid-State Circuits*, vol. 42, no. 10, pp. 2187-2196, Oct. 2007.

[7] M. F. Snoeij, A. J. P. Theuwissen, K. A. A. Makinwa, and J. H. Huijsing, "Multiple-ramp column-parallel ADC architectures for CMOS image sensors," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2968-2977, Dec. 2007.

[8] M. F. Snoeij, A. J. P. Theuwissen, and J. H. Huijsing, "A low-power column-parallel 12-bit ADC for CMOS imagers," *in Proc. IEEE Workshop CCDs, AIS*, Jun. 2005, pp. 169-172.