Linear Mode High Dynamic Range Bouncing Pixel with Single Transistor

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Abstract— A single NMOS pixel topology employing high dynamic range (HDR) bouncing scheme is proposed in this work. Previous pixel solutions employing such HDR bouncing scheme make use of a much complex circuit topology, yielding thus a low fill factor. The implementation of the proposed pixel topology requires an appropriate care with the low level of the gate voltage of the pixel NMOS transistor that must be lower than the GND level. Such control is performed by a special circuit also proposed in this work that uses an input signal varying from GND to VDD and produces an output signal varying from –VDD to VDD. Simulations have shown that the proposed HDR bouncing pixel applied to a simple 2x2 produces results similar to those of previous solutions asserting thus its effectiveness.

Keywords-Image Sensor; APS; Bouncing Pixel; High Dynamic Range; Swing Doubler; Voltage Level Shifter;

I. INTRODUCTION

High Dynamic Range (HDR) and high sensitivity are key requirements for many imaging applications [1]-[4]. Owing to the increased leakage current, noise components, limited quantum efficiency, and reduced signal swing as the feature size in CMOS technologies scales down, the dynamic range and sensitivity of imagers are negatively affected [4]. The design of imagers embodying HDR with good sensitivity while dealing with such issues is not an easy task.

In the literature a number of solutions have been proposed to solve such problem including: Companding sensors, or logarithm sensors, which presents HDR but poor sensitivity in the whole illumination range [1]; Multimode sensors, which operate in both linear and logarithm modes [3], present HDR and increased sensitivity for lower illumination levels, however, they still have poor sensitivity at high light intensities; Multiple scene capture [5] combines frames captured with different exposure times to produce the wide DR image, but requires complex signal processing and control, without solving the problem of the sensitivity at highlights. Besides that, they have lower frame rate due to the need of multiple exposures; Clipping sensors [6] use the well-capacitance adjustment to achieve a HDR, however they require a more complex control and signal processing and, due to the multiple reset switches, additional noise may be introduced; and frequency-based sensors [7], that feature HDR, high frame rate and linear response. However, as it works detecting saturation levels, very low sensitivity is achieved towards low illumination.

In a recent work, an alternative HDR pixel topology based on the Current-Mirroring-Integration (CMI) architecture was proposed [4]. Unlike other approaches presented in the literature, the alternative topology produces the HDR response operating in the linear mode using just a single sample, and employing a bouncing scheme which prevents signal from saturation. The HDR response is achieved with constant sensitivity within the whole DR. The schematic of such a pixel topology is presented in Fig. 1.

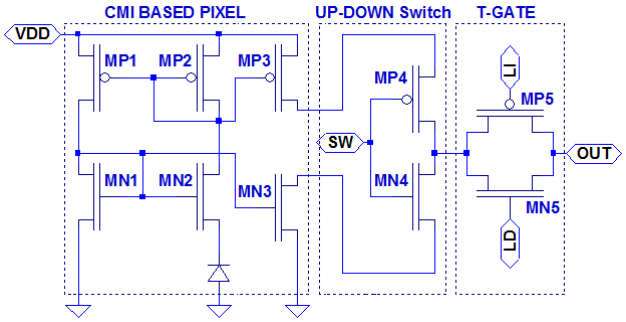

Figure 1- Schematic of the Original Bouncing Pixel.

The approach proposed in [4] employs a simple on-pixel automatic control, avoiding, therefore, complex built-in algorithms or image post processing. However, as the pixel employs six transistors (3NMOS and 3PMOS), it yields a much smaller fill factor than the basic well known 3T and 4T topologies presented in the literature [2]. This problem is especially detrimental when such topology is intended to be applied to high density arrays. In order to overcome such limitation a new single NMOS pixel topology is proposed in this work to be employed with the bouncing scheme of [4].

The proposed bouncing pixel topology details, and the simulation results asserting it, will be presented in section II. Conclusions drawn from this work are given in section III.

II. THE PROPOSED SOLUTION

In the original pixel topology [4], the unit cell comprises a CMI circuit and a photodiode. In order to customize the use of the CMI circuit and also to improve the pixel fill factor, in this work it is proposed the decoupling of the photodiode of the pixel in Fig. 1 from the CMI circuit via an NMOS access transistor. Such approach allows the use of a single CMI circuit by all photodiodes in a column of a pixel array. An example of the implementation of the NMOS access transistor and the shared use of the CMI circuit in a 2 x 2 array is presented in Fig. 2. In this figure, the remaining column shared components, as described in the original approach (counter, shift register, capacitor and comparators), are omitted for a clearer visual understanding. Furthermore, in the original design, where the CMI was placed inside the pixel itself, a big concern would be process variations from pixel-to-pixel. While calibration for the whole array could be a good solution for that problem, the simple fact of removing the CMI block from the unit cell, besides of enhancing the fill-factor, also precludes potential Fixed Pattern Noise (FPN) from one pixel to another, which would be mainly due to CMI transistors mismatch. With

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that new architecture, a column FPN would still exist, but allowing much more robust CMI design, and easier calibration process.

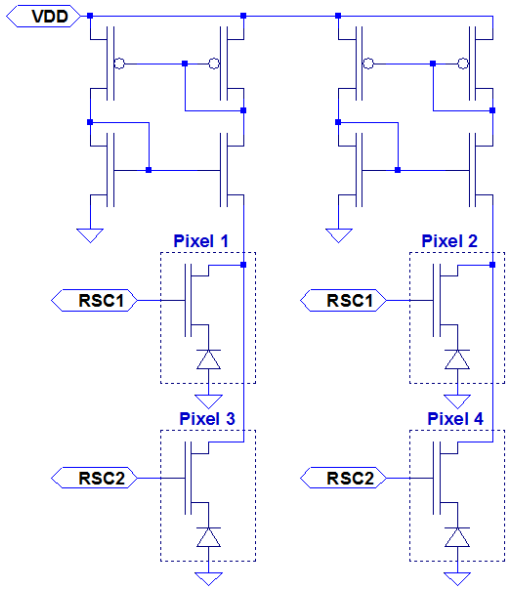

Figure 2- 2x2 Pixel array with their respective NMOS access transistors, and the proposed CMI sharing scheme.

The implementation of such pixel topology requires appropriate care with the low level of the NMOS access transistor gate voltage, that must be lower than GND level. This is necessary because when a high light intensity reaches the pixel, the source voltage of the access transistor falls below GND, thus turning on this transistor in an inappropriate moment. BSIM3V3 simulations of the array presented in Fig. 2, designed in the AMS CMOS 0.35µm technology, using a source voltage of V_{DD} = 3.3 V, have shown that setting the access transistor to the accumulation regimen, with its gate voltage at -1.0V, is effective to prevent it inappropriate activation even for hypothetical photocurrents as high as 100 mA.

In order to produce the appropriate control signal for the NMOS access transistors, a special circuit based on a swing level doubler presented in [8] was employed. The output produced by this circuit is used as row selection control (RSC) to drive both terminals RSC1 and RSC2 in Fig. 2. The schematic of such circuit is presented in Fig. 3. The upper circuit of this figure, labeled as SWING DOUBLER, doubles the swing of a signal varying between GND and V_{DD}, producing thus an output varying between GND and $2V_{DD}$. The lower circuit labeled as LEVEL SHIFTER, shifts the voltage by $-V_{DD}$, thereby producing the desired output for RSC swinging from $-V_{DD}$ to V_{DD}.

In the RSC generator of Fig. 3 the transistor M_{b1}, M_{b2}, M_{b3}, and M_{b4} are employed to perform body bias to the PMOS transistors. The body bias scheme proposed in [9] is necessary to avoid latch up that may occurs when the PMOS transistors operate at high voltage levels, like in this case. As the low level of RSC is $-V_{DD}$, it assures an excellent cut off of the NMOS access transistor, since it is much lower than the -1 V needed for proper gating operation. This circuit is suitable to drive very high impedance nodes, as the gate of MOS transistors.

During the slot of time in which the NMOS access transistor is turned on, the operation of the proposed pixel is fairly similar to that of the original bouncing pixel in Fig. 1, which is described in [4]. Whereas the NMOS access transistor is turned off, the photodiode is decoupled from the CMI circuit, and this circuit can be connected to a different pixel in the same column of the array.

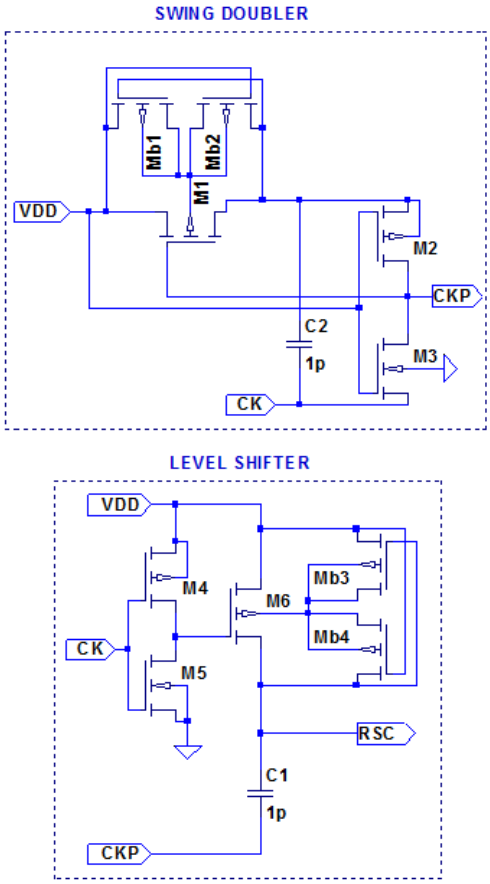

Figure 3- Proposed Row Selection Control Generator.

The basic operating principle of the bouncing pixel is quite similar to that of a regular integrating pixel [2]: the higher the photocurrent, the steeper the output slope. However, the bouncing scheme proposed in [4] prevents saturation of the integrated pixel output signal, by inverting the slope when the output reaches a predefined high level. The output is again inverted when it reaches an also predefined low level, and this process repeats itself every time the signal would saturate within the boundaries of a stipulated voltage difference. An example of the original bouncing pixel output of Fig. 1 for four different photocurrents is shown in Fig. 4.

In the results present in Fig. 4 the lower photocurrent of 5 nA produces the smoothest slope, whereas the photocurrent of 20 nA produces a slightly steeper slope than the first. The bouncing feature can be observed with the photocurrent of 200 nA that produces a so steep slope, that the output signal bounces twice at the uppermost and once at the lowest limit in the integration time of 40 µs. Whereas for the highest photocurrent of 1 µA, the pixel output bounces eight times at the uppermost limit and seven times at the lowest limit during the same integration time.

For the bouncing scheme both the output read voltage, and the number of inversions within the integration time, determine the actual photocurrent value, and hence the

illumination level [1]. The output voltage signal is compared to the upper and lower references by two comparators, comprising part of the column shared circuit, omitted in Fig 2. Likewise, the number of signal slope inversions are counted and shifted to a serial output by a counter and a shifter register, which also compose the column shared circuit as described in [1]. A dynamic range as high as 118 dB has been achieved using such scheme.

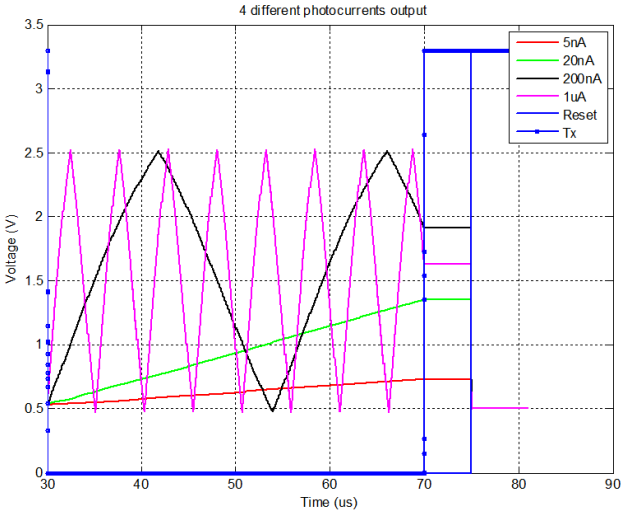

Figure 4- Pixel Output.

An example of the operation of the RSC generator of Fig. 3 is presented in Fig. 5. This plot shows an RSC control signal with a period of 300 µs and a pulse width of 65 µs. The results show that the circuit requires a settling period before delivering the appropriate control signal varying between V_{DD} = 3.3 V and a level near -V_{DD}, of -3.1 V. It is important pointing out that the approximation of the lowest level of -V_{DD} depends of the on the value of the capacitances C1 and C2 in Fig. 3. For example when C1 and C2 are of 1 pF each, the lowest output level is -3.1 V, whereas when these capacitances are of 10 pF each, the lowest output level is -3.26 V. This output was produced by an input signal varying between GND and V_{DD} applied to the CK terminal in Fig. 3.

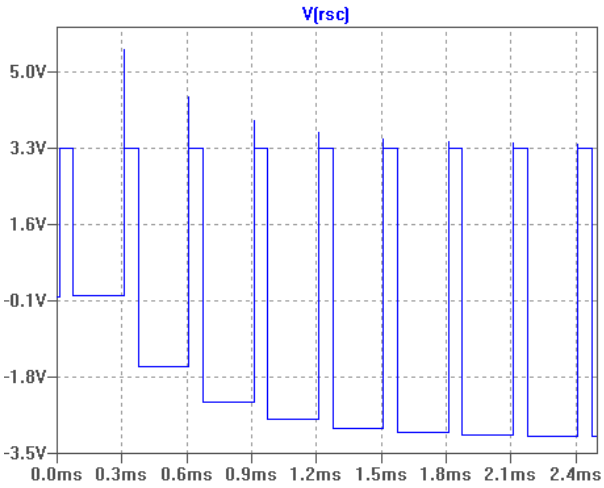

Figure 5- Row Selection Control.

The outputs plot of the 2 x 2 pixel array using the proposed CMI sharing scheme is presented in Fig. 6. All the pixels in a column share the same output circuit as that of Fig. 1, i.e. the CMI, the UP-DOWN switch and the T-GATE, besides of the omitted capacitor, comparators, counter and shift register. The T-GATE is also employed as column selection. In this plot the photocurrents in pixels (1,1), (1,2), (2,1), and (2,2) are 5 nA, 200 nA, 1 µA, and 20 nA, respectively. The outputs of the pixels in the same row are plotted in the same window of time. These plots show that the slope and the number of bouncing inversion for the simulated photocurrents are similar to the results presented in Fig. 4.

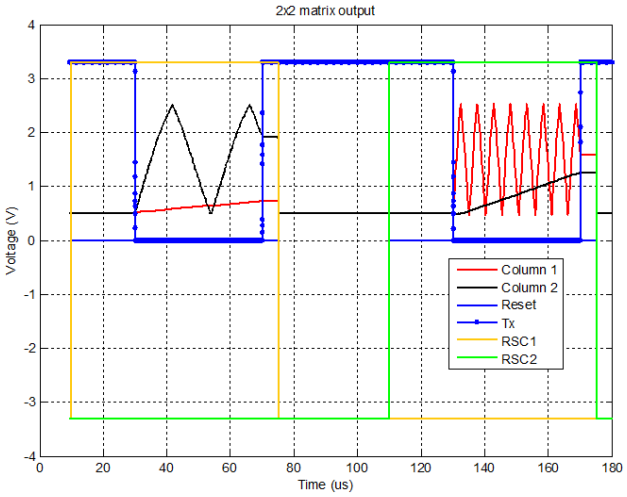

Figure 6- 2x2 pixel array integrated signal output (regarding Figure 2).

For the proposed scheme, in order to avoid spurious charge injection during the switching between columns, the transfer gate circuit, T-GATE in Fig. 1, must be activated just after the selection of a specific row. The yielded results assert the effectiveness of the serial selection of pixels in the same column, one at a time, using the proposed column shared scheme.

The results herein presented show an effective, yet simple way to extend the usability of the linear HDR bouncing pixel architecture, where a single transistor per pixel is employed, resulting in a solution with much higher fill factor than those of the conventional 3T and 4T pixel architectures.

It is important to point out that as smaller and smaller technology nodes are introduced in the image-sensor scenery, the extension of the signal range by using current, rather than voltage, plays a more significant role than the noise it introduces at the bottom.

III. CONCLUSIONS

The single NMOS pixel topology presented in this work provides a way to extend the usability of the HDR bouncing pixel for applications where high density arrays are required, by enhancing the fill-factor, and suppressing pixel FPN, due to the removal of the CMI, that is the biggest source of mismatch, from inside the pixel. Such pixel solution just requires that the low level of the control signal, applied to the gate of the NMOS access transistor, to be lower than GND. The circuit solution employed to produce such signal controlling makes use of an input signal pulse varying from GND to VDD, producing an output signal swinging from V_{DD} to a voltage close to $-V_{DD}$. Evaluations of the proposed pixel topology, as well as comparisons with previous solutions were performed through BSIM3V3 simulations, in AMS 0.35µm technology. The yielded results have shown that the

proposed HDR bouncing pixel with the proposed signal controlling applied to a simple 2x2 array, produces results similar to those of previous solutions, asserting therefore its higher potential for dense image arrays.

REFERENCES

[1] A. Spivak, a. Belenky, A. Fish, O. Yadid-Pecht, "Wide Dynamic Range CMOS Image Sensors – Comparative Performance Analysis," IEEE Transactions on Electron Devices, 2009, Vol. 56, Issue 11, pp. 2445-2461.

[2] A. E. Gamal and H. Eltoukhy, "CMOS Image Sensors," IEEE Circuits and Devices Magazine, vol. 21, pp.6-20, May-June 2005.

[3] C. A. de Moraes Cruz, D. W. de Lima Monteiro, E. A. Cotta, V. F. de Lucena Jr, and A. K. Pinto Souza, "FPN Attenuation by Reset-Drain Actuation in the Linear-Logarithmic Active Pixel Sensor," IEEE Trans. Circuits Syst. I, Reg. Papers, Online Early Access version July 11th, 2014.

[4] P. N. A. Belmonte, P.J. French, D. W. De Lima Monteiro1, F. Sill Torres,"Linear High-Dynamic-Range Bouncing Pixel with Single Sample," In Proceedings of 2013 International Image Sensor Workshop, ISSW 2013, Snowbird-Utah-USA, June 12-16, 2013.

[5] O. Yadid-Pecht and A. Belenky, "In-pixel autoexposure CMOS APS," IEEE J. Solid-State Circuits, vol. 38, no. 8, pp. 1425–1428, Aug. 2003.

[6] S.Decker, D. McGrath, K. Brehmer, and C. G. Sodini, "A 256 × 256 CMOS imaging array with wide dynamic range pixels and columnparallel digital output," IEEE J. Solid-State Circuits, vol. 33, no. 12, pp. 2081–2091, Dec. 1998.

[7] X. Wang, W. Wong, and R. Hornsey, "A high dynamic range CMOS image sensor with inpixel light-to-frequency conversion," IEEE Trans. Electron Devices, vol. 53, no. 12, pp. 2988–2992, Dec. 2006.

[8] C. A. de Moraes Cruz, C. A. dos Reis Filho, D. W. de Lima Monteiro, "Improved Charge Pump Circuits for Standard CMOS Technologies," in Proc. 27th Symp. Integr. Circuit Syst. Design, SBCCI, Aracaju-SE, Sep. 1-5, 2014.

[9] J. Cha, M. Ahn, C. Cho, C.-H. Lee, H. Kim, and J. Laskar, "Analysis and Design Techniques of CMOS Charge-Pump-Based Radio-Frequency Antenna-Switch Controllers," IEEE Transactions on Circuits and Systems—I: Regular Papers, Vol. 56, No. 5, May 2009.