A single-exposure linear HDR 17-bit hybrid 50µm analogue-digital pixel in 90nm BSI

Jeffrey M. Raynor[1], Andrew Scott[1,2], Christopher Holyoake[1,3], Donald S. Reay[2]
1 - STMicroelectronics, Imaging Division, 33 Pinkhill, Edinburgh, EH12 7BF, UK
2 - School of Engineering & Physical Sciences, Heriot-Watt University, Edinburgh, EH14 4AS, UK
3 - School of Engineering & Electronics, The University of Edinburgh, Edinburgh, EH9 3JL, UK
Phone: +44 (0)131 336 6192, Email: jeff.raynor@st.com

Introduction - We present an improved photon counting pixel (PCP) which includes both coarse and fine ADC which reduces the readout noise at lower light levels by 40dB compared to previous PCP sensors resulting in 100dB DNR. The ADC and all varying analogue voltages are contained inside each 50µm×50µm pixel making it especially suitable for large area sensors. In-pixel digital storage allows for global shutter operation without parasitic light sensitivity and fabrication in BSI process enables the capacitors to overlay the photodiode without affecting photosensitivity.

Increased dynamic range (DNR) of CMOS image sensors has been a goal since at least 1990 [1] and is key in many applications, especially automotive and other machine vision applications, medical imaging, especially X-Ray and other high-end consumer applications. Various techniques have been tried to increase DNR, including non-linear response [2], pixel skimming [3], multiple exposures [4], in-pixel ADC [5] [6]. Each of these approaches has limitations. Logarithmic response is not compatible with accurate colour image processing. Multiple exposures produce image artefacts with moving objects. PCP architectures [7] [8] allow for increased signal capability by counting the number of times the pixel has acquired a predetermined quantity of charge. As this count is stored in a digital counter, adding a single extra bit of storage will double the maximum number of signal electrons. The disadvantage of existing PCP architectures is that the output from the pixel is only the number of times the predetermined quantity of charge has been received, resulting in quantization noise dominating the noise performance. Some pixels include in-pixel ΣΔ ADC [9], but these require high frequency clock signals which are difficult to transmit over large areas.

The Analogue-Digital pixel with Range Extremely Wide (ANDREW) presented here overcomes the limitations in existing PCP by adding a "fine" conversion mode which enables readout of the quantity of charge remaining at the end of the exposure [10]. This reduces the quantization noise by 32dB in charge injection mode and 52dB in ramp mode. Hence the readout noise at lower light levels is reduced and the dynamic range is increased. The pixel also includes an auto-zero technique to cancel the effect of input offset voltage and reduce kTC noise.

Pixel Architecture - Fig.1 [11] shows the pixel schematic. Feedback capacitor C_{FB} and operational amplifier converts the photo-generated charge into a voltage and a constant level of illumination will cause the output to ramp linearly from the reset voltage (VRT) to a threshold voltage (VREF). The nominal swing is 1V (2Mē with 300fF capacitor), but can be controlled by adjusting these voltages.

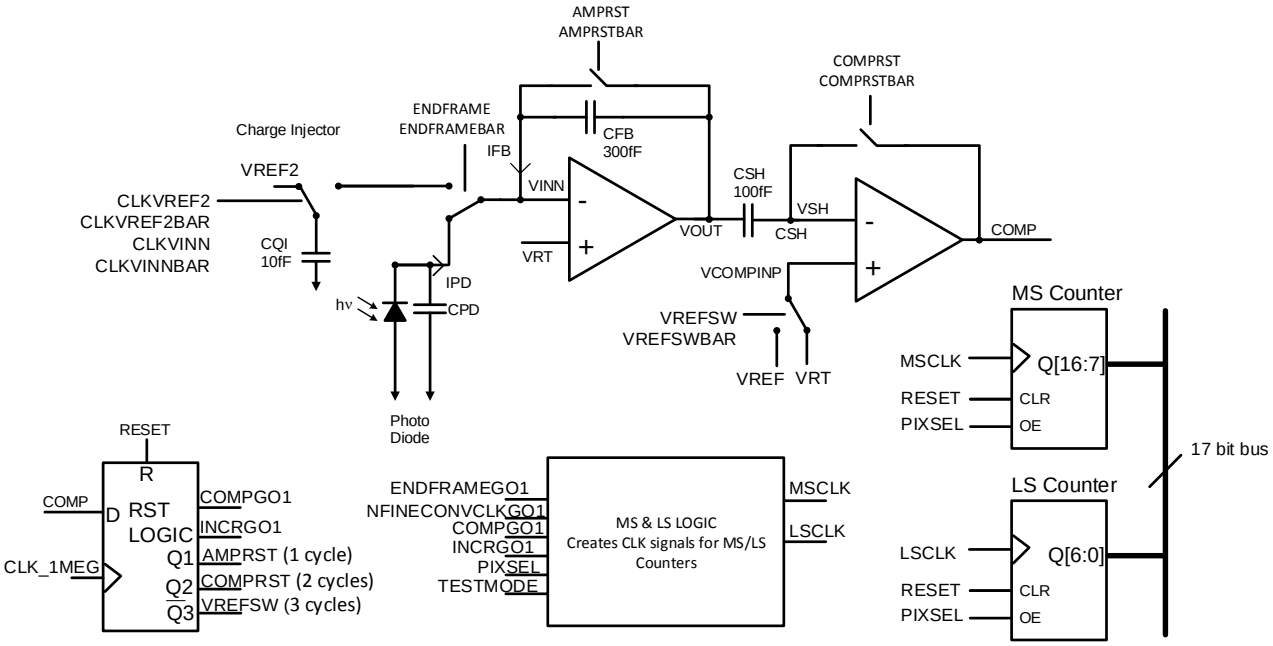

Figure 1 Pixel Architecture [11]

The conversion gain (CVF) can be adjusted by resizing C_{FB}. Once the output has moved by the desired amount, the charge integrator is reset and the 10 bit coarse counter is incremented. The charge integrator is AC coupled to the comparator (C_{SH}) and during every reset phase, an auto-zero operation is performed which cancels the effect of kTC noise on the charge integrator and the pixel-pixel variations in input-offset voltages of both the charge integrator and comparator. To ensure complete discharge of C_{FB}, the reset switch is controlled by in-pixel digital logic.

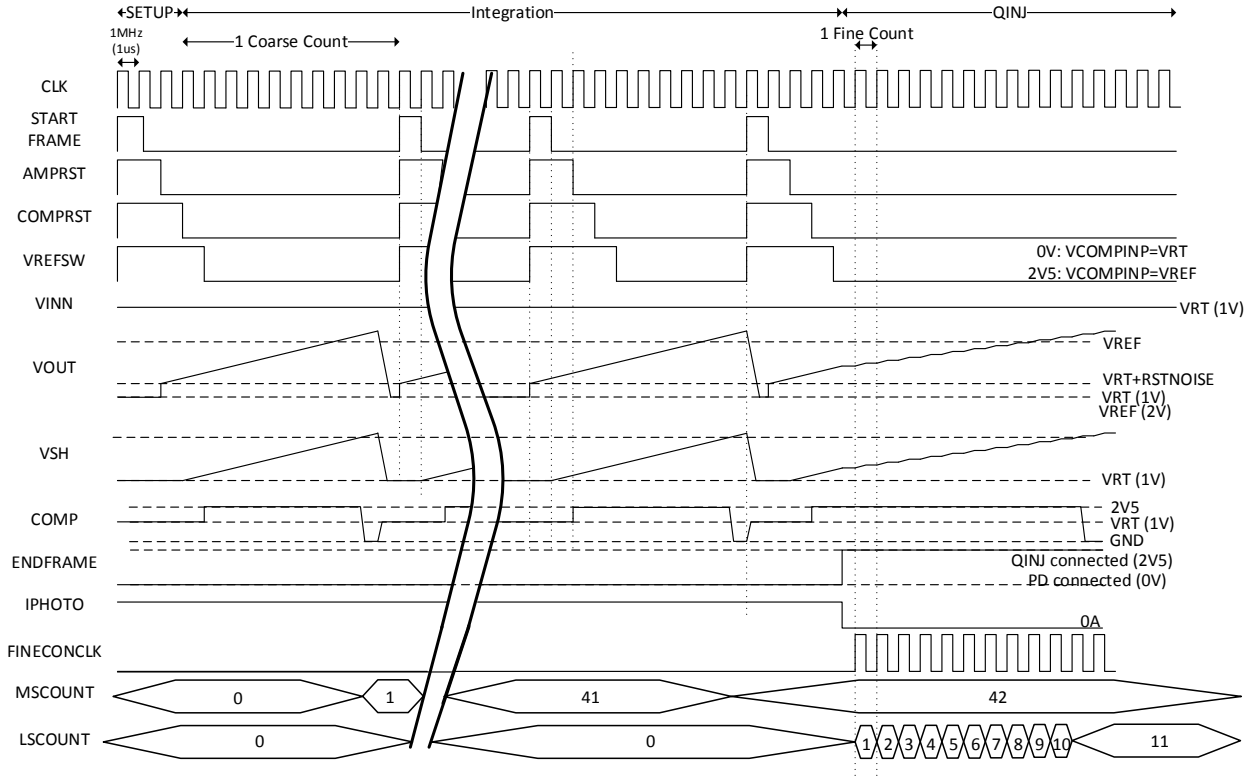

Figure 2 Pixel Timing Diagram – Coarse + Fine ADC conversion [11]

At the end of the integration phase, the charge remaining on C_{FB} is measured. The device supports two different readout modes. In the first type of fine-conversion mode (Figure 2) the comparator reference voltage VREF is kept constant and a small packet of charge is injected for each clock cycle at the input of the charge integrator and the fine counter in each pixel is incremented. Once the charge integrator has reached the threshold, the comparator fires and the counter is halted. The advantage of this mode is that the time varying analogue signals are confined to each pixel and not over a large array. This is an advantage in a large area sensor (such as an X-Ray sensor) as performance is independent of the capacitance and resistance of the analogue lines. In the second type of fine-conversion mode, the charge injection circuitry is not used, and the reference voltage VREF is instead ramped. The fine counter counts until the comparator fires; this is similar to the single slope ADC found in many image sensors, except that the comparator and digital storage is in-pixel. As each pixel contains storage, it can be operated in global shutter mode and as the storage is digital, it is immune to parasitic light effects.

$$\boldsymbol{V_O = (Max_{Count} - N_{Count}).(VRT - VREF2).C_{QI}/C_{FB}} \qquad \textbf{Equation 1}$$

From the fine count (N_{Count}), the reference voltages and capacitances, it is possible to calculate V_O (VOUT – VRT). Max_{Count} can either be calculated using Equation 2 or by calibrating the device in the dark.

$$\boldsymbol{Max_{Count} = \frac{VREF-VRT}{VRT-VREF2}.\frac{C_{FB}}{C_{QI}}} \qquad \textbf{Equation 2}$$

Implementation - The pixel was implemented in ST's 1P4M 65nm (BEOL) / 90nm (FEOL) BSI imaging process. 30% of the area is used by the MIM capacitors, however the BSI process allows vertical integration and they are placed over the front side of the photodiode without impacting the photosensitivity. Photo-generated charge in the PMOS transistors' NWELLs are lost and most of the charge generated near the NMOS transistors will also be lost, the size of the pixel was chosen such that the fill-factor was 50%. The pixel contains 63 GO2 transistors for the analogue and 812 GO1 for digital. The test device has an array format of 64(H)×68(V) pixels (Figure 4), which includes 9 sub-arrays, each with different photodiodes and capacitor implementations (Table 1). The N-Well collection "islands" are surrounded by epitaxy and photo-generated carriers diffuse into the collection region [11]. On two edges of the pixel array, there are H & V

decoders, but as all the control and readout logic is inside each pixel, there are only digital buffers and pads outside the array. Control signal timing and voltage references are generated off-chip.

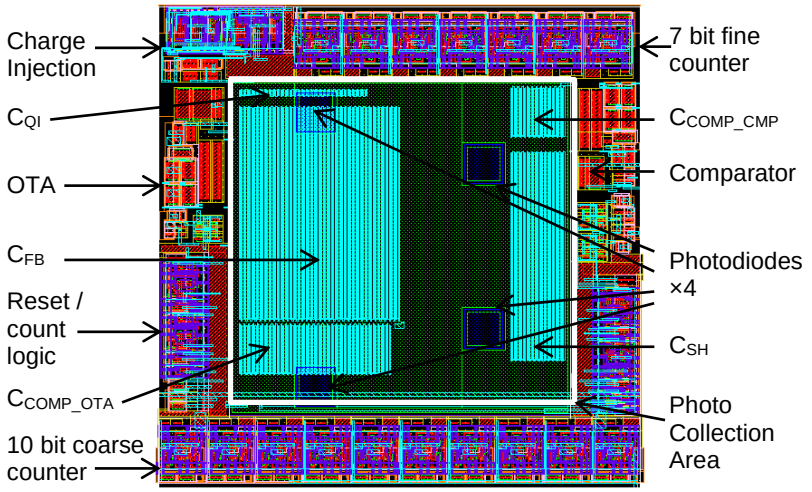

Figure 3 Pixel Layout

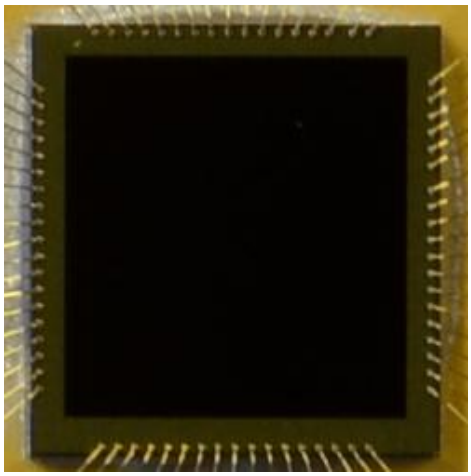

Figure 4 Sensor Microphotograph

Measurements - The charge integrator (QINT) is operating as expected, but there is a bug with the QINT reset logic. The control signals change on both clock edges, suggesting a problem with slew rate of the clock signal. The pixel will produce a number of coarse counts per frame before entering a locked state. A future device would include a Schmitt buffer on the clock signal of each pixel to ensure correct operation.

Fortunately, the fine conversion, which is the novel part of this pixel, is operating correctly, so the device was measured at lower light levels before a coarse count occurs, avoiding the logic bug. The device was illuminated by 640nm LED with integration time being varied and outputs recorded.

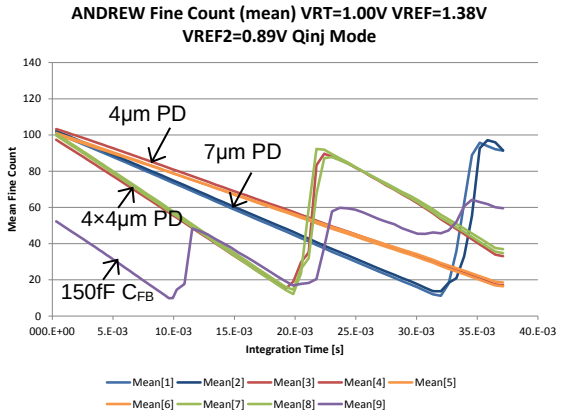

Figure 5 Charge Injection Fine Conversion

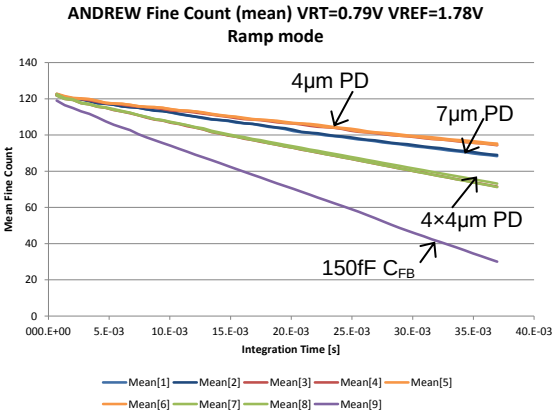

Figure 6 Ramp Mode Fine Conversion

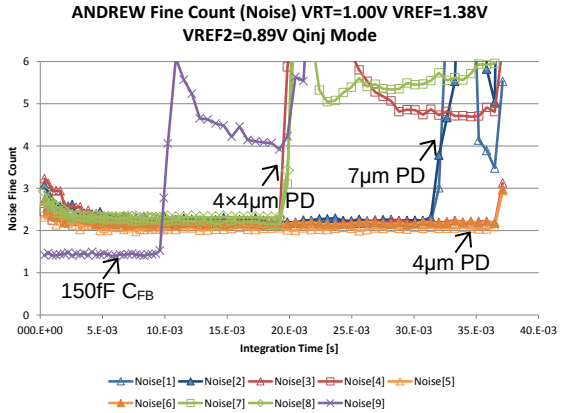

Figure 7 Charge Injection Fine Conversion Noise

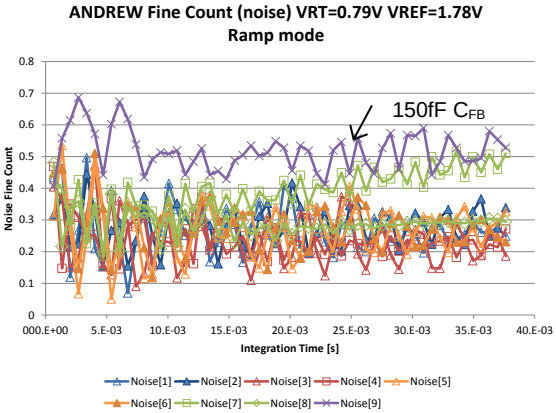

Figure 8 Ramp Mode Fine Conversion Noise

Type	1	2	3	4	5	6	7	8	9
Collection Node	1* 7×7µm	1* 7×7µm	1* 4×4µm	4* 4×4µm	1* 4×4µm	1* 4×4µm	4* 4×4µm	4* 4×4µm	4* 4×4µm
Implants	NWell	NW+DNW	NW	NW	NW_PIX	NW_PIX	NW_PIX	NW_PIX	NW_PIX
C_{FB}	300fF	300fF	300fF	300fF	300fF	300fF	300fF	300fF	150fF
Fill Factor	50%	50%	50%	50%	50%	50%	50%	50%	50%
QE	32%	32%	26%	49%	26%	25%	51%	50%	51%
I_{DARK}/Pix	127fA	128fA	116fA	169fA	114fA	112fA	181fA	177fA	152fA
Q_{inj} Noise	2.3	2.4	2.4	2.2	2.1	2.2	2.3	2.3	1.4
Q_{inj} Range	90	88	90	82	88	87	88	86	54
SNR_{Qinj}	31.9dB	31.3dB	31.3dB	31.4dB	32.4dB	31.7dB	31.5dB	31.2dB	31.6dB
Ramp Noise	0.27	0.29	0.23	0.28	0.28	0.28	0.44	0.30	0.52
Ramp Range	97	97	97	97	97	97	97	97	97
SNR_{Ramp}	51.0dB	50.5dB	52.4dB	52.1dB	50.9dB	50.8dB	46.8dB	50.1dB	45.4dB

Table 1 Photodiode Types and Pixel Performance

The QE values in Table 1 do not include fill factor. The increase in noise seen in Figure 7 occurs after a course count and is a result of the occasional mis-firing of the reset logic. The values for noise in Table 1 are average noise values before one coarse count occurs.

Conclusions

A hybrid analogue-digital pixel allows for easier scaling of pixel size with smaller process geometries without the loss of dynamic range found in analogue only pixels. The technique presented here demonstrates a fine conversion mode in charge counting pixels which results in a SNR improvement over of 52dB in ramp conversion mode and 32dB in charge injection conversion mode.

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