Time-resolved imaging device with high-speed modulators for fluorescence lifetime measurement system

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I. Introduction

Fluorescence provides a powerful means of achieving molecular contrast for a wide range of biological and medical applications. Particularly, fluorescence lifetime imaging microscopy (FLIM) [1]-[3], which is a nondestructive and minimally invasive method and can therefore be applied to living cells and tissues, is a great analysis tool in fundamental physics as well as in the life sciences. Recently, authors developed a high time resolution CMOS lock-in pixel imaging device [4] for fluorescence lifetime measurement system. By using new approach for fast charge transfer, so-called LEFM (lateral electric field modulation) [5], we achieved a sub-nanosecond charge transfer time to storage area from photo-sensitive area. In addition, the LEFM method can also help to reduce the noise components which are generated by a charge trapping under the MOS gate, because the proposed pixel using LEFM does not need any transfer gates between the pinned photodiode (PPD) and pinned storage-diode (PSD).

In this paper, the detailed design and implementation of the 2-stage charge transfer time-resolved imaging device with LEFM for true CDS readout is described. To demonstrate the prototype imaging device, we performed the device simulation and measurement. Using a technique with high-speed charge modulation of LEFM and 74ps pulse laser, the time-resolution of approximately 10ps has been attained for the first time as a CMOS-based time-resolved imager.

II. CMOS 2-tap lock-in pixel

A. Structure

An active pixel includes a PPD and two PSDs (SD_1 and SD_2) formed in optimized semiconductor substrate for LEFM implementation and three sets of gates (G_1, G_2, and TD). Fig. 1 shows developed 2-tap CMOS lock-in pixel used for fluorescence lifetime measurement. Each of two source follower outputs (SF_1 and SF_2) from each

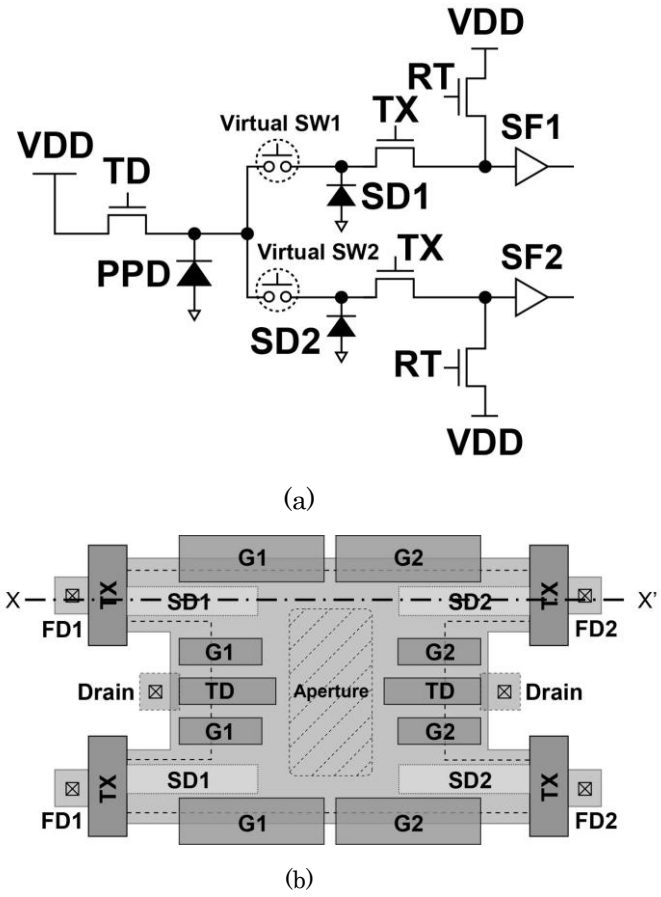
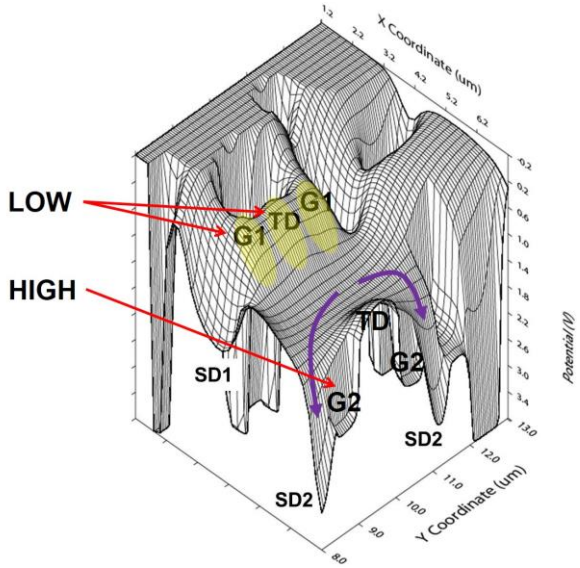


Figure 1: Developed 2-tap CMOS lock-in pixel for time-resolved imaging. (a) Schematic. (b) Layout.

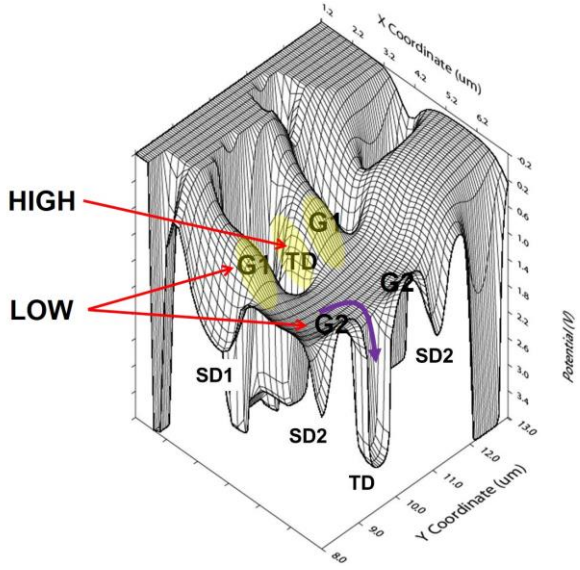
pixel is connected to each of two column readout circuits as shown in Fig. 1 (a). The SDs have a deeper potential well than that of the PPD. Therefore photo-charge in PPD is automatically transferred to the SDs, when a high voltage is applied to G_1 or G_2. In other words, virtual switches (SW_1 and SW_2) can be controlled by G_1, G_2, and TD. Fig. 1 (b) shows the layout of developed lock-in pixel. Each SD can store up to around $3ke^-$. In addition, all signal charges generated by photon in sensing area reach to the targeted SDs within 1ns.

B. Pixel operation principle

Fig. 2 shows 3-dimensional potential distributions with transfer mode and drain mode,

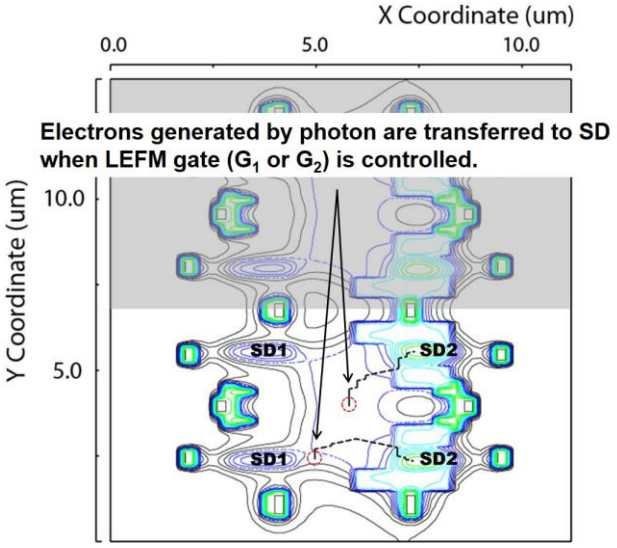


(a)

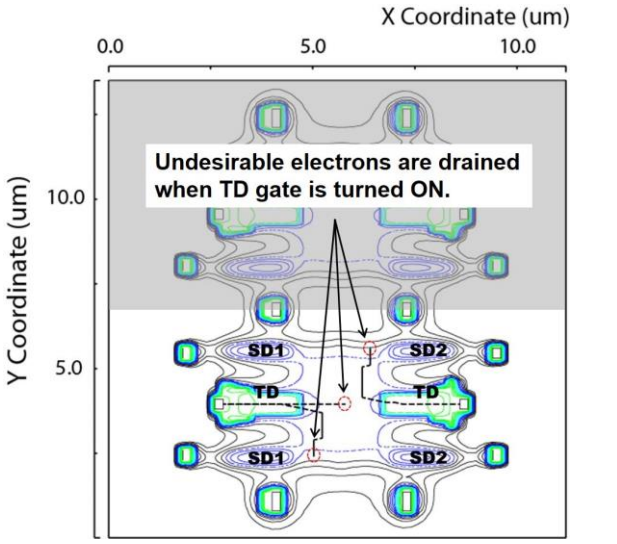


(b)

Figure 2: 3-D device simulation results. (a) Transfer mode (@ G_2=HIGH, G_1 & TD=LOW). (b) Drain mode (@ G_1 & G_2=LOW, TD=HIGH).



(a)



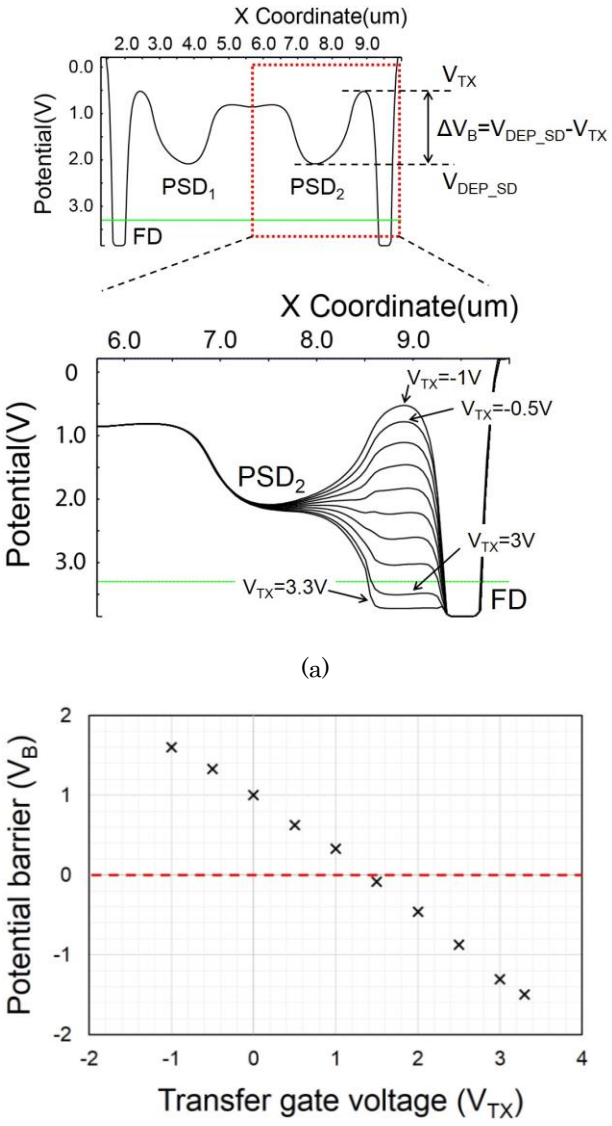
(b)

Figure 3: Charge transfer simulation results. (a) Transfer mode (@ G_2=HIGH, G_1 & TD=LOW). (b) Drain mode (@ G_1 & G_2=LOW, TD=HIGH).

respectively. As can be seen from these results, the potential barrier between PPD and PSDs, or PPD and drain node is perfectly disappeared by LEFM and TD gate. Then accumulated signal charges or undesirable charges is transferred to PSD or drain node, respectively.

Fig. 3 shows plots of equipotential lines and carrier transportations for two cases of charge-transfer mode and drain mode. The red circles mean the initial position of electrons before moving by the electric fields and black dot lines indicate the trace of movement of electrons. The direction of the electron flow is controlled by the gate voltage of G_1, G_2, and TD. The charge transfer time from the initial positions is less than one nanosecond, even though a generated electron is farthest away from the destinations (PSDs or drain node).

Two-stage charge transfer is one of the important techniques for reducing the in-pixel noise, because true-CDS operation can be performed by using this technique. Fig. 4 shows the simulation results for checking 2-stage charge transfer from PPD to PSD_2. The depleted potential diagram along with x-x' (see Fig. 1 (b)) is shown in Fig 4 (a). V_{DEP_SD} and V_{TX} mean that the deepest point of potential well at PSD and the highest point of TX (transfer gate) potential barrier, respectively. V_B means the voltage difference between V_{DEP_SD} and V_{TX}. We trace the



(a)

(b)

Figure 4: Simulation results for confirming 2-stage charge transfer from PSD to FD node. (a) Depleted potential changes by TX gate voltage. (b) Plot of potential barrier (ΔV_B) as a function of the TX gate voltage.

changes of potential barrier (V_B) by supplying the different TX gate voltages. This changing of V_B is plotted as shown in Fig. 4 (b). In this plot, the potential barrier of 0V or below means that there is any barriers for transferring the signal charges to FD node. In other words, all accumulated charges can be perfectly transferred as signal without the loss and residues. To design the successful 2-stage charge transfer structure, sufficiently large dimension of PSD is required for increasing the sensitivity, but at the same time the deepest point of the depleted potential well of PSD should be away from the FD region to prevent the electrons in FD scooping by TX gate

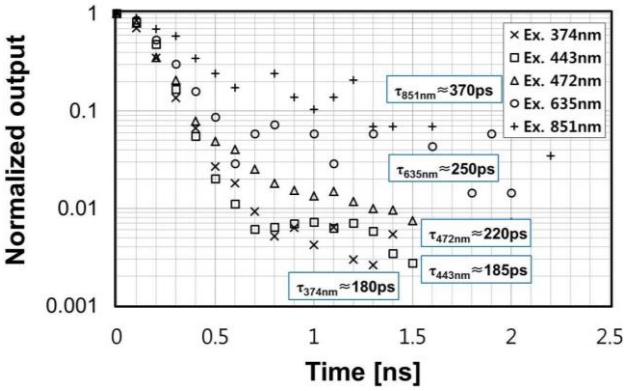


Figure 5: Developed time-resolved sensor's intrinsic responses with different laser diodes for excitation.

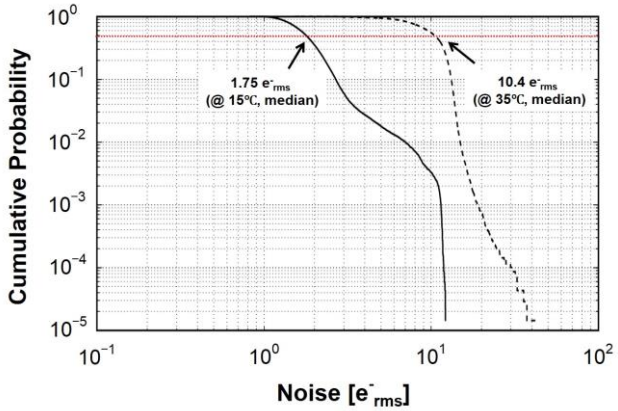


Figure 6: Temporal random noise of the prototype imager (@ 15℃).

operation. This charge injection leads to degrading the image quality, i.e., image lag and increase of the random noise. In our pixel design, we keep the potential margin between the PSD and FD region over 1V for avoiding the charge injection. In addition, we simultaneously attain a quite large full well capacity (FWC) of PSD by optimizing the pixel structure.

III. Measurement results

A prototype image sensor is implemented with 0.11μm 1-poly 4-metal CMOS image sensor (CIS) technology. An intrinsic response time is also very important parameter for realizing a precise lifetime measurement system. Fig. 5 shows the intrinsic responses of the developed time-resolved imager with different light sources. The LEFM pixel has its own intrinsic response which is determined by the dispersion of light spot on the sensing area and the dispersion of the transfer time. In the measurement of intrinsic response, excitation lights from 374nm to 851nm are

Parameter	Value
Process technology	0.11 μm 1P4M CIS process
Total area	7.0 (H) mm X 9.3 (V) mm
Number of effective pixels	256 (H) X 512 (V)
Pixel size	11.2 (H) μm X 5.6 (V) μm
Conversion gain	85 μV/e$^-$
Fill factor	16.7 %
Full well capacity (@ SD)	3.24 ke$^-$
Full scale of ADC (ΔV_{REF})	0.3 V
Temporal random noise	1.75 e$^-_{RMS}$ (@ median, 15℃)
Time resolution (Ex. 374nm)	10.8 ps (@ median, 50 frames avg.)
	13.9 ps (@ median, single frame)
Frame rate (Max.)	15 fps

Table I: Performance summary of the imagers.

illuminated directly and uniformly on the sensor chip. As can be seen from Fig. 5, the developed imager achieves a very short intrinsic response of approximately 180ps with 374nm laser diode. Even if a longer wavelength laser diode of 851nm is used as light source, still enough fast intrinsic response of around 370ps is attained.

Fig. 6 shows the noise performance of imager. The low noise level of 1.75e$^-_{rms}$ at 15ºC with an analog gain of 128 is achieved by optimized pixel structure with LEFM and true-CDS operation. The sensor performance and characteristics are summarized in Table I. The number of effective pixels is 256(H)×512(V). A pixel size is 11.2(H)×5.6(V) μm^2 and its fill factor is 16.7%.

IV. Summary

A high time-resolution 2-tap CMOS lock-in pixel sensor is implemented for fluorescence lifetime imaging. Particularly, the developed time-resolved pixel device with 2-stage charge transfer and the LEFM helps to achieve the high-speed charge modulation, short intrinsic response, and low noise performance. In conclusion, the developed imaging device will be one of key technologies in next-generation biological and medical imaging tools.

Acknowledgment

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