Compact time-gated analog counting SPAD-based pixels for high resolution, single-photon, time-resolved imagers

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Abstract **– In this work, three different pixels for time-resolved, single-photon imaging are investigated. The pixels include a Single-Photon Avalanche Diode (SPAD), a gating circuit and an analog counter. The presented structures aim at achieving sub-nanosecond gating performance with a reduced number of transistors to enable high resolution imaging with a high fill factor. The pixels have been implemented in a test chip and their photon counting capabilities are here presented.**

Fluorescence Lifetime Imaging Microscopy and other scientific and bio-medical imaging techniques require high resolution, time-resolved, low flux imagers. Solutions available today, such as Electron-Multiplying CCDs and Intensified CCDs, offer high photon detection efficiency and low noise at the expense of a high cost at detector and system level. A fully CMOS solution based on SPADs represents a valid alternative when the photon flux is relatively large (around 1k photons/sec/μm^2), thanks to its good performance in terms of frame-rate and timing resolution (<1 ns). Despite the SPAD's intrinsic digital nature (a current pulse is generated for every detected photon), digital implementations of in-pixel time-stamping or time-gated photon counters suffer from extremely low fill-factor. The problem can be overcome by accumulating the photon counts in the analog domain in a capacitance within the pixel, and convert it back to the digital domain after the acquisition process [1] [2] [3] [4] [5] .

In this work, a comparison of three analog pixel implementations is presented. Two novel NMOS-only pixel topologies with a reduced number of transistors per pixel are described, enabling low-pitch (below 20 µm), high fill-factor (above 20%), suitable for high-resolution imagers with sub-nanosecond time gating. Small linear arrays of the proposed pixels have been implemented in a test chip in 150nm CMOS Technology. A slightly different version of one of the structures has also been implemented in a 100×100 array in 0.35 HV CMOS technology.

The first implementation has been presented in [6] The pixel is designed to generate a voltage drop on the analog counter for every photon being detected while the gating window is open. Its schematic diagram is shown for completeness in Figure 1. Whenever a photon is detected, a relatively long (hundreds of nanoseconds) voltage pulse is generated at the anode of the SPAD. The pulse is narrowed in time by a logic AND between the (clamped) pulse and a slightly delayed, inverted copy of it, and determines a voltage drop on the analog counter through transistor M9. Gating is performed by activating the AND gate only within a selected timing window. The AND gate is implemented with the series of two NMOS transistors and controlled by the WIN signal, operating on the source voltage of M8. PMOS devices are required to limit the power consumption.

Figure 2 shows the pixel schematic for the second topology and its functionality. It consists of 7T+1MOSCap. M1 is the quenching resistor. MC2, a MOS working as a capacitor, and M3, operated in the linear region, act as a C-R high-pass filter. When an avalanche is generated, a fast pulse propagates to the gate of M5, implementing the time gating mechanism. If the pulse falls within the time gate pulse provided at the source of

M5, a voltage drop occurs on the analog counter MC6. The pixel has been designed to generate a linear voltage drop within a wide range of MC6 voltages. It is worth noting that the voltage drop occurs only when the pulse at node 2 exceeds by a threshold the low level of the WIN signal. Transistor M4 resets the analog counter. Transistors M7 and M8 are required to read out the pixel value.
The performance of this topology is limited by the HPF. Ideally, the pulse at node 2 should be large in intensity but short in time to obtain a small minimum gating window and a uniform voltage step. This desired behavior is in contrast with the present pixel architecture, since M3 is operated at a fixed V_{GS} voltage (V_B). For large V_B, pulses are short but with a limited excess voltage, while at low V_B pulses are large in amplitude but long in time.

The third topology overcomes this limit using two additional elements (M9 and MC10), as shown in Figure 3. The transistor M3 is controlled by a slightly delayed version of the avalanche pulse, rather than biasing it at a fixed voltage. In this way, the pulse at node 2 can be higher in voltage, but shorter in time (if we consider the pulse active only when it exceeds the M5 transistor's threshold voltage).

The three structures have been implemented in small linear arrays in a test chip. For easiness of implementation, the pixel pitch has not been minimized. Figure 4 shows the histograms of the output voltage of the three pixel structures obtained after multiple acquisitions. Reference voltages have been tuned to obtain the same voltage step in each of the three structures. The voltage step has been set to guarantee a shot-noise limited operation for all the structures. Each peak in the histogram represents a different discrete photon count. The first structure obtains the best performance, as peaks are well separated from each other even for larger counts, but requires both NMOS and PMOS transistors. The second and third structures are potentially more aggressive in terms of fill factor, at the expense of lower photon-count resolving capabilities.

A 100×100-pixel array of a modified version of the second topology has been implemented in 0.35 HV CMOS technology. A metal capacitor has been used for the high pass filter. The pixel pitch is 25µm, leading to a 22% fill factor. The chip micrograph is shown in Figure 5. A much higher fill factor can be obtained with a more advanced technology process. Unfortunately, the pixel exhibits a large non uniformity due to the underestimation of the SPAD resistance, which caused excessive attenuation of the pulse at node 2 by the C-R filter.
The table in Figure 6 quickly compares the present solutions with respect to the state of the art.

References

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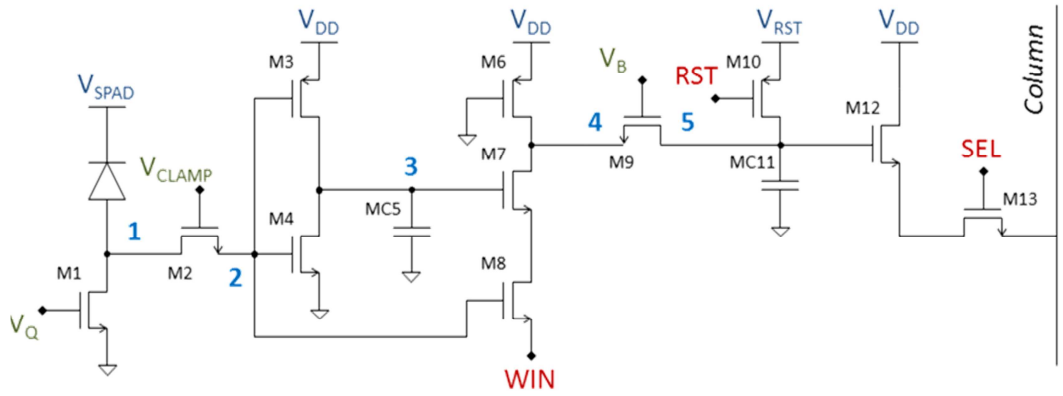


Figure 1 - Schematic of the first version of the pixel. M3 and M4 operate as an inverter. M6, M7 and M8 implement the AND gate, which is enabled only when the WIN signal at the source of M8 is set low. M9 tunes the voltage drop occurring on MC11 when a photon is detected within the gating window.

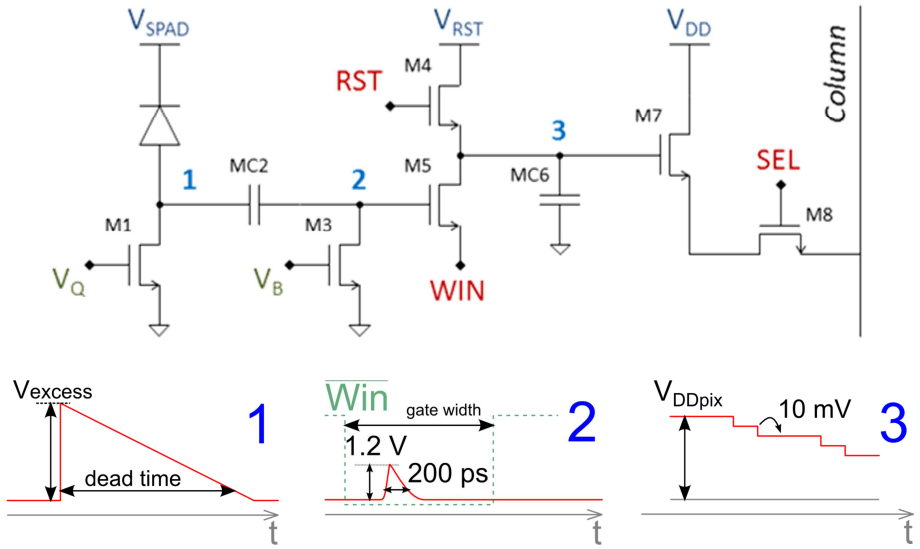


Figure 2 – Schematic of the second version of the pixel. MC2 and M3 act as a high pass filter. When the SPAD detects a photon, the voltage step at node 1 translates into a narrow, short pulse at node 2. If this pulse falls within the gating window WIN provided at the source of M5, a voltage drop is generated at the analog counting node MC6.

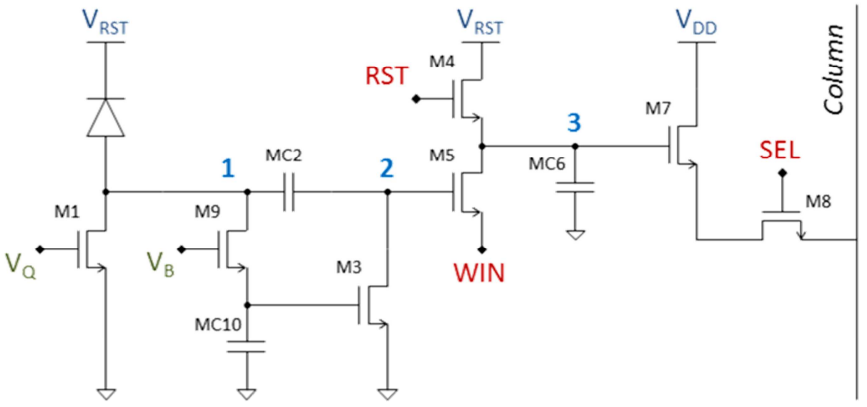
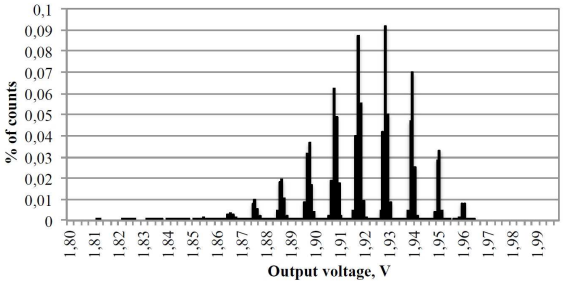
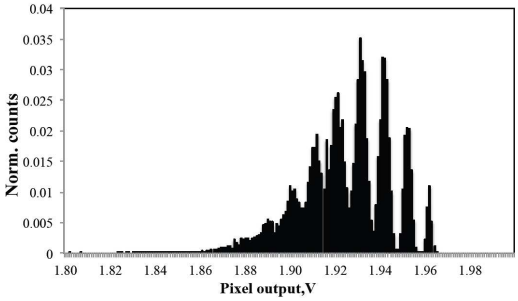


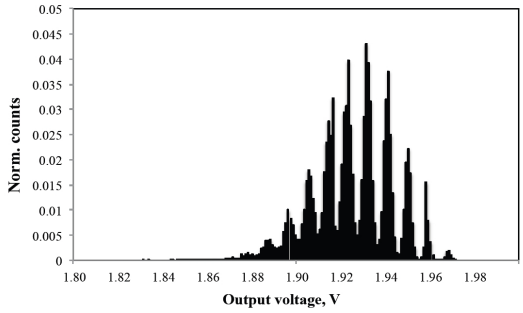
Figure 3 - Schematic of the third version of the pixel. The additional transistors with respect to the second version of the pixel are M9 and MC10. The effect is that the pulse at node 2 is higher in voltage and shorter in time (if we consider the pulse active only when it exceeds the threshold voltage of M5).



(a)

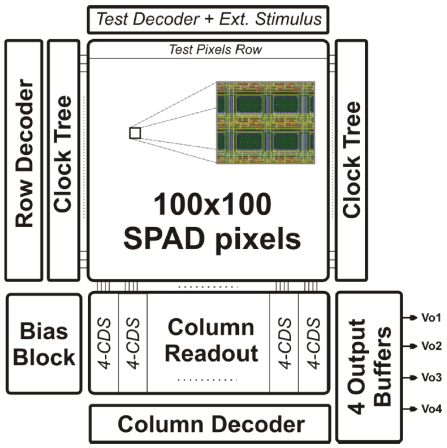


(b)



(c)

Figure 4 - Histograms of the pixels output voltage across multiple acquisitions. Each peak represents the output voltage for 0, 1, 2, 3, ... photon counts (from right to left, respectively). Reference voltages have been applied to obtain the same voltage step in each structure. Ideally, peaks should be well separated from each other, so that photon counts are clearly identifiable. The first version of the pixel (a) provides the best performance, thanks to the joint use of NMOS and PMOS. In the second version (b), the first peaks are well separated, and start merging at the 4th peak. The third version (c) clearly shows an improvement with respect to the second one, at the expense of a lower fill factor. All the structures exhibit a shot noise limited operation.



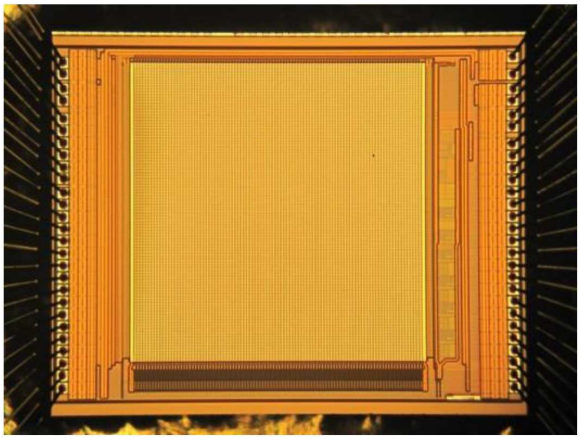


Figure 5 - Architecture and Chip Micrograph of the 100×100-pixel array implemented in 0.35 HV CMOS technology.

	[1]	[2]	[3]	This work - Pixel v1 -	This work - Pixel v2 -	This work - Pixel v3 -	This work - Array -
Process	0.35um HV	130nm CIS	0.35um HV	150nm	150nm	150nm	0.35um HV
Pixel num.	32×32	320×240	160×120	1×40	1×15	1×15	100×100
Pixel size	25µm	8µm	15µm	25µm	25µm	25µm	25 µm
Fill Factor	20.8%	26.8%	21%	12.6%	12.6%	12.6%	22%
Transistors per pixel	12	9	7 + 1MOSCAP	12	7 + 1MOSCAP	9 + 1MOSCAP	6 + 1METALCAP + 1MOSCAP
Time-gate width	>1ns	Not tested	0.75ns	0.95ns	<1ns (simulation)	<1ns (simulation)	<1ns (simulation)

Figure 6 - Summary table.