Monolithic Active Pixel Sensor Development for the Upgrade of the Inner Tracking System of the ALICE Experiment at CERN

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ABSTRACT

ALICE is the first experiment on the Large Hadron Collider (LHC) at CERN to plan an important upgrade entirely based on monolithic active pixel sensors (MAPS): the Inner Tracking System (ITS) will be upgraded to significantly improve its particle tracking capability[1]. The sensor development is described and measurement results on prototypes are presented.

1. REQUIREMENTS AND TECHNOLOGY CHOICE

After the successful installation and operation of a vertex detector based on MAPS in the STAR experiment [2], the ALICE experiment has decided to fully replace its ITS in 2018 by a new detector (Fig. 1) consisting of seven cylindrical layers of MAPS covering an area of about 10 m^2 with about 12.5 billion pixels. Fast insertion and removal are necessary to allow yearly maintenance. This new detector should reduce the material budget or the radiation length per layer X/X0 from 1.14 to 0.3 %, the pixel size from 425x50 to 28x28 μm^2, and the first layer radius from 39 to 22 mm.

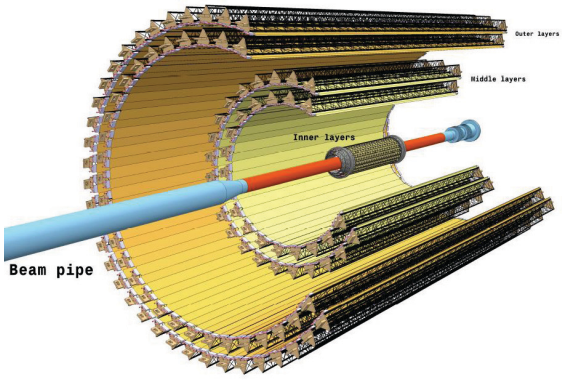

Figure 1. Layout of the new ALICE ITS with 3 inner and 4 outer layers spanning a range in radius of 22 to 400 mm.

The TowerJazz 180 nm CMOS imaging sensor process [3] has been chosen for the sensor development as it is possible to use full CMOS in the pixel due to the offering of a deep pwell (Fig. 2) and also to use different starting materials. This technology was also expected and later on experimentally demonstrated to offer sufficient radiation tolerance for the modest ALICE requirements (see Table 1).

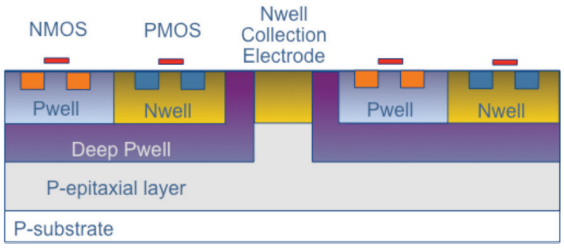

Figure 2. The deep pwell prevents nwells containing circuitry from collecting signal charge from the epitaxial layer and therefore allows full CMOS within the pixel.

	Inner layers	Outer layers
Max. silicon thickness	50 µm	
Chip dimensions	30 mm x 15 mm	
Spatial resolution	5 µm	10 µm
Max. integration time	30 µs	
Max. power density	300 mW/cm^2	100 mW/cm^2
Detection efficiency	> 99%	
Fake hit rate per pixel and per readout	< 10^{-5}	
TID radiation hardness	2700 krad	100 krad
NIEL radiation hardness	1.7 10^{13} n_{eq}/cm^2	10^{12} n_{eq}/cm^2

Table 1. Overview of the main specifications

2. CHIP DEVELOPMENT

Several developments satisfying ALICE requirements based on rolling shutter architectures were started, but reducing power consumption well below 100 mW/cm^2 allows a significant reduction of the material in the detector. Also reducing integration time to only a few µs limits overlap of events and background. The ALPIDE (ALICE Pixel Detector) development further described

below and now adopted as the baseline for the ITS upgrade was started to reach these lower values for power consumption and integration time. It is based on a low power 40nW analog front end in each pixel which outputs a logic "1" if the collected charge in the corresponding pixel is above a specific threshold, combined with a hit-driven readout.

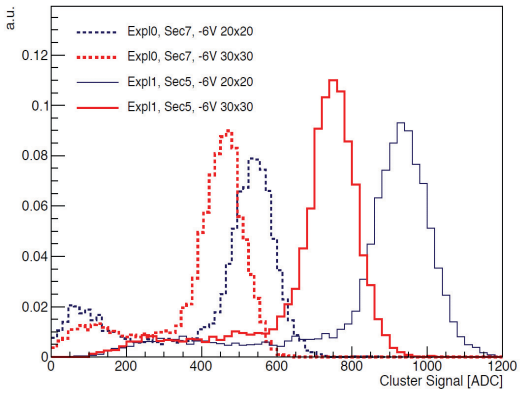

Figure 3. ^{55}Fe spectrum obtained by Explorer0 and Explorer1.

Power is consumed in the sensor chip in the analog and digital circuitry, and also to transmit the data off-chip. Analog power consumption is determined by the collected charge over capacitance (Q/C) ratio [4], requiring pixel sensor optimization. Several prototypes allowing reverse substrate bias were submitted to optimize the sensor for Q/C through design but also using different starting materials, and measured [5]: reverse substrate bias reduces input capacitance and average cluster size, and increases efficiency (= the probability to detect a particle traversal) for a certain charge threshold. Fig. 3 shows how the signal from a ^{55}Fe source improved between two generations of Explorer prototype chips due to a reduction of circuit input capacitance from about 5 to 2 fF.

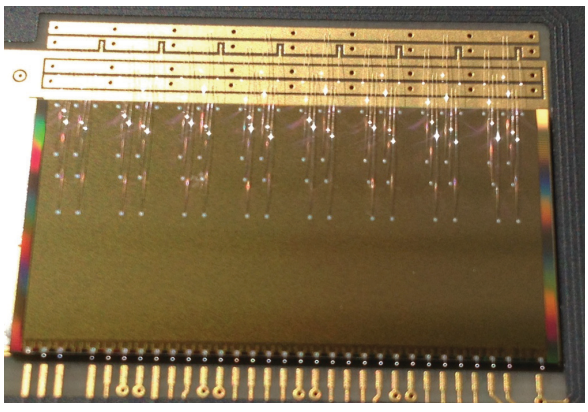

Figure 4. First full size (3x1.5 cm^2) ALPIDE prototype.

Digital power consumption depends on the on-chip architecture and also on cluster size. In the ALPIDE, a priority encoder circuit provides the address of the first hit pixel in a sector, and subsequently resets it, so that during the next clock cycle the address of the next hit pixel is made available. This continues until all hits in the sector have been read out. Power is consumed only if hits are present.

A first full size prototype (see Fig. 4) containing 1024 x 512 pixels in 3 x 1.5 cm^2 was fabricated last year and was extensively tested [6]. Measurement results are reported in the next section.

A second full size prototype has just come back from fabrication. It includes chip-to-chip communication functionality required for the outer layers to reduce the number of lines: sets of 7 chips are grouped together, and one of them – the master – acts as the interface to the outside world: it propagates clock, command and control information to the other chips, and regroups the data from the set of 7 chips to transmit it off-detector. Power consumption is reduced by deactivating the high speed data transmission unit on the six other chips. For the inner layers data is transmitted at 1.2 Gb/s. For the outer layers data has to be transmitted over a much larger distance on a flex circuit, and the signal attenuation at this data rate would be too important. Data rate for the outer layers was therefore reduced to 400 Mb/s, regrouping the data of only 7 chips.

In these two prototypes only one bit of memory per pixel has been foreseen, therefore preventing taking new data before completing data transfer from the pixel matrix to the periphery of the chip. This dead time has been reduced by operating 32 priority encoders in parallel, but would practically be fully eliminated by implementing more than one memory element per pixel. The submission of a third full size prototype is being prepared, which will include three memory bits per pixel and the high speed data transmission unit which can be configured to operate at 1.2 Gb/s for the inner layers and 400 Mb/s for the outer layers. We expect a power consumption of less than 200 mW or less than 50 mW/cm^2 for this chip, but still plan further power optimization for the final chip, which should go into production next year.

3. MEASUREMENT RESULTS ON THE FIRST FULL-SCALE PROTOTYPE

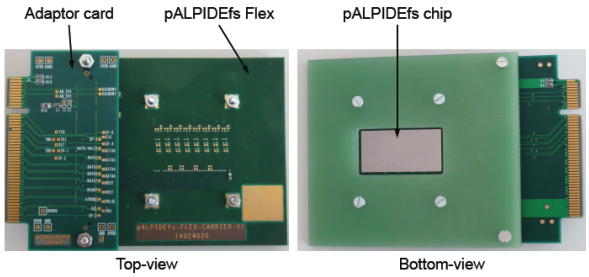

Figure 5. ALPIDE prototype flip-chip laser soldered on a flex.

The first full size prototype shown in fig. 4 was thinned down to its final thickness of 50 µm and flip-chip bonded to a flex by laser soldering (fig. 5), and measured [6].

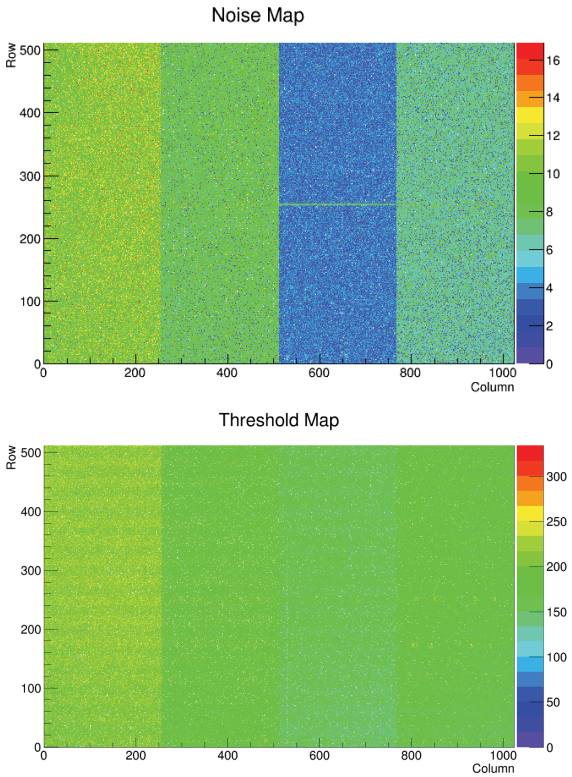

Figure 6. Noise and charge threshold map observed on the first full scale ALPIDE prototype.

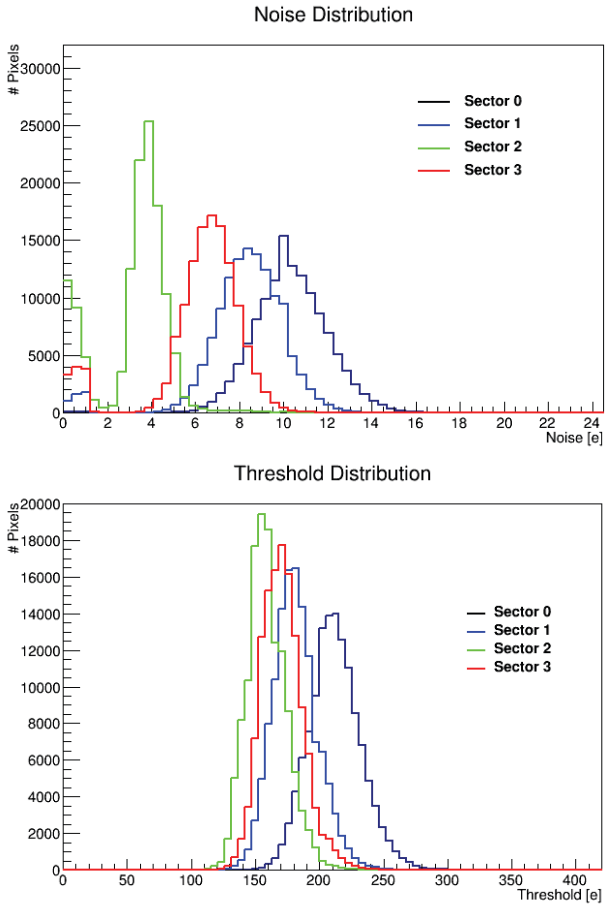

Figure 7. Noise and charge threshold distributions observed on the first full scale ALPIDE prototype.

Fig. 6 shows charge threshold and noise map over the pixel matrix: the band structure reflects the differences in pixel designs in the four sectors on this prototype. Fig. 7 shows the distributions and it can be observed that threshold spread is significantly larger than the noise. This is acceptable, but not desirable, and therefore significant design effort is being carried out to reduce this spread. Similar observations were made on chips before thinning and soldering indicating these processes do not degrade the chip performance.

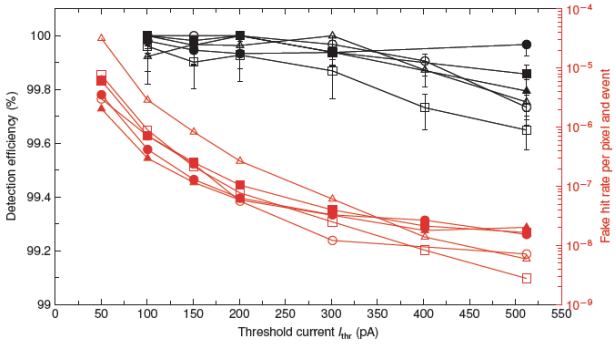

Figure 8. Efficiency and noise occupancy versus threshold setting observed in a particle beam. Results refer to chips thinned to 50 µm: 3 non irradiated (solid symbols) and 3 irradiated (open symbols) with neutrons at 10^{13} 1MeV n_{eq}/cm^2.

This first full size prototype was also tested in a particle beam (5-7 GeV π^-): fig. 8 shows detection efficiency and noise occupancy as a function of the current determining the charge threshold (50 pA corresponds to a charge threshold of about 80 electrons, 500 pA to about 180 electrons). It can be observed that a detection efficiency well above 99 % with a fake hit rate per pixel and per event of less than 10^{-5} can be achieved (only 20 pixels out of ~500 000 on the chip were masked). Fig. 9 shows the cluster size and the position resolution, and indicates a position resolution of 5 µm can be achieved. Fig. 8 and 9 report measurements both for unirradiated and irradiated devices, and illustrate that this first full size prototype satisfies the ALICE requirements (Table 1), and that performance remains practically unaffected for the NIEL radiation levels foreseen.

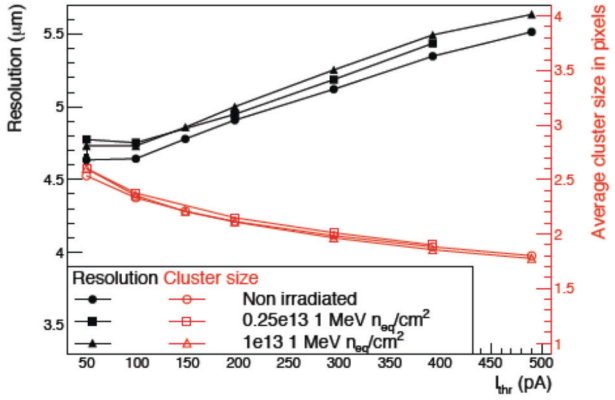

Figure 9. Spatial resolution and cluster size observed in a particle beam (5-7 GeV π^-).

The measurements in a particle beam were carried out using a telescope with seven sensor chips, six of which were used as a reference for the device under test. Since the position resolution is significantly better than the pixel pitch (~28 μm in both X and Y), and further refined by using several reference sensor chips one can study in more detail the pixel response as a function of the position of incidence of the particle. This is illustrated in Fig. 10 for the cluster size. As expected, cluster size is small if the particle is incident near the charge collection electrode in the pixel center, and larger if the particle is incident near the boundary of different pixels.

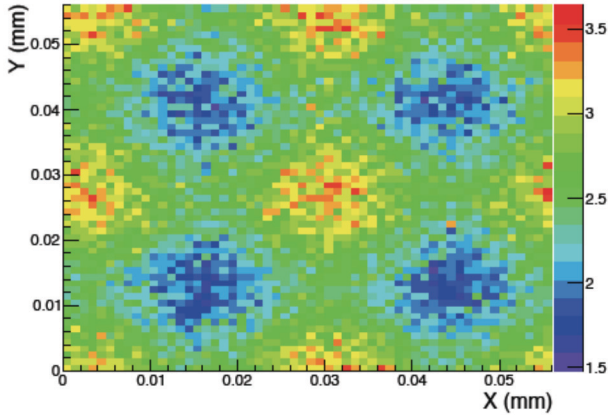

Figure 10. Cluster size versus position of the cluster within the pixel

4. CONCLUSIONS

ALICE is the first LHC experiment at CERN to adopt monolithic active pixels for an important upgrade at the LHC. It is foreseen to fully replace its inner tracker system with a new 10 m^2 detector constructed from 4.5 cm^2 sensor chips. First full size prototypes have been verified to satisfy requirements. Further development is foreseen this year to include features important for system operation like high speed and chip-to-chip data transmission, and multiple data memories per pixel, and to further optimize pixel-to-pixel uniformity and power consumption.

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