Multi-Bit Quanta Image Sensors

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Abstract *– Various performance aspects of the multi-bit Quanta Image Sensor (QIS) concept are discussed.*

I. Introduction

The single-bit Quanta Image Sensor (QIS) concept was introduced in 2005 (as a digital film sensor) as a possible evolution of solid-state image sensors with integrated signal collection and scanned readout (like CMOS image sensors today) where pixels are shrunk to sub-diffraction limit size, the number of pixels increased substantially to gigapixel or more, read noise reduced to allow reliable single photoelectron detection, and readout rate increased to avoid saturation of the sensor under normal imaging conditions [1]. Image pixels and image frames are then formed from the resultant x-y-t data cube. The data cube is composed of bit planes or fields, with pixels formed from "cubicles" of bits in a localized region of 2D space and time. Such a temporally and spatially oversampled imaging concept results in challenges for realizing the specialized pixel (called a "jot") in accessible foundry technologies, and implementing novel readout electronics meeting noise, speed and power requirements. Additional challenges are in creating a methodology for developing image pixels from the jot data. These challenges and some progress were discussed in more detail in subsequent publications [2,3]. Meanwhile, binary image sensors that are not necessarily sensitive to single photoelectrons have been explored independently [4-6] and single-photon avalanche detector (SPAD) arrays have also been considered for QIS devices.

In the single-bit QIS, each photodetector ("jot") in the array is binary in nature, with a signal corresponding to either no photoelectron, or one (or more) photoelectrons. The response of the sensor, in terms of bit density (local density of jots that have received a photoelectron during the integration period), gives rise to the so-called D-log H S-shaped response curve, well known in film since the late 1800's [7]. Detailed analysis of the response of the QIS was presented in 2013 [8].

II. Flux Capacity

In order to handle a photon flux ϕ under normal lighting conditions, the jot density and readout rate must be relatively high. The flux capacity ϕ_w of the single-bit sensor is given by (flux for quanta exposure H=1):

$$\phi_w = jf_r/\sigma\bar{\gamma}$$

where j is the jot density (jots/cm^2), f_r is the field rate, σ is the shutter duty cycle and $\bar{\gamma}$ is the average quantum efficiency. For example, with a jot pitch of 500nm, 1000fps field rate, unity duty cycle and 50% avg. QE, the flux capacity is 8x10^{11} photons/cm^2/s which at F/2.8, QE=50%, lens T=80%, scene R=20%, corresponds to ~400 lux at the scene (yielding H=1 at the sensor). It can be seen that sub-diffraction-limit jot density and field rate is driven mostly by flux capacity and not necessarily by improved spatial or temporal resolution of the final image. The sub-diffraction jot pitch requires use of advanced-node processes that are expensive today. The high readout rate creates challenges in controlling power dissipation in the readout circuit, although significant progress has been made recently [9].

While analyzing the read noise requirements for single-bit QIS devices, it was found that if the read noise was low enough, such as 0.15 e- rms, then the ability to discriminate between no photoelectron, and at least one photoelectron was quite satisfactory, achieving a low bit error rate of under 1/2500. In fact, probably higher bit error rates could be tolerated. Nevertheless, it was also observed that if one indeed achieved such a low read noise, for example, through the use of a high conversion gain of say, 1mV/e-, discriminating between 0 and 1 photoelectron was essential the same difficulty as discriminating between say 11 and 12 photoelectrons. All that is required is increasing the bit depth of the ADC from one bit to *n* bits, where the digital number (DN) from the ADC corresponds directly to the number of photoelectrons in the jot. (Now the meaning of the term jot has been stretched from its original meaning.) Thus, it became evident that one should also consider multi-bit QIS devices where we retain most of features of the QIS, but allow each jot to hold more than one photoelectron up to a full well capacity FW given by 2^n-1. The flux capacity of the QIS increases to:

$$\phi_{wn} = jf_r(2^n - 1)/\sigma\bar{\gamma}$$

However, the bit depth *n* cannot be extended too far for a number of reasons.

First, it is desired to keep the conversion gain very high to ensure low read noise, and this limits the full well which has grown from 1 electron to $(2^n - 1)$ due to voltage range constraints on the signal chain in advanced technology nodes.

Second, gain variation from jot sense node capacitances and other amplification stages, will lead to errors in accurate photoelectron counting. Ideally,

if the gain is G, the gain variation $\delta G/G$ should be less than $1/2^n$, and more likely less than$1/2^{n+3}$. Thus, for 1% gain variation, the bit depth *n* should be no more than 6, and perhaps no more than 4 for accurate counting. On the other hand, the utility of accurate photoelectron counting to the nearest photoelectron, for counts approaching 100 photoelectrons is not clear when considering shot noise, and may thus be moot in most imaging applications.

Third, the power required for the ADC grows at least linearly, and for some designs, exponentially with bit depth *n*. On the other hand, for constant flux capacity, the field rate or jot density can be traded for bit depth *n*. Reduction of either, particularly field readout rate, results in a reduction in power dissipation that may partially or entirely compensate for the increase in ADC power.

III. ADC Bit Depth

We have performed a preliminary study on the impact of bit depth on power dissipation in the quanta image sensor. A test chip has been designed in XFAB's XS018 (180nm) image sensor process that contains several different ADC designs and taped out. A schematic of the test chip signal chain is shown in Fig. 1.

Each ADC's bit depth can be dynamically varied from 1 to 5, thus allowing for concomitant field rate reduction up to 32x for constant flux capacity. A regular 4T CMOS APS pixel design was used since the focus was on the tradeoff between bit depth, ADC power, total readout power and field rate. ADC designs included a 1b ADC used for the baseline QIS readout, a single-slope ADC (power scales exponentially with bit depth at same field rate), and two algorithmic ADCs – successive approximation and cyclic. Post-layout extraction and simulation leads to the power estimates shown in Fig. 2. The 1b ADC was previously proven to operate at record low FOM of 2.5pJ/b including gain and ADC power [9].

It can be seen that the single-slope ADC power remains relatively flat with increasing bit depth and decreasing speed, but both algorithmic ADCs show a favorable decline in power dissipation. However, area utilization is unfavorable for the successive approximation ADC and the cyclic ADC is more complex to design. The test chip is in fabrication and we hope to see silicon by the end of summer.

IV. Non-Linearity

The linearity of the sensor response is directly related to the full-well bit depth *n* [8]. The single-bit QIS has a non-linear response and high over-exposure latitude. The non-linearity in the sensor comes from the low (one electron) full well of the single-bit QIS. As soon as one electron is collected by the jot, it is full, and additional electrons collected in the same jot do not increase the signal from the sensor. Thus while on average each jot may have received one photoelectron at a quanta exposure H=1, due to this process typically only 63% of jots are occupied, many with more than one photoelectron, the remainder are "empty". As the bit depth increases from 1 to *n*, there is a continual decrease in non-linearity (the signal becomes more linear) and decrease in over-exposure latitude, as illustrated in Fig. 3. By *n*=5, the strong non-linearity has nearly vanished and the response approaches the linear response of the regular CMOS image sensor. This is because now each jot can contain, say, 31 electrons before it saturates, providing a larger linear range of response.

The comparative non-linearity of the response is shown in Fig. 4. The dashed line shows the relative response of an ideal conventional CMOS image sensor, which is linear up to an exposure that yields full-well saturation, and then flat beyond that. Let's define a relative exposure of unity as the exposure where, on average, each pixel or jot has received FW photoelectrons. The response of a multi-bit QIS for various bit depths *n* is also shown in Fig. 4. For large *n* (*n*=6) the response is close to that of the conventional CMOS image sensor. As *n* becomes smaller the non-linearity increases and the overexposure latitude also increases down to *n*=1 for the single-bit QIS. The number of photoelectrons collected for a relative exposure of unity depends on *n*, and for a single photosite, this impacts SNR due to shot noise. To collect the same number of electrons for smaller values of *n*, either the number of fields must be increased and digitally summed, or more neighborhood jots must be aggregated, or some combination, since this number ultimately determines the image pixel SNR.

At a relative exposure of unity, the quanta exposure $\mathrm{H} = \mathrm{FW} = 2^n - 1$, and expected % capacity saturation is given by:

$$\%Cap = 100\left[1 - \sum_{k=0}^{FW}\left\{1 - \frac{k}{FW}\right\}\frac{e^{-H}H^k}{k!}\right]$$

which can be fit by $\%Cap = 100\left[1 - e^{-n^u}\right]$ with u=0.60 yielding %cap=0.63, 0.78, 0.85, 0.90, 0.93 and 0.95 for *n*=1,2,3,4,5,6 respectively (see relative exposure of unity in Fig. 4) revealing some sense of the non-linearity of the response.

V. Selectable Non-Linearity

It is interesting to consider a multi-bit QIS, with say *n*=2, so that each jot could hold 0, 1, 2 or 3 photoelectrons, and where the response beyond 3 is coded as 3, either due to physical capacity of the jot, capacity of the analog signal chain, or bit depth of the ADC. (In fact, for small *n*, only the latter of these is truly likely). Thus, assume a 2-bit ADC. The response of the sensor will have the response curve shown in Fig. 3 for *n*=2 with its associated non-linearity.

Suppose we now took the same data and reprocessed it *postcapture* so that if the signal were greater than 1, that is, 2 or 3, it was recoded as 1. This means the FW for the same data has been reset to 1, and now reflects the non-linear response curve of the single-bit QIS, with an effective increase in relative exposure and worse SNR. For the multi-bit QIS and similar systems, the linearity of the response can be adjusted postcapture.

One can also imagine a multi-bit QIS, where the ADC bit depth is dynamically adjustable to alter the linearity of the response curve. Adjust to single-bit to get maximum non-linearity, and perhaps increase field rate to maintain flux capacity and SNR, or, adjust to multi-bit depth $n>1$ to get higher linearity, and adjust the field rate down to maintain flux capacity and reduce power dissipation.

VI. HDR Operation

The multi-bit QIS can be operated in an HDR mode by varying the shutter duty cycle across multiple fields as was analyzed for the 1b QIS [8]. As with the 1b QIS, the increase in dynamic range is offset by a decrease in low-light sensitivity and exposure-referred SNR (SNRH) for the same total frame integration period. An example is shown in Fig 5 with 10x increase in DR, minimal SNRH dips, and good contrast for brightly lit objects (no wash out). Other HDR parameters could be chosen to improve low-light sensitivity but increase SNRH dips and decrease SNRH for bright objects as shown in Fig. 6. In the latter example, the non-linear DR [8] is nearly 140 dB.

VII. Jot Consideration And Discussion

Nearly all jot devices considered by our group will work equally well with single-bit or multi-bit QIS architectures. The pump-gate jot [10], for example, has a full-well capacity of over one hundred electrons. Even for high conversion gain of 1mV/e-, $n=6$ corresponds to a signal swing of under 100mV and should not overload most readout signal chains.

SPAD devices, on the other hand, due to their effective high internal gain, don't seem to be well suited for multi-bit applications, despite their fine operation as large jots in single-bit QIS operation [11].

It is also important to note that the multi-bit approach might also be useful for scientific imaging applications, where non-linearity should be minimized, and where photon counting in high resolution is desired. In such applications, the multi-bit jot need not be sub-micron in pitch since high flux capacity may not be needed, which also suggests high frame rate is not required. Or is the multi-bit jot now just an ordinary pixel with high conversion gain? It is in this limit that the boundary between multi-bit QIS and high-conversion gain (photoelectron-counting) CMOS image sensor nomenclature becomes unclear. But aside from what to call it, such a multi-bit QIS device is sure to be useful, and will be demonstrated within a few years by some group.

Acknowledgments

The author gratefully acknowledges the support of Rambus, especially L. Stark, M. Ching, J. Endsley, and M. Guidash. Collaboration with XFAB is also appreciated. Finally, I would like to thank my research group at Dartmouth for their contributions and discussions.

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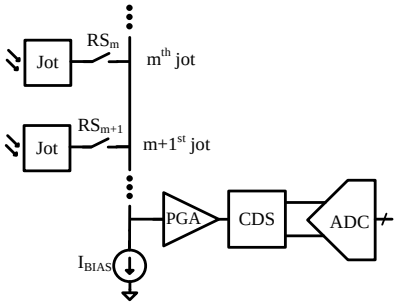

Fig. 1. Simplified readout circuit schematic for a single column of jots in a multi-bit QIS. In fact, it looks the same as for conventional CMOS image sensors except for the bit-depth of the ADC.

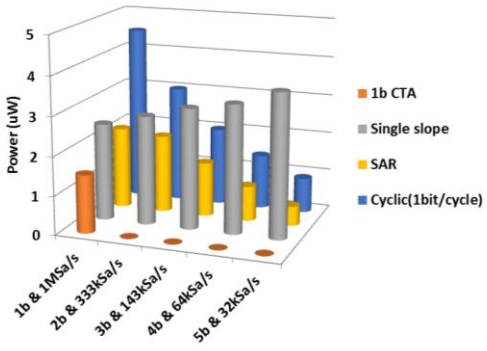

Fig. 2 shows power dissipation of single-bit and multibit QIS ADCs operating at different resolutions, and at different speeds for constant flux capacity. (From simulation of a chip in fab, S.Masoodian, D. Starkey, A. Rao, S. Chen, K. Odame and E.R. Fossum)

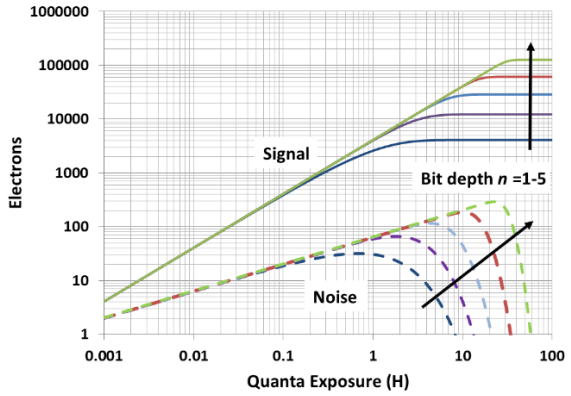

Fig. 3. Log signal and noise as a function of log exposure for multi-bit QIS jots with varying bit depth. The signal is the sum over 4096 jots (e.g. 16x16x16). Saturation signal is 4096·(2^n - 1).

Fig. 6 (right) Alternate HDR mode that improves low-light sensitivity and expense of reduced SNRH at higher light levels. Note 10% of max signal change occurs over last 40 dB of DR. First 13 fields duty cycle is unity, next field duty cycle is 1/5, next field is 1/25, and last is 1/125. The contribution of each set of fields is also shown.

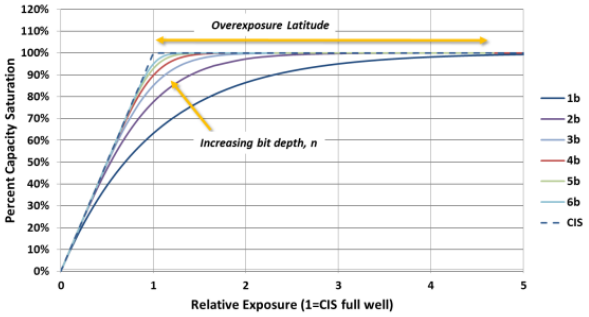

Fig. 4. Non-linearity and saturation characteristics of single-bit and multi-bit QIS for $1 \le n \le 6$ bits. For the QIS, the capacity of the full well is given by $FW = 2^n - 1$. The relative exposure is the quanta exposure H (in photoelectrons) divided by the full well, and the percent saturation is calculated from the expected number of photoelectrons in the photosite. Generally for the QIS, a "cubicle" in x,y, and t might be summed.

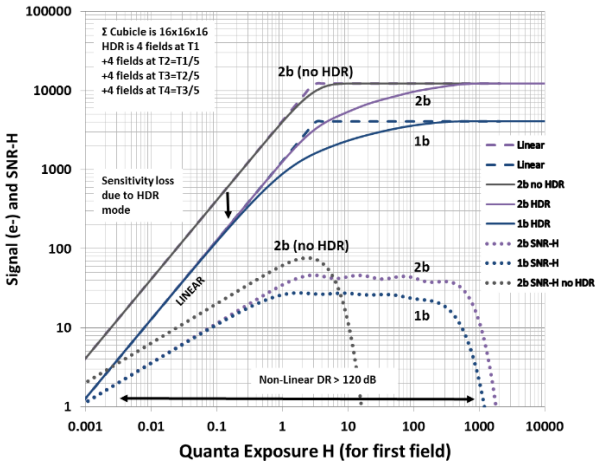

Fig. 5. Comparison of an HDR mode for 1b and 2b QIS. Cubicle is 16x16x16 fields, with 4 different shutter duty cycles. First 4 fields duty cycle is unity, next is 1/5, next is 1/25, and last group of 4 fields is 1/125. Signal is sum of cubicle data.