A 256 x 256 SPAD array with in-pixel Time to Amplitude Conversion for Fluorescence Lifetime Imaging Microscopy

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***Abstract*—A high resolution Time Correlated Single Photon Counting (TCSPC) image sensor based on sample and hold Time to Amplitude Converter (TAC)pixels and a global ramp voltage is presented. The 256×256 array achieves an $8\,\mu\mathrm{m}$ Pixel Pitch (PP), $19.63\,\%$ Fill Factor (FF), output voltage range ($0.7\,\mathrm{V}$) and time jitter of $368\,\mathrm{ps}$ at $10\,\mathrm{fps}$ employing an off-chip 14-bit differential Analogue to Digital Converter (ADC). A column-parallel flash ADCis also implemented, allowing coarse 3-bin TCSPC histogramming at $4\,\mathrm{kfps}$ for video rate fluorescence lifetime imaging.**

***Index Terms*—SPAD, Single Photon Avalanche Diode, TAC, Time to Amplitude Converter, TCSPC, Time Correlated Single Photon Counting, FLIM, Fluorescence Lifetime Imaging Microscopy.**

I. Introduction

Fluorescence Lifetime Imaging Microscopy (FLIM) provides absolute measurements of the environment and interaction of specific probes in living cells. Time Correlated Single Photon Counting (TCSPC) [1] is the preferred approach for FLIM due to its high photon efficiency as well as clearly defined Poissonian statistics and easy visualization of fluorescence decays [1]. TCSPC is however generally implemented in a laser scanning system using a single instrumentation channel which severely limits image acquisition rates. In recent years, Single Photon Avalanche Diodes (SPADs) sensors offer solid-state, multichannel implementations of TCSPC hardware [1]. Two different approaches are employed to obtain the time of arrival of each photon, Time to Digital Converters (TDCs) and Time to Amplitude Converters (TACs). Arrays of a few thousand SPAD-based TCSPC pixels have been reported at relatively low Fill Factor (FF) and large Pixel Pitch (PP) [2]–[7]. Improvements in these parameters have been obtained through simple analogue SPAD pixels, primarily through less photon efficient, time-gated approaches [7]. We present the first high resolution TCSPC image sensor based on sample and hold TAC pixels and a global ramp voltage [7]. The 256×256 array achieves an $8\,\mu\mathrm{m}$ PP, $19.63\,\%$ FF, output voltage range ($0.7\,\mathrm{V}$) and a time jitter of $368\,\mathrm{ps}$. An analogue readout and an off-chip 14-bit differential ADC allows per-pixel TCSPC histograms to be constructed at 10 photons/pixel/s. To allow a trade-off between lifetime accuracy and image acquisition rate, a fast column parallel ADC is also implemented, allowing coarse, 3-bin TCSPC histograms to be accumulated at $4\,\mathrm{k}$ photons/pixel/s.

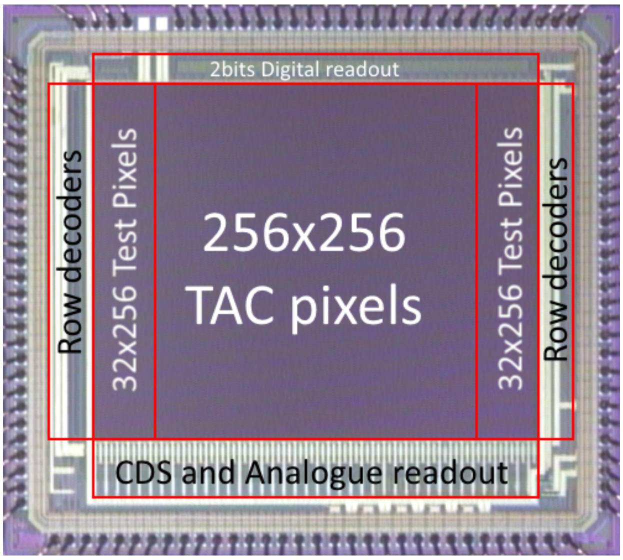

Figure 1. Micrograph of TCSPC Image Sensor.

II. Design

A micrograph of the TCSPC image sensor is shown in Fig. 1. It measures $3.5\,\mathrm{mm} \times 3.1\,\mathrm{mm}$ and is implemented in STMicroelectronics $130\,\mathrm{nm}$ CMOS image sensor process (Fig. 1). The pixels have been realised using the shared-well layout style in [8] to improve the pitch and fill-factor of the TAC pixel circuit reported in [7]. Fig. 2 shows the pixel circuit diagram. M2 and M3 transistors perform the time gate needed to filter Dark Count Rate (DCR). M4 and M5 create an NMOS only dynamic memory. The linear conversion range of this pixel has also been increased to around $700\,\mathrm{mV}$ by including a metal-oxide-metal (MOM) pump capacitor CM and a Boost signal. This represents an improvement of around $600\,\mathrm{mV}$ compared to our previous design [7]. The voltage on the Memory node is pumped up to above $3.5\,\mathrm{V}$ allowing a maximum $2.5\,\mathrm{V}$ sine wave or ramp signal to be sampled by M6 onto a hold MOS capacitor MC (Fig. 2). Transistors M7 and M8 constitute a conventional source follower and read transistor onto a shared vertical column line. Pixel column outputs are read-out through a differential double sampling analogue readout chain into an off-chip 14-bit, $20\,\mathrm{MS/s}$ Analogue to Digital Converter (ADC). A

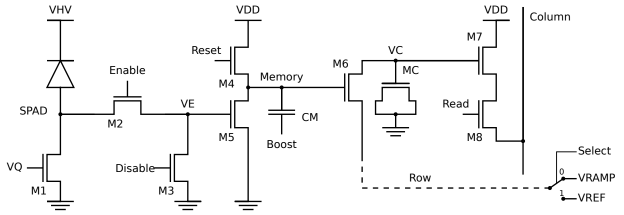

Figure 2. Time to analogue pixel circuit diagram.

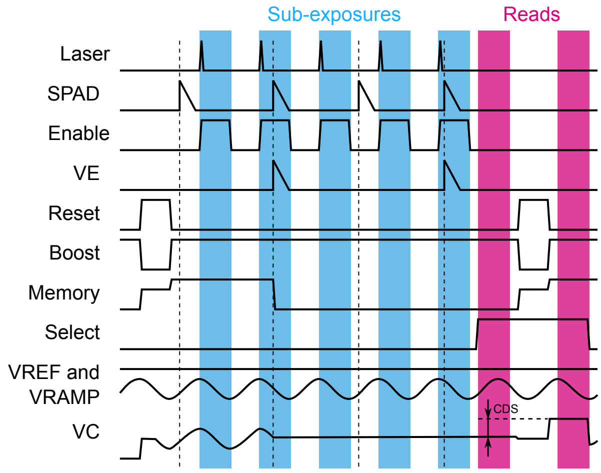

Figure 3. Time to analogue pixel timing diagram.

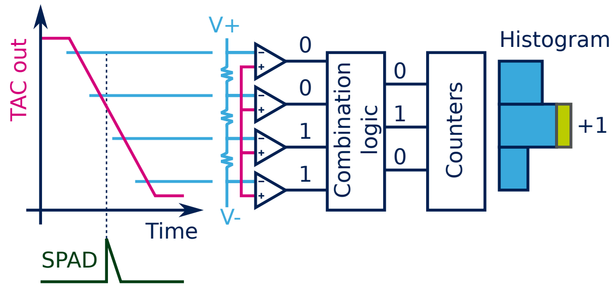

Figure 4. Column-parallel flash ADC digital readout.

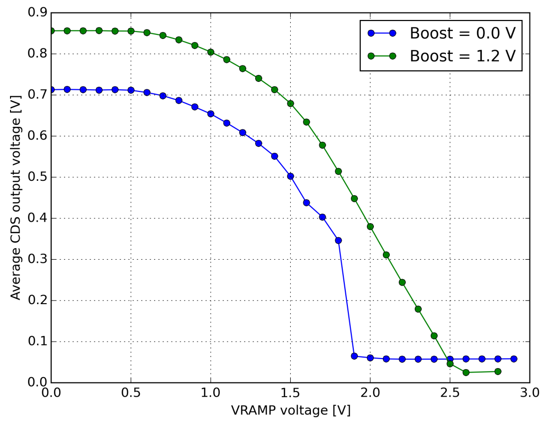

Figure 5. Pixel output range measurement with and without boost voltage.

differential sampling technique is employed during readout of VC to cancel pixel source follower (M7) Vt offsets by resetting the pixels after readout and switching the row voltage to a reference VREF.

At the top of the pixel array a 2 bit column-parallel Flash ADC was designed (Fig. 4). This allows a trade-off between the slow but precise analogue readout with a fast but coarse operating mode of the sensor allowing video rate fluorescence lifetime imaging. Fig. 4 shows the overall concept of a histogramming time to analogue converter obviating the read-modify-write sequence of conventional TCSPC hardware implemented in the analogue domain [8]. The technique is only partially implemented on chip here due to limitations on silicon area. Each column comprises 4 comparators sampling 4 globally distributed voltage references generated by a single resistive ladder. The thermometer code output of the comparators can be decoded by combinational logic (series of XORs) to increment one of a bank of ripple counters representing the TCSPC histogram. A pixel voltage lying outside the range set by the reference voltages V_+ and V_- representing the no-photon case can be easily discarded. In our specific implementation the comparator output bits are serialised and sent off-chip to an FPGA at $40\,\mathrm{MHz}$ over a 16-bit parallel I/O bus.

An additional feature of this scheme is that the two reference voltages are fully adjustable via off-chip DACs to allow zooming in to a time region of interest. This allows the TCSPC time bin range to be matched to the typical average lifetime range in a given image. Although the digital readout does not at present implement correlated double sampling, this technique would be readily applicable towards precise time-zooming once comparator and pixel source follower offsets are cancelled.

At the bottom of the sensor a single channel differential analogue readout is designed capable of Correlated Double Sampling (CDS). The output is converted by an external $14\,\mathrm{bit}$ ADC.

III. Results

A $1\,\mathrm{V}$ $10\,\mathrm{MHz}$ sine-wave input on VRAMP (Agilent 33220A and LeCroy WaveStation 3082) was used to characterise the array. VRAMP is synchronised to a pulsed laser (Hamamatsu PLP-10-044) and an Opal Kelly XEM6310-LX150 FPGA card. Fig. 5 shows the $600\,\mathrm{mV}$ improvement in DC output range, with and without, the Boost voltage [7]. A second experiment was performed in order to characterise the sampling performance and impulse response function (IRF) of the sensor. A laser was directed at the sensor with a lens spreading the laser beam over the whole array sampling a $10\,\mathrm{MHz}$ sine wave in each pixel. A single frame of pixel analogue time-stamps was then readout through the analogue readout and displayed as an image (Fig. 6). A histogram of the time stamps in this image is shown in Fig. 7 for a $20\,\mathrm{ns}$ ns laser pulse delay with respect to sine wave minimum. The histogram shows two clear distributions showing (1) no photon capture at 0V and (2) photon capture from the laser pulse at $0.3\,\mathrm{V}$. The IRF jitter is due to pixel leakage currents, residual offsets and noise from the readout and signal generator. The laser pulse delay was then swept using a delay generator (SRS DG645) through the maximum of the sine-wave to its minimum to characterise the time

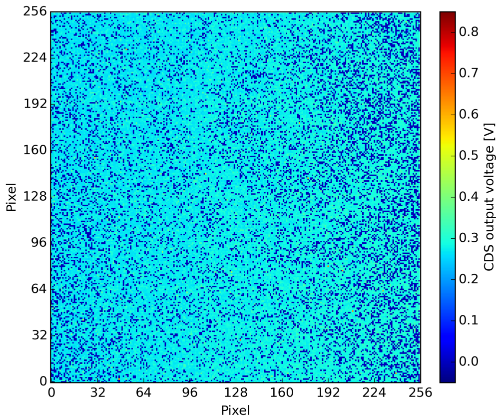

Figure 6. Frame of analogue time stamps from single cycle of 10 MHz pulsed laser.

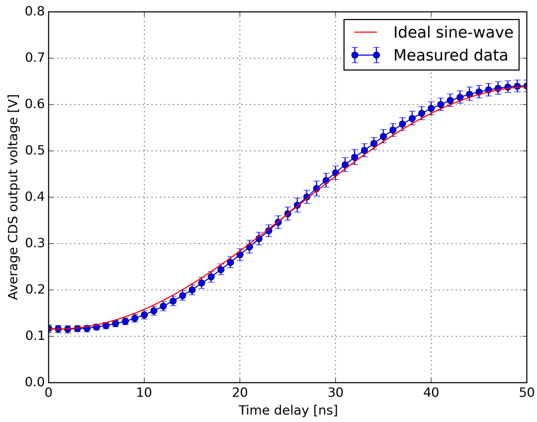

Figure 8. Time to analogue transfer function of imager for sinusoidal VRAMP.

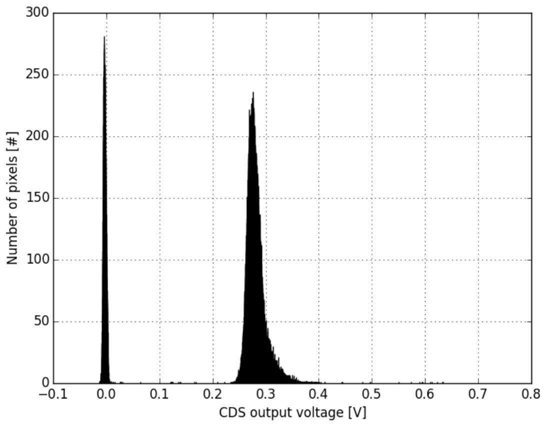

Figure 7. Histogram of the pixel timestamps in the image of Fig. 6.

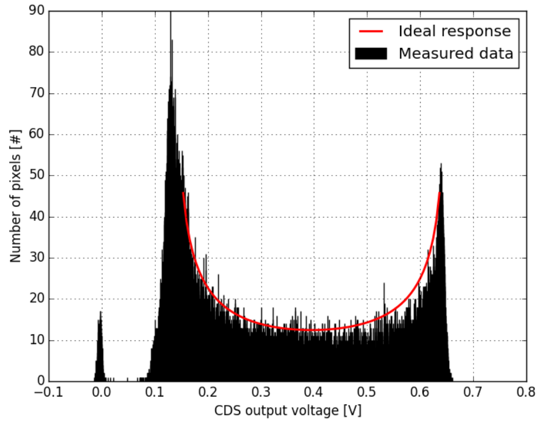

Figure 9. Code density plot for imager using sinusoidal VRAMP.

response, linearity and the noise contribution. Fig. 8 shows the peak position obtained by stepping the laser pulse in 1 ns intervals showing an excellent match to the ideal sine-wave.

Fig. 9 shows the image histogram due to uncorrelated light from a blue LED showing the expected "cusp-shaped" probability distribution expected as the code-density plot of a sine-wave. The low dark rate of the SPADs (median 50 Hz at 2 V excess bias) show very few dark count related events. A clear separation of the 'no photon' case from the signal range is observed.

Fig. 10 shows a CCD fluorescence intensity image of Culshaw root Xylem cells measuring around 120 µm diameter obtained after 1 s exposure with a 20 MHz, 483 nm pulsed laser. Fig.11 shows a coarse fluorescence lifetime image taken using 50 ms total exposure using the digital readout. The image is composed of 3-bin histograms per pixel formed by accumulating 5000 x 10 µs exposure frames generating around 100 photons/pixel. At a maximum frame rate of 4 kfps, the image would be acquired in 1.25 s. With a brighter sample, a FLIM video frame rate approaching 10 fps is attainable with the same number of photons/pixel allowing live cell behaviour to be studied. Two lifetimes of 1 ns and 5 ns were measured in the image by application of the Megaframe camera from [3] with 50 ps time resolution. The 1 ns lifetime is present in the cell boundaries while the 5 ns is present in the interior and periphery of the cells. The fluorescence lifetime is estimated using the rapid lifetime determination (RLD) technique between bin 1 and bin 2 of the flash ADC output [9]. A threshold of 1.5 ns is then applied, showing clearly two lifetime populations consistent with the values obtained with the Megaframe camera [3]. The noisy pixels and no photon cases have been rendered in black. The image shows column vertical and pixel fixed pattern noise which can be improved by application of noise cancelling circuit techniques. The horizontal artefacts are due to unequal distribution of the ramp voltage through a balanced metal tree.

Table I shows a comparison between the specifications and performance of multi-channel time resolved converter arrays suited to TCSPC fluorescence imaging. The imager achieves the highest image resolution, smallest pixel pitch and highest fill-factor of SPAD-based pixel arrays. Although the time resolution is not the lowest, the imager offers a practical tradeoff of frame rate and imaging resolution for typical FLIM time constant ranges.

Table I
TAC AND TDC COMPARISON

Type	This work TAC pixel	[7] TAC pixel	[5] TAC pixel	[6] TAC IC	[2] TDC pixel	[3] TDC pixel	[4] TDC pixel
Technology	130 nm CMOS CIS	130 nm CMOS CIS	130 nm CMOS	350 nm SiGe BiCMOS	350 nm CMOS	130 nm CMOS	130 nm CMOS
Dyn. Range	50 ns[1]	80 ns[1]	20 ns[1]	100 ns[1]	320 ns	53 ns	64 ns
Time Res. [1LSB]	6.66 ps[2]	5.1 ps[2]	160 ps	30-110 ps	312 ps	52 ps	62.5 ps
Time Jitter	368 ps[2] (RMS)	5.1 ns[2] (RMS)	$<$ 600 ps[3] (FWHM)	18 ps[3] (FWHM)	254 ps[2] (RMS)	0.6 LSB[3] (mean)	200 ps[3]
Differential Non-Linearity (DNL)	TBD	$<$ 3.5 LSB	0.4 LSB	0.2 % LSB	2 %	0.4 LSB	$<$ 4 LSB
Pitch X	8 µm	9.8 µm	650 µm	50 µm	150 µm	50 µm	48 µm
Pitch Y	8 µm	9.8 µm	440 µm	50 µm	150 µm	50 µm	48 µm
SPAD diameter	2.4 µm $\times$ 5.7 µm	2 µm	6.6 µm	N/A	30 µm	6.6 µm	5 µm
FF	19.63 %	3.27 %	1 %	N/A	3.14 %	1 %	0.77 %
Number of pixels	65536	9	1024	16	1024	1024	4096

[1] Adjustable
[2] Optical stimulus
[3] Electrical stimulus

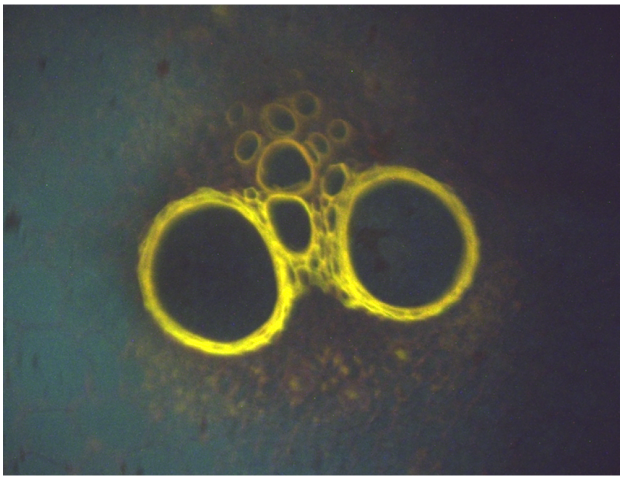

Figure 10. Microscope CCD imager of Cushaw Root Xylem cells taken with a pco.pixelfly usb CCD camera.

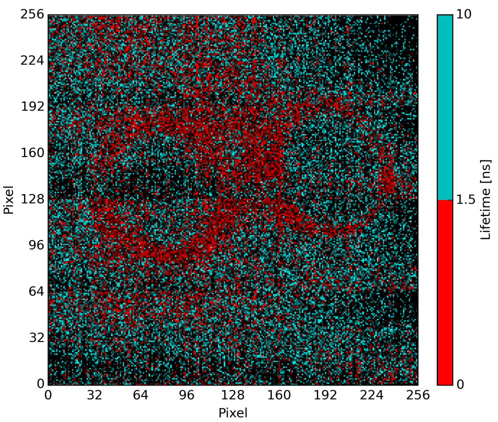

Figure 11. Thresholded lifetime image of Cushaw Root Xylem cells.

IV. CONCLUSIONS

TCSPC imaging is implemented in a wide-field, high resolution camera format achieving high fill-factor by the application of compact SPAD pixel layout and analogue circuit techniques. Low temporal resolution video-rate TCSPC FLIM is enabled by a novel flash-ADC column parallel readout whilst an slower analogue readout allows high temporal resolution, low frame rate but precise lifetime determination.

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