CMOS Image Sensor for Multi-Aperture Optics

A 15x9 Array sensor for low z-height 720p camera modules with depth information

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***Abstract*— This paper presents a 15x9=135 array sensor for wafer level multi-aperture micro optics intended for low z-height (<2mm) camera modules. The sensor acquires 1440x864 pixel for a 720p 30fps image and integrates image acquisition circuitry and digital reconstruction algorithms in-between the image arrays. The presented image sensor allows the computation of a depth map of the scene.**

Keywords—Mulit-aperture, computational imaging, CMOS image sensor

I. Introduction

Multi-Aperture systems see growing interest due to their ability to circumvent some of the current challenges in mobile device imaging. They enable lower z-height cameras with depth sensing capabilities. Due to the wafer level production of the optical elements these systems can be built at low cost. As currently pixels don't shrink as fast as the resolution increases conventional single aperture optics can't shrink the z-height due to geometrical optical considerations.

Apart from this, multi-aperture optics can enable additional features as depth information and refocus [1]. Multi-aperture optics project multiple images on the sensor. These images can't be adjacent due to technology constrains of the production of the lenses. Therefore, there are gaps between these images, which cannot be used for light detection. The silicon area between the arrays is used for analog column circuits, the analog to digital converter, the digital timing circuit and the reconstruction algorithm. The lenses form partly overlapping projections of the scene, which is different from the super-resolution used in [1] and the described 16 focal plane sensor [2]. The reconstruction algorithms for the proposed method are less complex and therefore lower power consumption can be achieved.

II. Sensor Architecture

The implementation aims at a multi-aperture sensor with low area and the ability of computation between the individual image areas. To reduce overall area the analog to digital conversion, row selection, digital processing and output formatting is implemented between the image areas. The sensor consists of 15x9 image areas, each composed of 96x96 pinned pixels of 2.2µm in a 4-shared configuration as depicted in Fig. 1.

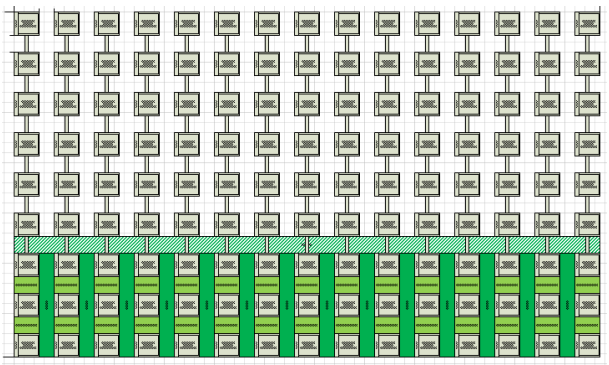

Fig. 1. Image area of sensor

The image areas are covered with a uniform RGB color filter, so there is no color crosstalk between adjacent pixels. A classical Bayer configuration is used as can be seen in Fig. 5. Each image area has a decoder for the selection and control of the necessary row signals. The column sample and hold (S&H) and comparator are in the lower 2 row-channels, the memory for the single slope converter is placed in the column-channel as shown in Fig. 2.

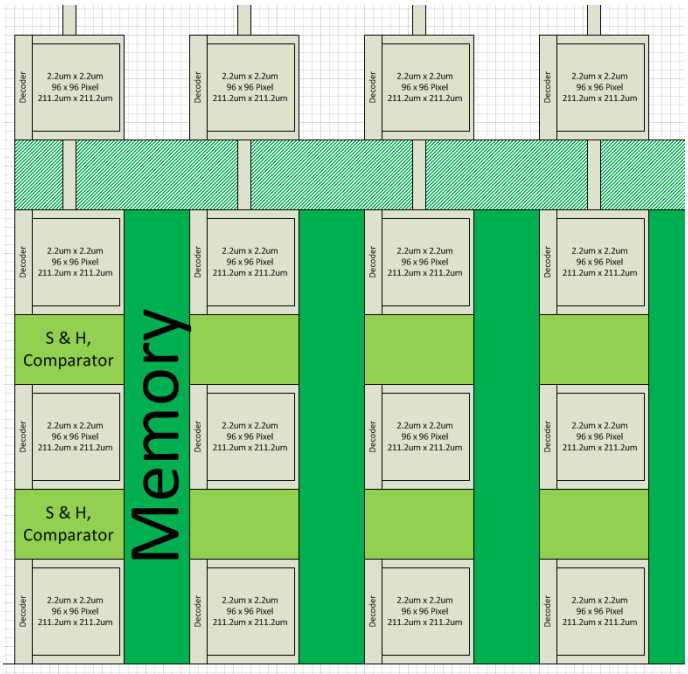

Fig. 2. Detailed view of lower left part of the sensor: Distribution of sample and hold and memory

The column-level, single-slope converter compares the column voltage with a globally generated ramp signal. It has a built-in correlated dark sampling (CDS) as depicted in Fig. 3.

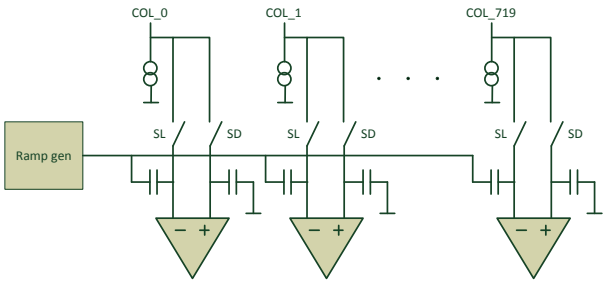

Fig. 3. Column correlated dark sampling ciruit

The correlated dark sampling is done by storing the column voltage on a capacitor after the pixel reset was done (dark signal) by setting the signal SD (sample dark) as can be seen in Fig. 4. Then the transfer of the charge corresponding to the information about the illumination in the pixel is done. The column voltage containing this information is sampled on a second capacitor by the signal SL (sample light). The sampling is done with the reference voltage set to the code 32 of the digital to analog converter. So with no signal (dark picture) the

code 32 (± noise) will be digitized in the following analog to digital conversion. This enables smoother pictures compared to using the default value of 0 as the noise would be clipped in half of the digitized signals.

After the sampling is done the global ramp shifts the voltage at the input of the comparator. The comparator flips as the voltage crosses the value of the "dark" sampled signal. The digitized value is therefore the difference between the two signals (dark and light) as desired. The corresponding digital code is stored in a column-level digital memory of 10bit.

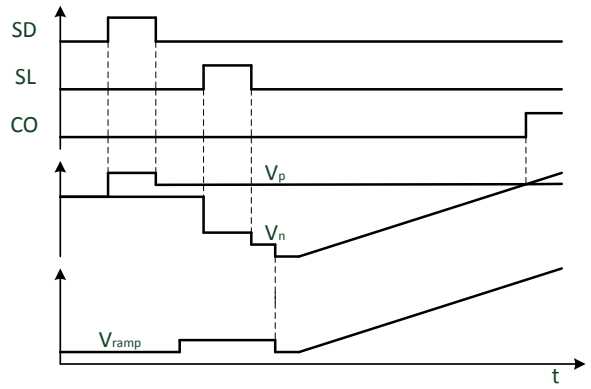

Fig. 4. Timing of column correlated dark sampling ciruit

The digital circuitry in-between the image arrays controls the sensor and integrates image processing algorithms as the image reconstruction and black level correction. The sensor is operated on a single clock and can be configured via an SPI. The sensor output is a 10bit/pixel serial data stream, which can be directly connected to the video interface of an OMAP-processor.

III. Sensor Implementation

The sensor is implemented in a 4 metal 180nm CIS process. Key challenge was the efficient implementation of the analog processing and the digital algorithms within the image area. An algorithm with electronic focus for the reconstruction of the segmented picture with different depths is built into the sensor. The implementation is done with little memory usage and is therefore very area efficient. Several other algorithms are in the image processing pipeline (ex. black level correction). As the goal of this sensor is not an integration of a complete image processing chain, some algorithms (ex. demosaicing) are not yet included but can be done in a later extension as there is still enough area for digital algorithms.

IV. Results

The sensor was fabricated and assembled with the micro optical array (Fig. 5 and Fig. 6).

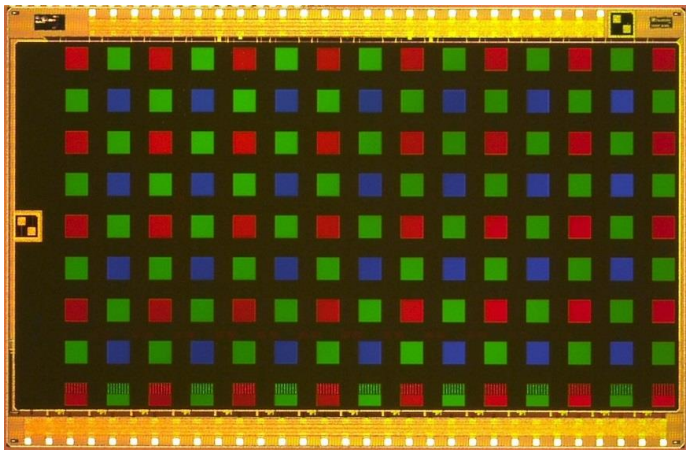

Fig. 5. Picture of the sensor

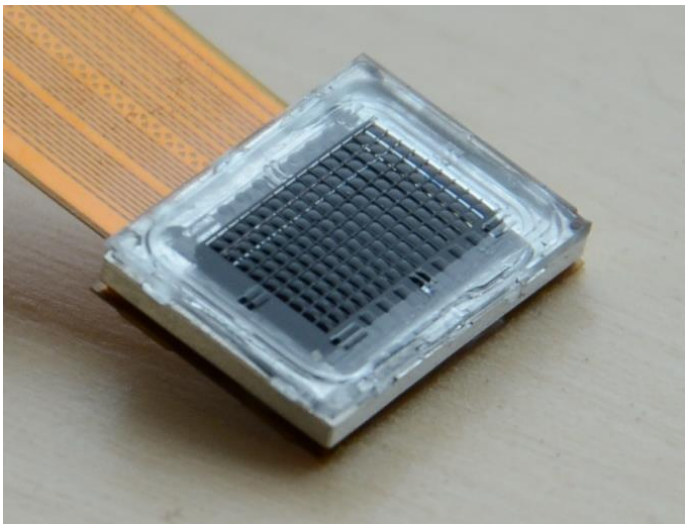

Fig. 6. Picture of the assembled module

First images could be successfully taken from the sensor. It could be proved that the algorithms needed for picture reconstruction can be implemented in the silicon area between the pixels even if some of the algorithms need improvements for better picture quality in the next stage.

Key parameters are listed in Table 1.

TABLE I. KEY PARAMETERS

Process	180nm CIS, 4 metal, MIM
Pixel	4shared 2.2µm
Image Area	15x9 image areas of each 96x96pixel =1440x864
ADC	10bit single slope converter with column-wise correlated dark sampling; configurable gain setting
Die size	6400x4250um
Framerate	30fps
Processing	Exposure control, image reconstruction, depth focus, black level correction, quadrupel correction,
Interface	Single clock input, SPI configuration, 10bit serial 36MPix/s output; output format compatible with OMAP video interface

V. Summary

We demonstrate an array sensor tailored to a multi-aperture optical system for a very low z-height 720p camera module with 3D capabilities. The area between the optical sensitive arrays is used for the analog column circuitry, the digitization and digital processing chain including an image reconstruction algorithm.

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References

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