# Dark Current Limiting Mechanisms in CMOS Image Sensors

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Dark current density in image sensors has dropped by 4000x since the 1970's both due to robust designs and process improvements.[1,2] The improvements have addressed the Shockley-Read-Hall (SRH) defects related to unpassivated interfaces and metallic contamination. The result is that the temperature dependence for the preponderance of pixels within an image sensor has changed at 60C from nominally 11 C/doubling to 6 C/doubling. This indicates that mid-energy band traps are no longer the dominant source of the pixel background dark current. There is a consensus that the dark current will continue to be reduced due to improvements as the technology scales, but at present there is no established root cause for the dominant dark current with this temperature dependence to guide the effort.

This presentation will address the unique aspects of the pixel design and device physics that could be relevant to defining a root cause for the dark current.

These include the implications of the long minority carrier lifetimes and the extremely low density of minority carriers when viewed with regard to the pixel dimension. In the CMOS process technology developed for image sensor manufacture the minority carrier density in the undepleted region is << 1e-/pixel providing limiting intrinsic diffusion dark current. The dark current collected in a video pixel also can be <1e-/pixel/frame. Since the dark current is physical electrons or holes, the dark current has aspects of being quantized in both in space and in time. As photon counting becomes a reality, the nature of dark current will shift from being a shot-noise limiting background into being a “false positive” signal. TCAD simulation needs to comprehend the quantized nature of the charge.

The presentation will provide a survey of possible mechanisms and origins (Figure 1). Dark current reduction has traditionally been a process of identifying the root cause of what is the dominant generation method of the moment. This has successfully been used to reduce metallic contamination in the process through equipment improvements, improved cleanliness and through gettering. It has eliminated the generation by passivation of the interfaces by process and robust design. This has dramatically lowered the dark current rate and changed the nature of it as shown by the shift in temperature dependence. There is a need to identify the present root mechanism to guide further reduction so as to continue the industry trend of 10x reduction per generation. The image sensor becomes the prime diagnostic tool, providing insight into the silicon and the device through varying operation. It provides precise noise and signal measurements as the electrical profile in the pixel is modulated (Figures 2 and 3). For instance, varying the operating voltage and the temperature allows the mapping of dark current sources within the bandgap (Figure 4). There is also the possibility of comparing pixel designs, for instance frontside-illuminated pixels versus backside-illuminated pixels to understand the impact of the underlying silicon.

With the traditional mid-bandgap SRH no longer dominant, there is a need to evaluate new candidate mechanisms, particularly ones with activation energy close to the band gap. A possibility is SRH for the case of traps near the band edge, including the doping states themselves. A second is the lightly-doped undepleted silicon regions, which with their very long lifetimes and their

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proximity of depleted photodiode volumes act the same as depleted regions in that the minority charge generated quickly disperses without recombination. A third is that charge generated by interfaces outside of the depletion region or at the contacts diffuse through the undepleted regions.

TCAD simulations, using tools such as Synopsys®'s Sentaurus [3], show that shallow traps, dopants, and frontside or backside interface generation can provide the temperature dependence seen in a representative commercial product (Figure 5) [4].

In addition, the presentation will speculate on the intrinsic dark current for a pixel in defect-free silicon. This is important in that it provides the limit of what is possible by foundry efforts to improve process which seem to be continuing to follow the historical approach based on either SRH trap-assisted or impact ionization [5].

The limiting could be an Auger generation, often called "impact ionization", set by a mechanism related to the band dynamics of silicon being defect-free. At the limit and with good device design, this would not require high field acceleration, but would be due to the thermal energy of carriers hence the more accurate designation as "Auger generation". This is a three particle process with an energetic particle that provides energy, an electron that is promoted across the indirect bandgap and a phonon that is needed to conserve momentum. In this scenario the important feature to impact the dark current would be the volume of the silicon providing a trade-off with quantum efficiency.

The other possibility is that the limit is SRH for traps near the band edge. In the defect-free limit, this would be the dark current due to SRH to dopant levels with highly doped regions having higher dark current. In this case design can have a major impact on this.

It appears that this limit could be only 10x to 100x lower than what is presently being manufactured.

In summary, there appears to be room for process improvements to continue the trend of reduced dark current. There is a need to continue this trend to complement the on-going reductions in read noise and to realize the potential of photon-counting image sensors. There is value in a fresh look to understand the physics of the pixel in regard to dark current generation and to develop a hypothesis for the present limiting mechanism and its relation to process-induced defects. It is important to understand the eventual limiting dark current when there are no significant defects and where further efforts to reduce dark current will need to shift to design based on the knowledge gained.

References:

[1] R.H. Dyck, M.D. Jack, "Low Light Level Performance of a Charge-Coupled Area Imaging Device", 1974 CCD Workshop, Edinburgh, UK

[2] M.Kobayashi, et al, "A Low Noise and High Sensitivity Image Sensor with Imaging and Phase-Difference Detection AF in All Pixels", 2015 IISW, Vaal, Netherlands
Canon Inc.

[3] https://www.synopsys.com/content/dam/synopsys/silicon/datasheets/sentaurus_ds.pdf

[4] H. Rhodes et al, "The Mass Production of Second Generation 65 nm BSI CMOS Image Sensors", 2011 IISW, Hokkaido, Japan

[5] D.K.Schroder, editor, **Semiconductor Material and Device Characterization**, 3rd Ed., John, Wiley & Sons, 2006

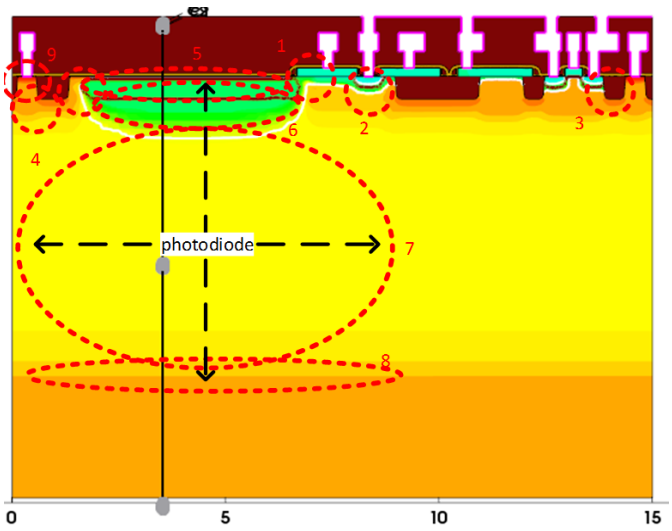



Figure 1. Dark current sites within pixel: [1] TX edge: diffusion from interface ($E_g$); lucky drift from interface ($E_g/2$); interface stress ($E_g$); [2] FD injection: blooming forward bias; [3] Other junction: forward bias or carrier injection; [4] STI interface: diffusion from interface ($E_g$); interface stress ($E_g$); [5] Pinning layer: diffusion from interface ($E_g$); interface stress ($E_g$); doping-based SRH ($E_g$); [6] Deep depletion: SRH from contamination ($E_g/2$); [7] Lightly doped region: diffusion from weak SRH ($E_g/2$ or $E_g$) ; [8] Back interface: diffusion from weak interface SRH ($E_g$); Contact diffusion current ($E_g$)

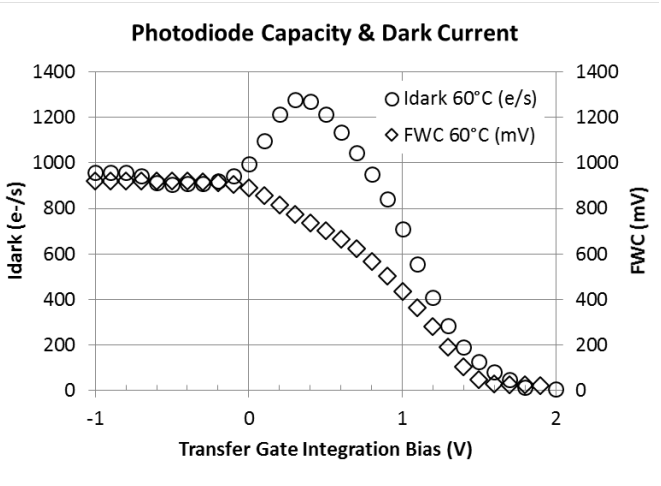



Figure 2. Full Well Capacity & Dark current behavior versus Transfer Gate Bias. The curves provide insight into dividing the operation into regions & classifying the dark current sources.

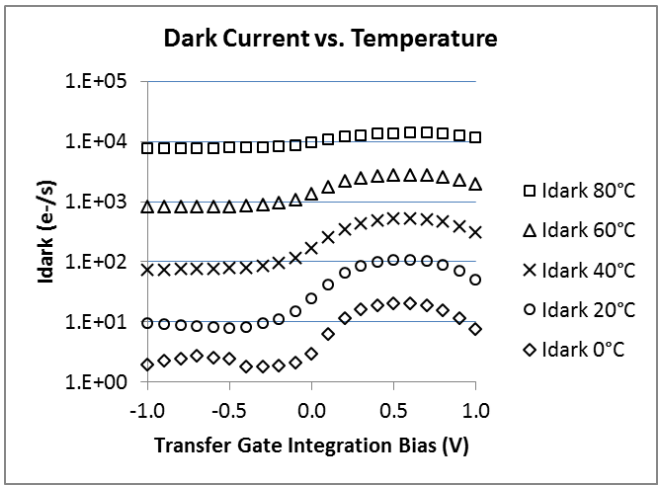



Figure 3. Dark current versus Transfer Gate Bias over Temperature. It shows the difference in temperature dependence between having $V_{LOTG}$ being biased negative or being biased positive during integration

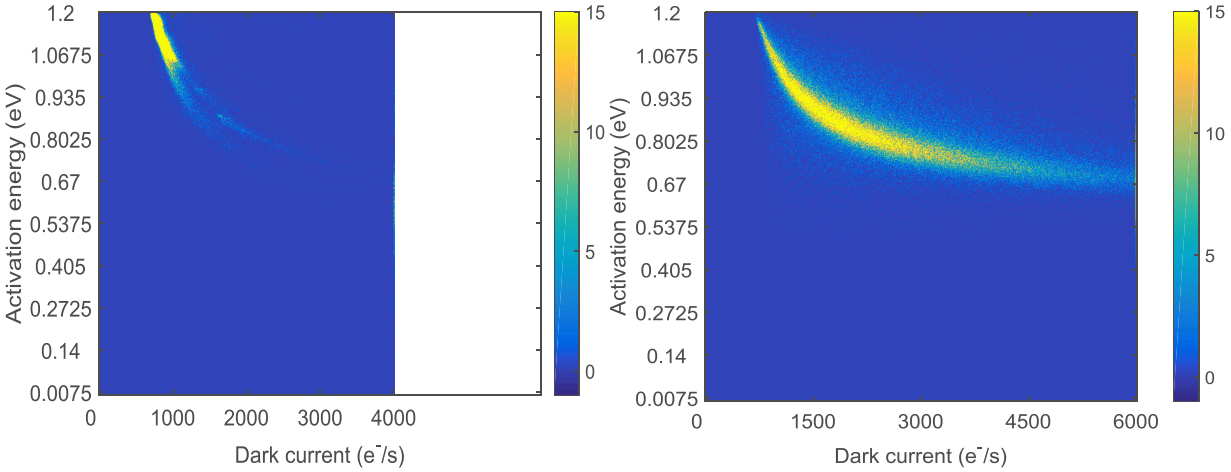
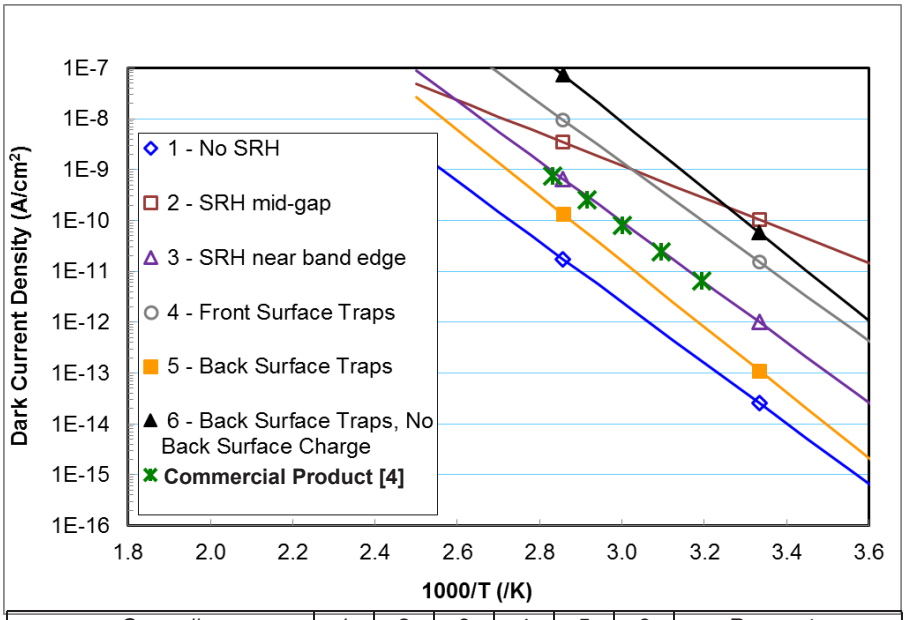



Figure 4. Dark Current Activation Energy vs. Generation Rate at 60C showing location of dark current generation sites in energy bandgap: [left] $V_{LOTG}$ =-0.8V; [right] $V_{LOTG}$ = +0.6V




| Curve # | 1 | 2 | 3 | 4 | 5 | 6 | Parameters |
|---|---|---|---|---|---|---|---|
| Ea (eV) | 1.18 | 0.64 | 1.18 | 1.16 | 1.28 | 1.29 | |
| Bulk SRH, mid-gap | | X | | | | | Et=0, tau=1e-3 s |
| Bulk SRH, near band edge | | | X | | | | Et=0.5, tau=4.6e-8 s |
| Front surface SRH, mid-gap | | | | X | | | Et=0, Nit=1e11 cm-2 |
| Back surface SRH, mid-gap | | | | | X | X | Et=0, Nit=1e11 cm-2 |
| Back surface fixed charge | X | X | X | X | X | | Qf=-1e12 cm-2 |

Figure 5. 3-d simulation of pixel dark current mechanisms. $E_t$ is the SRH trap energy relative to mid-gap. $E_a$ is the activation energy from the slope of the curve.