A highly linear CMOS image sensor with a digitally assisted linearity-calibration method

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Abstract

A highly linear CMOS image sensor designed in 0.18μm CMOS image sensor (CIS) technology is presented in this paper. A new type of pixel design is adopted to cancel off the nonlinearity of the source follower (SF) and hence enhance the linearity. Furthermore, a digitally assisted calibration method is proposed to improve the linearity of the image sensor. The measurement results show that the new type of pixel can achieve better linearity performance comparing with the typical 4T pixel. With the calibration, the linearity of all types of pixels have been improved.

Introduction

The linearity of a CIS is determined by its pixel design and readout circuitry. Usually, the readout circuit can achieve relatively excellent linearity with an elaborate circuit design. However, the variable gain of the source follower over the pixel's output range and the nonlinearity of the integration capacitor make the pixel's photoelectric conversion nonlinear [1].

The circuit of a typical 4T pixel together with bias circuits is shown in Fig. 1. The pixel circuit consists of a pinned photodiode associated with a transfer gate (M_1), a reset switch (M_2) which used to reset the photodiode, a source follower (M_3) that drives the loading readout circuit and a row select switch (M_4). The current source transistor (M_5), located on the column bus, is shared by multiple rows of pixels.

The gain of the SF is not a constant value due to the body effect, shown in Equation (1).

$$G_{SF} = \frac{g_{m,SF} \cdot R_S}{(g_{m,SF} + g_{mb,SF}) \cdot R_S + 1} = \left(1 + \frac{\gamma}{2 \cdot \sqrt{\varphi + V_{PIX}}} + \frac{1}{g_{m,SF} \cdot R_S}\right)^{-1} \quad (1)$$

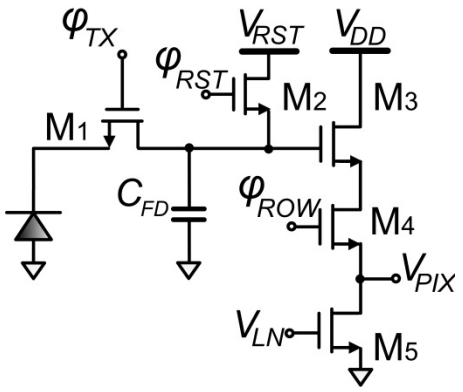

Fig. 1 Schematic of a 4T pixel.

In Equation (1), $g_{m,SF}$ and $g_{mb,SF}$ are the gate-drain and the bulk-drain transconductances of the SF transistor; R_S is the finite output resistance of the current source; γ represents the body effect; φ is the strong inversion surface potential. The gain of the SF changes with the output voltage of the pixel V_{PIX}, which degrades the linearity of the image sensor.

The integration capacitor of the floating diffusion region in the pixel contains different types of capacitances. Some capacitances are related to the gain of the SF and the output voltage of the pixel[1]. The readout circuitry brings an extra nonlinearity. These factors make the output of the image sensor nonlinear.

Image Sensor's Architecture

In this paper, a highly linear CMOS image sensor with a digitally assisted linearity-calibration method is proposed. The overall block diagram of the prototype image sensor is shown in Fig. 2. It comprises a pixel array, column readout circuits, row decoder/driver, column decoder, bias/reference generator and digital logic controls. The pixel array consists of 128×128 pixels

with a pitch of 10μm. The column-parallel analog chain contains a column amplifier which has a programmable gain from 1× to 8×, a 10-bit single-slope Analog-to-Digital Converter (ADC), and a SRAM array. After the signals are digitized by the ADC and stored in the SRAM, they are further processed by an off-chip FPGA. The ramp signal of the ADC V_{RAMP} is provided by an on-board 12-bit digital-to-analog converter (DAC).

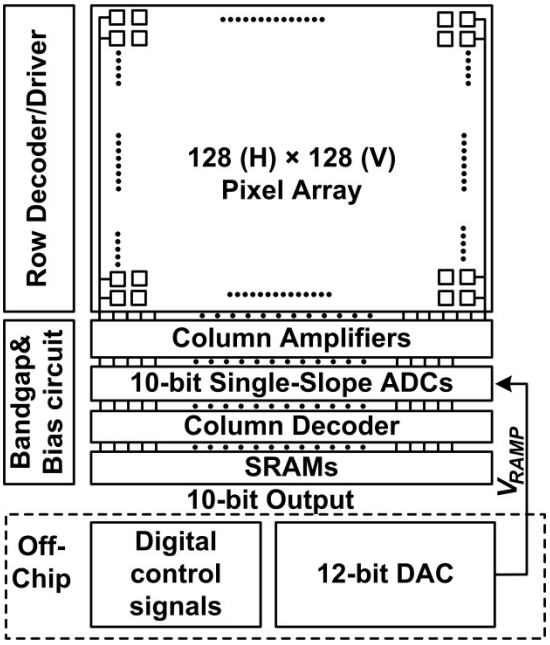

Fig. 2 The proposed CIS system diagram.

To reduce the nonlinear effects caused by the SF in the pixel, a single-stage operational amplifier is used instead as an analog buffer to drive the loading circuits. Fig. 3 shows the schematic and the timing diagram of a new type of pixel (Pixel V1). In our test device there are several other types of pixels available, including a traditional 4T one (Pixel V2), to compare the relative performance.

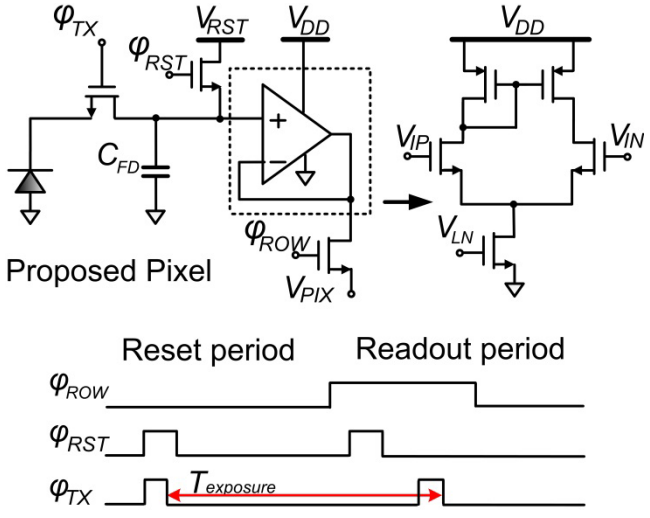

Fig. 3 The schematic and the timing diagram of Pixel V1.

Besides the optimization of the pixel design, this image sensor employs a calibration method to further improve the linearity of the image sensor, which is illustrated in Fig. 4.

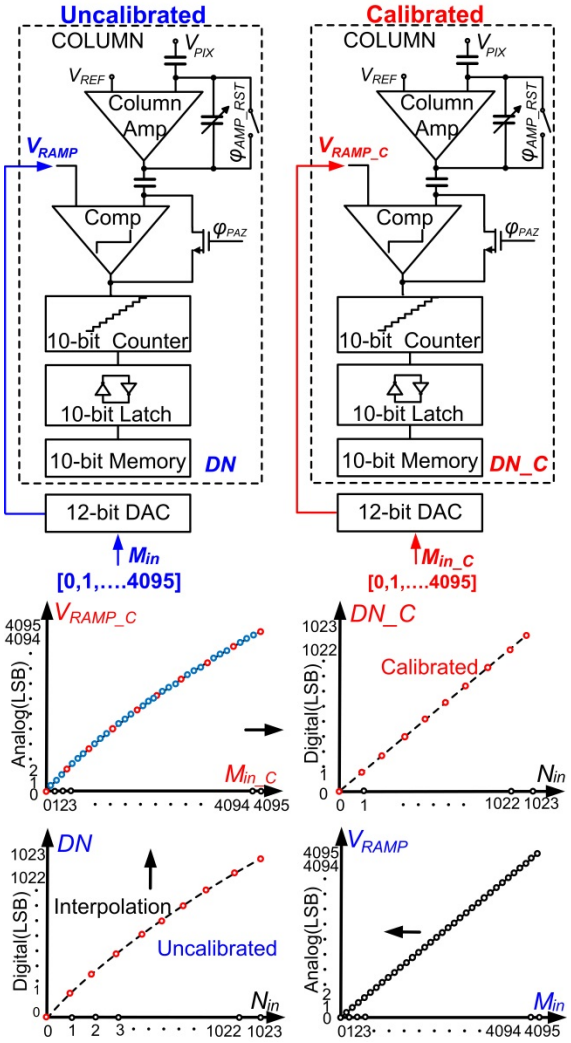

Fig. 4 The calibration method

To perform the linearity measurements, the amount of light coming to the sensor is changed by varying the exposure time under constant light conditions. Based on the nonlinear transfer function from the incremental injected photons to the pixel to the individual output digital number (*DN*) within an incremental exposure time, the nonlinearities of the circuit can be analyzed. This is done by copying the non-linear behaviour of the sensor into the ADC circuitry and to create a non-linear ramp for the ADC. In other words, the transfer function of the ADC is made non-linear to compensate for the non-linearity of the CIS. The whole process of calibration and compensation can run fully automatic.

During the calibration, the number of photons accumulated by the sensor is changed by increasing the exposure time from a unit $T_{exposure}$ to $1024\times T_{exposure}$ under

constant light intensity. N_{in} is the exposure sequence, which increases evenly from 0 to 1024. M_{in_C} is the corresponding digital output sequences after mapping and interpolation, while M_{in} is the interpolated sequences which increase from 0 to 4095. The mapping process removes the offset and the gain errors of the data collected from the SRAMs. Interpolation is needed for the 12bit DAC. The calibrated ramp signal V_{RAMP_C} contains the information of the nonlinearities of the pixel and of the readout circuit, which is employed to cancel out the latter nonlinearities.

Experimental Results

The proposed image sensor has been fabricated in a commercial 0.18μm CIS process technology. Fig. 5 shows the micrograph of the fabricated chip and the test camera system. The size of the chip is 2.6mm × 5mm.

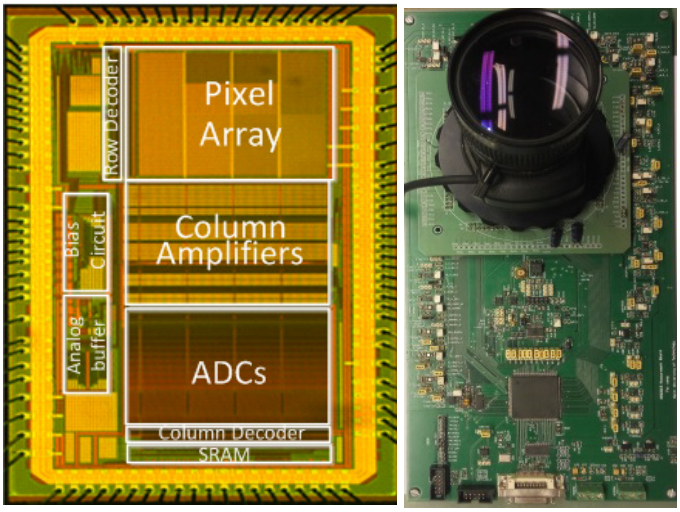

Fig. 5 Chip microphotograph and test camera system.

The pixel V1 achieves a better linearity, compared to the traditional 4T pixel V2. Fig. 6 shows the linearity results of the pixel V1 and V2. Both pixel types are using the same value of the transfer gate high voltage V_{TXH} and the reset voltage V_{RST}. The linearity of the pixel is related to V_{TXH}. In the test, we set the value of V_{RST} as 2.7V, and the value of V_{TXH} is variable from 2.5V to 3.3V.

In Fig. 6, the blue lines show the measurement results without calibration and the red lines represent those with calibration. A higher value of V_{TXH} results in a worse linearity of the CIS. However the calibration method improves the pixels' linearity effectively. When V_{TXH} equals 2.5V, the nonlinearity of pixel V1 is 0.26% while that of the typical 4T pixel V2 is 0.41%. With the help of the calibration, the nonlinearity of pixel V1 and V2 are optimized to 0.058% and 0.060%. When V_{TXH} equals 3.3V, the nonlinearity of the pixel V1 and V2 is 0.76% and 1.14%. After calibration, the nonlinearity can be improved to 0.11% and 0.12% respectively.

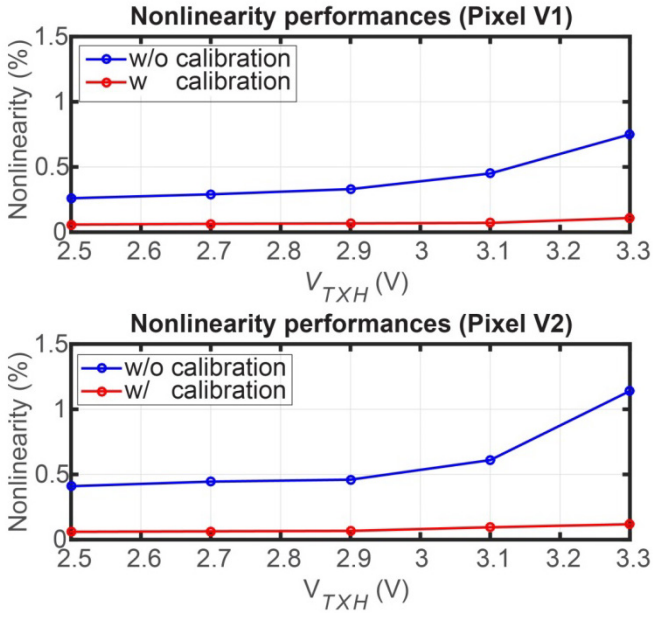

Fig. 6 Nonlinearity performances of pixel V1 and V2

Julien Michelot proposed that a higher value of V_{TXH} can bring charge spill back effect which will have an impact on the pixel performances[2]. As illustrated in Fig. 7, we plot the curve of digital output versus exposure time for the pixel V1 with different V_{TXH}. In the small signal region, the charge transfer tunnel is always in the depletion region. In the large signal region, electrons will spill back to the PPD after the charge transfer phase if the tunnel was in the inversion region, and a higher V_{TXH} makes the tunnel enter the inversion region earlier. This explains why a higher V_{TXH} deteriorates the linearity performance of the pixel. So the linearity with a lower V_{TXH} is better if image lag is not an issue [2].

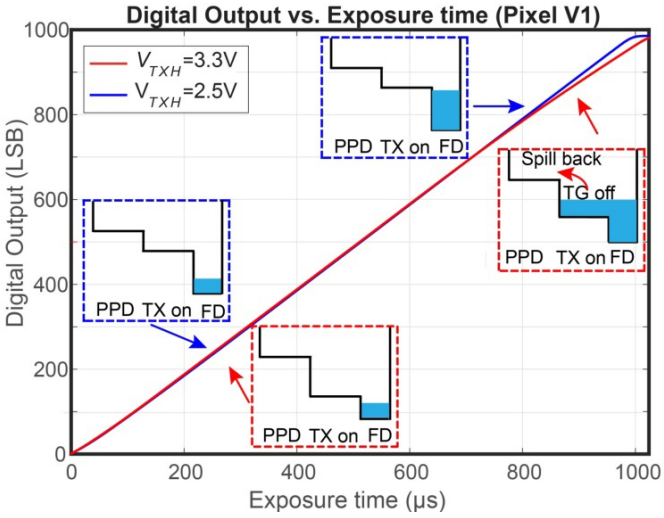

Fig. 7 Digital Output of the Pixel V1 vs. Exposure time.

According to the measurement, pixel V1 not only improves the linearity performance, but also realizes a near unit gain and hence increases the conversion gain of the pixel. The conversion gain of the pixel V1 is 56.8μV/e-, and that of the pixel V2 is 45.3μV/e-.

However, the new type pixel introduces more noise compared to the normal 4T pixel. Fig. 8 shows the input referred noise voltage for the proposed pixels with different amplifier gain under dark conditions. Pixel V1 has a higher noise than that of the 4T pixel V2. The high gain of the column amplifier efficiently suppresses the input referred random noise to 234μVrms and 189μVrms for pixel V1 and V2 at an analog gain of 18dB.

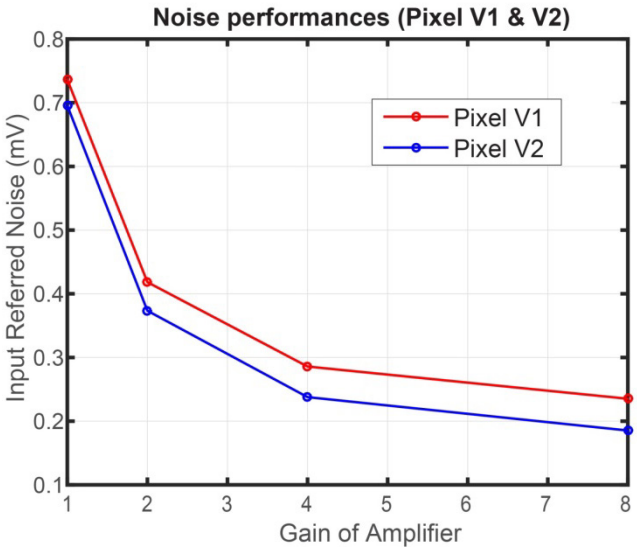

Fig. 8. Input referred noise vs. Column amplifier's gain.

An image taken by the prototype sensor with pixel V1 is shown in Fig. 9. The measurement were collected with the chip operating at 60 frames/s.

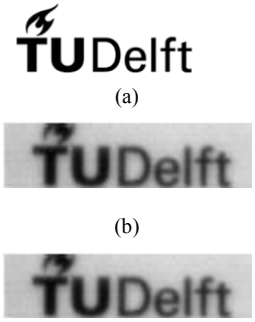

Fig. 9. (a) Sample picture (b) Captured picture (Pixel V1) without calibration (c) Captured picture (Pixel V1) with calibration.

Conclusion

In this paper, we propose a new type pixel design which has a better linearity performance. Furthermore, the image sensor achieves improved linearity performance with the assistance of the proposed calibration method. Table I shows a performance comparison among [3-4].

Table 1 Performance comparison

Process		This Work		[3] 2016	[4] 2015
		180nm		90nm	90nm/65nm
Number of	pixels	128×128		4624×2296	5246×3934
Pitch of	μm	10		5.86	1.43
Frame rate	fps	60		480	30
ADC Architecture		10bit SS		14bit SS	12bit SS
Conversion gain	μV/e-	Pixel V1	Pixel V2	30.3	76.6
		56.8	45.3		
Noise	e-rms	4.12 (Gain=18dB)	4.17 (Gain=18dB)	4.6 (Gain=12dB)	1.0 (Gain=27dB)
Full well capacity	e-	17270	20960	30450	9700
Nonlinearity	w/o calibration	**0.26%**	**0.42%**	**0.18%**	**0.16%**
	w/ calibration	**0.058%**	**0.060%**		

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