Challenges in Improving the Performances of Radiation Hard CMOS Image Sensors for Gigarad (Grad) Total Ionizing Dose

Vincent Goiffon[1], Serena Rizzolo[1], Franck Corbière[1], Sébastien Rolando[1], Aziouz Chabane[1], Marius Sergent[1], Philippe Paillet[2], Sylvain Girard[3], Magali Estribeau[1], Pierre Magnan[1], Marco Van Uffelen[4], Laura Mont Casellas[4], Marc Gaillardin[2], Robin Scott[5] and Wouter De Cock[6]

[1]ISAE-SUPAERO, 10 avenue Edouard Belin, 31055 Toulouse, France
[2]CEA, DAM, DIF, Arpajon, France
[3]Université de Saint-Etienne, Laboratoire Hubert Curien, UMR-CNRS 5516, France
[4]Fusion for Energy (F4E), c/Josep Pla, n◦ 2, Torres Diagonal Litoral, Ed. B3, 08019 Barcelona, Spain
[5]Oxford Technologies Ltd.(OTL), 7 Nuffield Way, Abingdon OX14 1RL, UK.
[6]SCK-CEN, Boeretang 200, 2400 Mol, Belgium

Email: vincent.goiffon@isae.fr, Phone: +33 5 6133 8093

Disclaimer: The work leading to this publication has been funded partially by Fusion for Energy under specific contracts F4E-OMF-272-01-18 and F4E-OFC-358-2-01-01. This publication reflects the views only of the author, and Fusion for Energy cannot be held responsible for any use which may be made of the information contained therein.

I. Introduction

Solid-state high definition and color imagers with radiation hardness well above than a Total Ionizing Dose (TID) of 100 Mrad(SiO_2) are required for the development of critical remote handling systems in ITER fusion reactor (Fig. 1). The availability of such rad-hard imager would also completely transform the way remote handling and monitoring are performed in highly radioactive environments, by increasing operational efficiency, but also by reducing risks, costs and the frequency at which cameras are replaced. It would enable the inspection of radioactive areas that cannot be observed today. Typical applications that would greatly benefit from this solution are remote handled maintenance, monitoring and inspection operations in many nuclear facilities—such as nuclear power plant, nuclear storage waste repository, particles physics and irradiation facilities (e.g. CERN)—as well as mobile rescue robots.

This IISW proceeding paper discusses the main challenges to meet in order to develop a Gigarad-rad-hard-CMOS Image Sensors (CIS) with acceptable performances. The discussion is based on the most recent results obtained on the currently developed demonstrator for ITER remote handling (this development is described more in details in [1]) compared with previous work on different design and process variations [2], [3]. All the results reported here have been obtained on a standard 180 nm CIS technology.

Only conventional photodiode architectures (i.e. 3T pixels [4]) are considered here since ionizing radiation renders Pinned Photodiodes (PPD) [5], [6] unusable after several Mrad [2]. As regards irradiation conditions, ^{60}Co gamma ray and 10 keV X-ray sources have been used with different biasing conditions (ON or OFF) and for the main discussion developed here, these different irradiation conditions lead to comparable degradation at a given TID. Therefore, for the sake of clarity, irradiation conditions are not stated for each results discussed here

II. Main Challenges

Deep submicrometer CMOS transistors are often supposed to be intrinsically radiation tolerant and the use of enclosed geometries is not always relevant for low or moderate TID applications (such as space or medical applications). Especially the use of enclosed geometries is often not considered for P-channel transistors or for core (i.e. low voltage) MOSFETs.

For a targeted end-of-life TID between 100 Mrad and 1 Grad, the use of Enclosed Layout Transistors (ELT) [7] appears necessary on both N-channel and P-channel “low” (1.8 V) and “high” (3.3 V) voltage MOSFETs to mitigate the radiation induced narrow channel effect (RINCE [8]). Fig. 2 illustrates this first conclusion as it shows that after a few Megarad the tested standard P-MOSFET is not functional anymore whereas the ELT P-MOSFET after 300 Mrad can still be used.

Hence, by using appropriate radiation hardening by design techniques [9], basic analog and digital CMOS functions (combinatorial and sequential logic, amplifiers, multiplexers, I/O pads, ADCs...) can tolerate up to 1 Grad of TID without suffering critical failure (see Fig. 3 and 4 for illustrations).

Fig. 4 shows the remaining degradation measured on a CIS current source ELTs for different device type. As expected [9], when thinner gate oxide is used (1.8 V transistor compared to 3.3 V one), the radiation induced voltage shift is significantly reduced (about a factor of 4 reduction). However, 3.3 V N-channel transistors are less degraded than 1.8 V P-channel ones for higher TID than 300 Mrad.

As a consequence, for analog circuits, avoiding P-channel transistors and using N-channel 3.3 V MOSFETs as much as possible is an efficient solution (in this technology) to keep the radiation induced voltage shift acceptable and a wide linearity range between 100 Mrad and 1 Grad.

Thanks to their limited thickness, the optical properties of dielectric material typically used on top of CIS are not significantly degraded (see Fig. 5 and Fig.6 for an illustration of color filter array transmittance evolution with TID).

As a first conclusion, the main issues to solve are related to the pixel design and more precisely to the influence of photodiode design on the radiation induced Dark Current (DC) increase.

III. Reducing Dark Current

To identify the levers that can influence this DC increase, several technological options are explored (see Tab. I for a quick summary) alongside a few variants of the promising gate overlap design (discussed in [2]) as illustrated in Fig. 7.

In this particular design with a protective gate, the lowest dark current should be reached for a negative or low gate voltage (as in PPD pixels) when the gate channel in placed under accumulation. Such behavior is observed in Fig. 8, as expected, on the gate overlap design terminated by a P+ ring. If the gate voltage is increased beyond this optimum gate voltage, the dark current rise again in the P+ isolated pixel because of high electric field effects. On the contrary, in the pixel with only a gate isolation (Fig. 7b), increasing further the gate voltage reduces the measured dark current. The fact that the dark current shot noise (secondary Y axis in Fig. 8) also decreases with the dark current confirms that this phenomenon is a real reduction of dark current (not a simple subthreshold reset compensation current).

The radiation induced positive trapped charge leads to the creation of weak inversion channels at the interfaces of Shallow Trench Isolations (STI) that are all connected to in-pixel ELT outer drains (biased to VDD or a voltage close to VDD). In this configuration (illustrated by the drawing presented in Fig. 9), dark electrons generated at the STI interface as well as dark electrons generated at the gate oxide interface are more likely to be collected by the high voltage N+ drains than by the photodiode itself, then cancelling the dark current coming from these interfaces.

This DC cancellation mechanism [3] has limited unwanted effects on the CIS performances as far as the gate voltage stays low enough to prevent the reduction of the full well capacity.

Fig. 10 shows that the studied technological variations (Tab. I) also allow reducing the dark current by an additional order of magnitude compared to the results presented at 2015 IISW [2]. Best results in terms of absolute dark current level in the 100 Mrad – 1 Grad are achieved with a shallow diode, a 1.8 V reset voltage and a gate isolation (that enables the dark current cancellation mechanism).

On the other hand, the shallow diode does not provide a good radiation hardness when a higher operating voltage (i.e. 3.3 V) is used because of high electric field enhancement effects [10].

IV. Conclusion

Most of the radiation induced degradation occurring outside the pixel can be either mitigated or reduced enough by using radiation-hardening-by-design techniques to maintain the functionality and to achieve acceptable performances.

Dark current levels reached in the 100 Mrad – 1 Grad range on the studied radiation hardened photodiode designs are low enough to enable acceptable imaging performances with sufficient illumination conditions (which is the case of this particular development). However, in applications where light power is limited, further dark current increase would be beneficial. Future research will focus on mitigating further this limiting radiation induced dark current increase.

References

[1] V. Goiffon *et al.*, “Total Ionizing Dose Effects on a Radiation Hardened CMOS Image Sensor Demonstrator for ITER Remote Handling,” *Be Publ.*

[2] V. Goiffon *et al.*, “Toward Multi-MGy / Grad Radiation Hardened CMOS Image Sensors for Nuclear Applications,” in *Proc. IISW*, 2015.

[3] V. Goiffon *et al.*, “Radiation Hardening of Digital Color CMOS Camera-on-a-Chip Building Blocks for Multi-MGy Total Ionizing Dose Environments,” *IEEE Trans. Nucl. Sci.*, vol. 64, no. 1, pp. 45–53, Jan. 2017.

[4] E. R. Fossum, “CMOS image sensors: electronic camera-on-a-chip,” *IEEE Trans Electron Devices*, vol. 44, no. 10, pp. 1689–1698, Oct. 1997.

[5] N. Teranishi, A. Kohno, Y. Ishihara, E. Oda, and K. Arai, “An interline CCD image sensor with reduced image lag,” *Electron Devices IEEE Trans. On*, vol. 31, no. 12, pp. 1829–1833, Dec. 1984.

[6] E. R. Fossum and D. B. Hondongwa, “A Review of the Pinned Photodiode for CCD and CMOS Image Sensors,” *IEEE J Electron Devices Soc*, 2014.

[7] G. Anelli *et al.*, “Radiation tolerant VLSI circuits in standard deep submicron CMOS technologies for the LHC experiments: practical design aspects,” *IEEE Trans Nucl Sci*, vol. 46, no. 6, pp. 1690–1696, 1999.

[8] F. Faccio and G. Cervelli, “Radiation-induced edge effects in deep submicron CMOS transistors,” *IEEE Trans Nucl Sci*, vol. 52, no. 6, pp. 2413–2420, Dec. 2005.

[9] H. L. Hughes and J. M. Benedetto, “Radiation effects and hardening of MOS technology: devices and circuits,” *IEEE Trans Nucl Sci*, vol. 50, pp. 500–501, Jun. 2003.

[10] J. Bogaerts, B. Dierickx, and R. Mertens, “Enhanced Dark Current Generation in Proton-Irradiated CMOS Active Pixel Sensors,” *IEEE Trans Nucl Sci*, vol. 49, no. 3, pp. 1513–1521, Jun. 2002.

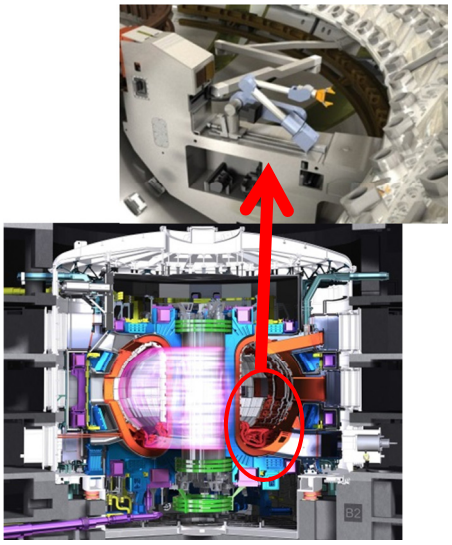

Fig. 1: Illustration of ITER fusion reactor and magnification of one of the in vessel remote handling systems for which rad-hard cameras are required.

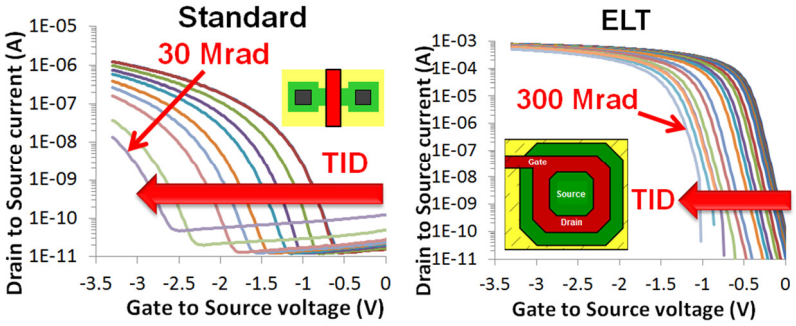

Fig. 2: Minimum size 3.3V P-MOSFET current-voltage characteristics evolution with TID (from 0 to 30 or 0 to 300 Mrad(SiO_2)) presented for a standard (open layout) and an radiation hardened (enclosed layout) transistor. The standard P-MOSFET layout suffers from a gate oxide positive trapped charge induced flatband voltage shift in addition to a RINCE induced voltage shift. This transistor is too degraded after 30 Mrad to enable the design of a Grad radiation tolerant CIS. On the other hand, the ELT design mitigates the RINCE effect in this PMOSFET and the remaining degradation after 300 Mrad is a 1 V threshold voltage shift due to the gate oxide positive trapped charge.

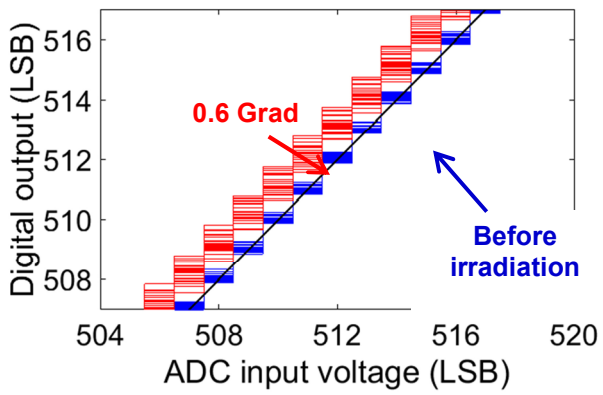

Fig. 3: Transfer function of 10 bit radiation hardened column Single-Slope ADCs manufactured with a 180 nm CIS process before and after exposure to ^{60}Co gamma-rays for a TID of 0.6 Grad(SiO_2). Differential and Integral Non Linearities (DNL and INL) degradations are below 2 LSB after 0.6 Grad.

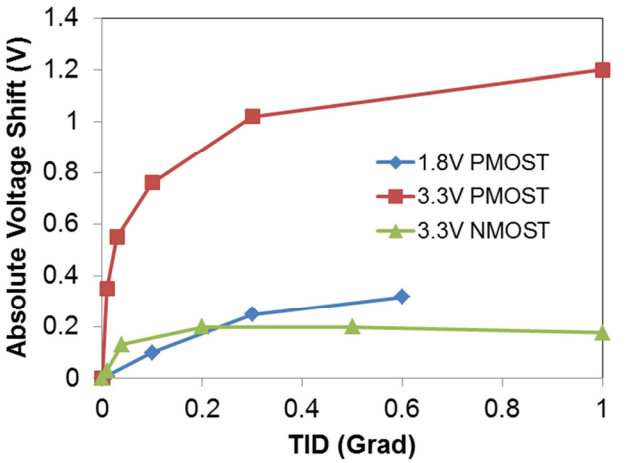

Fig. 4: Readout chain current source voltage shift as a function of TID for three MOSFET technology: 1.8V P channel MOSFET (thin gate oxide), 3.3V P channel MOSFET (with double gate oxide thickness) and 3.3 N channel MOSFET (with double gate oxide thickness). Using the thin gate oxide (1.8 PMOST) delays the degradation without reaching saturation whereas 3.3V NMOSFET degrades faster but saturates at 0.1-0.2 Grad leading to better performance beyond 0.3 Grad.

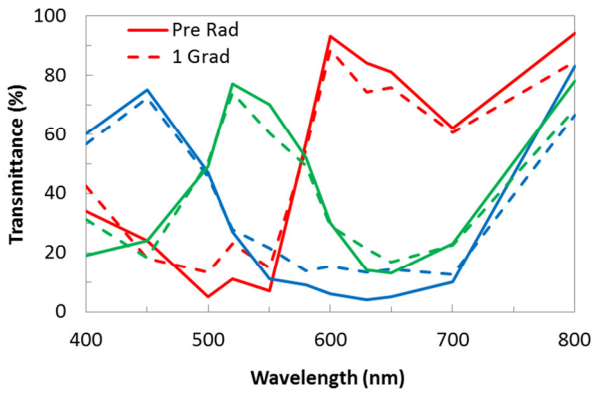

Fig. 5: Color Filter Array (CFA) transmittance before and after irradiation (TID = 1 Grad) showing that CFA degradation is negligible.

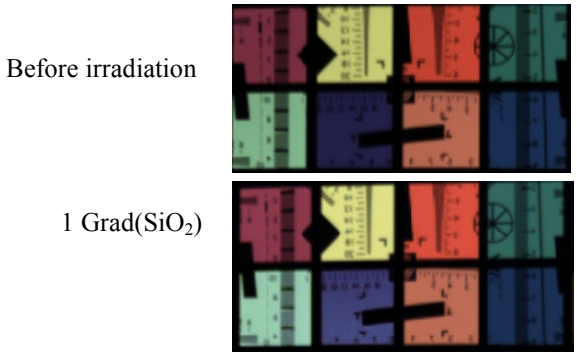

Fig. 6: Color image captured by a 256x128-pixel-rad-hard-CIS (RH CIS 2 with 3.3V N-MOSFETs for the analog functions) before (a) and after (b) the absorption of 1 Grad(SiO_2) of TID. This figure illustrates the good functionality of the rad-hard CIS and its ability to discriminate contrast and colors (with acceptable degradations) after 1 Grad.

Table I: Summary of the main technological differences between the studied radiation hardened CISs. Pixel array size varies between 128x128 and 256x256 pixels. All the studied imagers have been manufactured using a commercial 180 nm CIS process

	Photodiode type	Pixel voltage	Analog readout chain MOSFETS
RH CIS 1	Deep	3.3V	3.3V N&P
RH CIS 2	Deep	3.3V	3.3 N only
RH CIS 3	Shallow	3.3V	3.3 N only
RH CIS 4	Shallow	1.8V	1.8V N&P

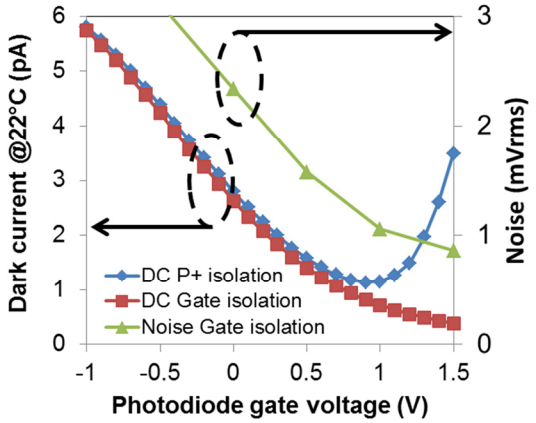

Figure 8: Dark Current (DC) as a function of surrounding gate voltage at 40 Mrad on a 3.3V pixel with a deep diode (CIS 2) for the two isolation cases depicted in Fig. 7. Total output noise (readout + dark current shot noise) is also presented for the gate isolation pixel on the second Y axis to demonstrate that the dark current is effectively cancelled (not just compensated) for gate voltage >0.6V.

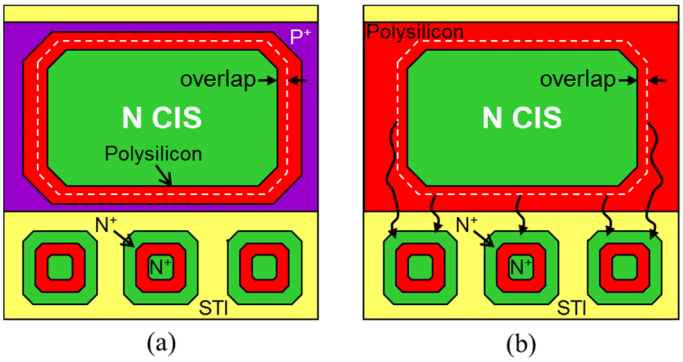

Fig. 7: Gate overlap pixel design top view illustrations with (a) a P+ isolation between photodiodes and (b) a gate isolation between photodiodes. Undulating arrows represent dark current cancelation paths.

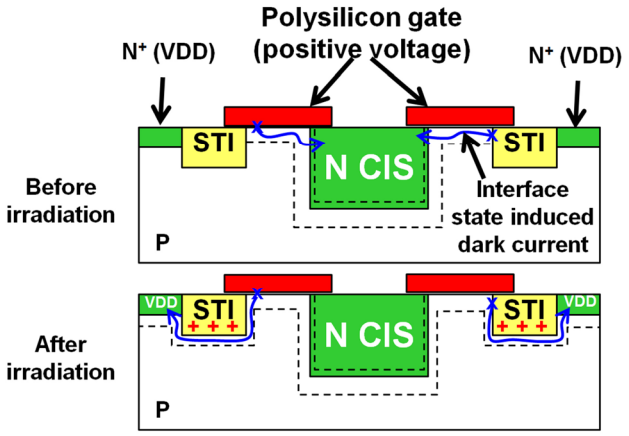

Figure 9: Illustration of the Dark Current (DC) cancelation mechanism in irradiated pixel with a gate isolation. After irradiation, dark electrons generated in the gate depleted region are collected by the nearest N+ VDD contacts (in-pixel MOSFET drains) through the STI interface (weakly inverted because of radiation induced positive trapped charge) with no influence on the photocurrent.

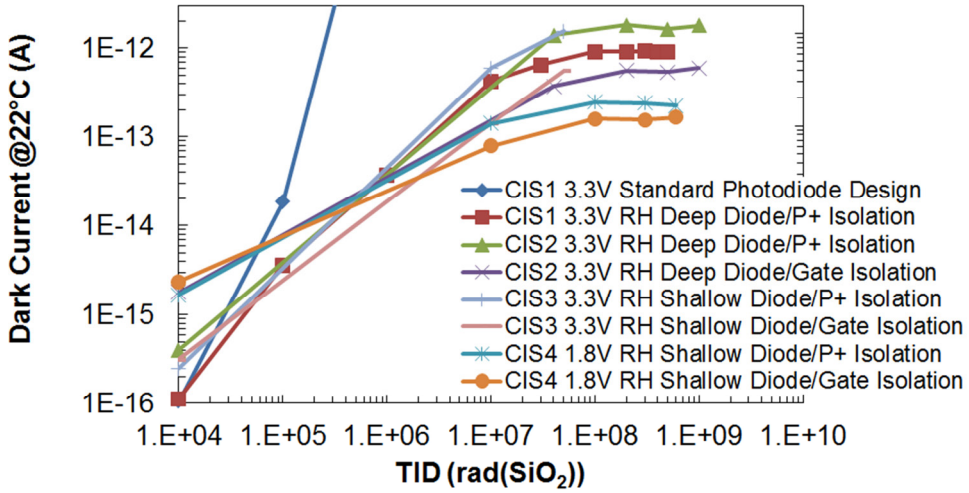

Figure 10: Dark current evolution with TID for the different technologies and designs studied. Best results in the Grad range are obtained with the shallow diode with 1.8V operating voltage and a gate isolation between photodiode to enable the dark current cancellation mechanism highlighted in Fig. 8 and 9.