A Fully Depleted 52 µm GS CIS Pixel with 6 ns Charge Transfer, 7 e^-_{rms} Read Noise, 80 µV/e^- CG and >80 % VIS-QE

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Abstract **– Imec is developing a CMOS compatible platform for fully depleted image sensors. Full depletion allows enhancement of the charge collection speed, signal detectivity and sensitivity in photodetectors. A 48x48 pixel test array with 52 µm pitch has been developed in this technology. An initial evaluation is presented in this paper. The device achieves 7 e^-_{rms} read noise at 80 µV/e- conversion gain. The mean charge transfer time is estimated to 6 ns. QE in the visible is expected to be >80 %.**

I. Introduction

Fully depleted CMOS image sensors are attractive for many advanced applications including direct soft X-ray detection [1-5], time-of-flight [6,7] and ultra-high speed imaging [8, 9]. A distinct benefit of fully depleted detectors is the combination of a large detection volume [1-9] and strong electric fields, offering both high sensitivity and fast photocarrier transport. At imec, a new technology to exploit these advantages in a CMOS compatible manner was developed. This allows monolithic integration of in-pixel readout electronics thereby enabling state-of-the-art performance in speed, detectivity and sensitivity.

II. Device Technology Description

A cross-section of the proposed technology is depicted in Fig.1. The photodetector consists of a fully depleted substrate, which is achieved by dedicated doping profile design as well as the application of a sufficiently large voltage difference between the floating diffusion (FD) junction and a backside contact. The in-pixel readout circuit is embedded inside a dedicated pWell. Additionally, electronics for, e.g. readout are embedded in standard 0.13 µm CMOS nWells and pWells, which are insulated from the epitaxial layer by means of a deep pWell implant. Thereby, 1.2V and 3.3V devices can be employed. The pixel area is shielded from the CMOS area by a n-guard ring to avoid transport of carriers generated below the CMOS area towards the pixel area.

Applying a back bias to conventional CMOS image sensor technology will result in resistive leakage current over the epitaxial layer and respective back contact. In order to circumvent this issue,

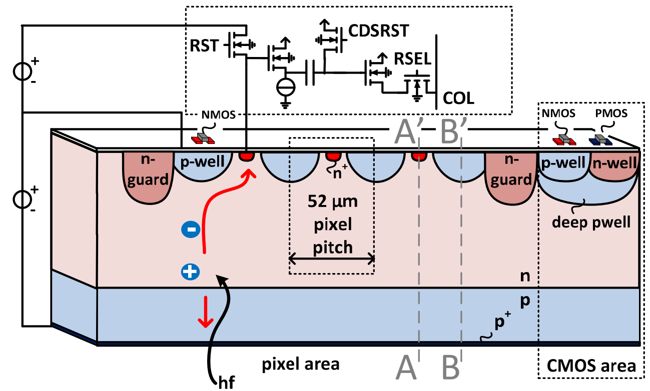

Figure 1: Device cross-sectional view.

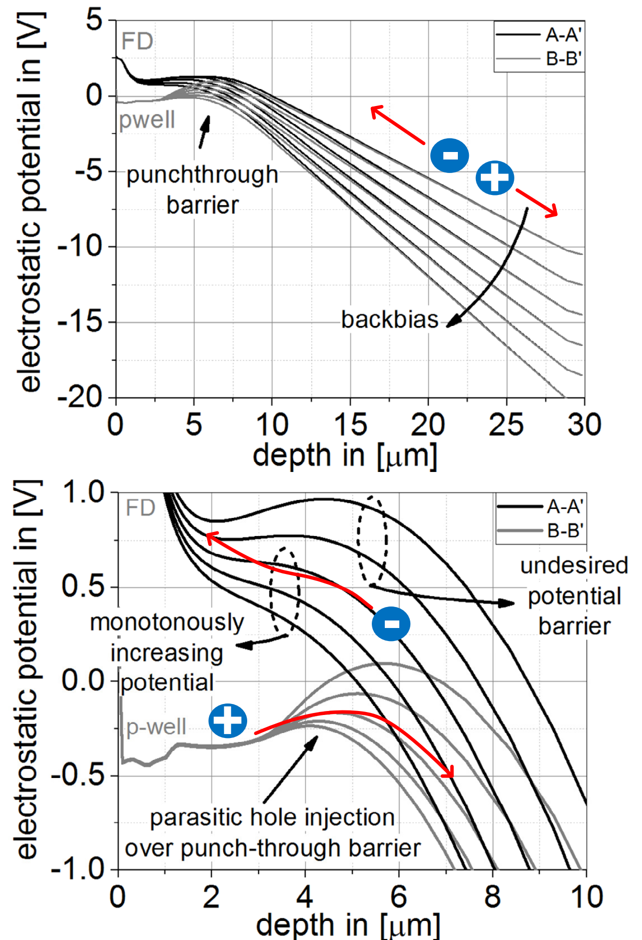

Figure 2: Exemplary electrostatic potential profiles through cuts A-A' and B-B' of Fig.1 (top: full epi, bottom: zoom)

Imec developed various implementations of built-in potential barriers [8, 9]. Exemplary cross-sectional views through pWell, built-in barrier and epitaxial layer (B-B') as well as through FD and epitaxial layer (A-A') are depicted in Fig. 2. The upper subfigure illustrates that photo-generated carriers are separated – holes are accelerated towards the back-contact; electrons to either the FD or towards the built-in local potential maxima. As the built-in potential barrier is graded towards the FD, carriers will swiftly migrate to the FD as well. The lower sub-figure illustrates that majority carriers of the top pWell – that embeds the readout electronics – can overcome the built-in potential barrier more likely if the back bias is increased. A trade-off between punch-through current and leakage current has to be made. Fig. 3 illustrates electrostatic simulation of the device by TCAD. At, e.g. -21V back bias and 2-3V at the FD full-depletion and a monotonic profile are yielded. Here, a punch-through current of 12 nA results. Charge transfer time distributions were estimated by forward Euler integration of injected electrons into the velocity field distribution. These were yielded from the electrostatic simulation at the minimum bias voltage needed for monotony and full depletion. The performed simulations show that the device allows vertical transfer of 30 µm below 1 ns. The bottleneck is the acceleration of the electrons through the graded potential maxima of the built-in barrier.

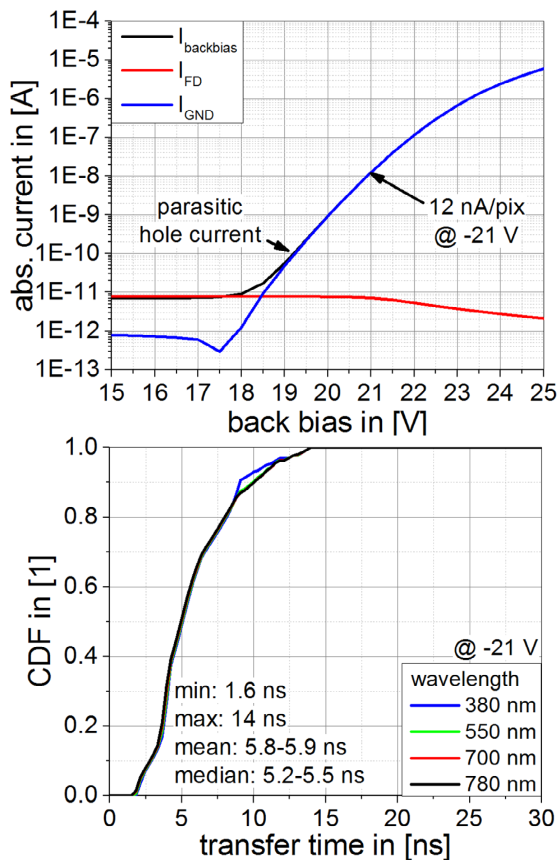

Figure 3: . IV characteristics of detector under everse bias (top) (TCAD) transfer time distribution vs. wavelength (bottom) (TCAD).

This implies that the transfer time is almost wavelength independent as depicted in Fig.3. For the described device with 52 µm pixel pitch, a mean transfer time of about 6 ns is expected. Carriers generated in the corners of the pixel require up to 14 ns for transfer towards the FD. At full depletion, the detector capacitance is dominated by the sidewall capacitance (Fig. 4). As the BEOL also contributes significantly to the sense node capacitance, BEOL and detector have been co-designed to optimize detectivity (Fig. 5). In order to allow for high speed global shutter operation, a capacitively coupled CDS stage [10, 11] has been implemented. Currently, the read noise is limited by the kT/C contribution of the CDS stage.

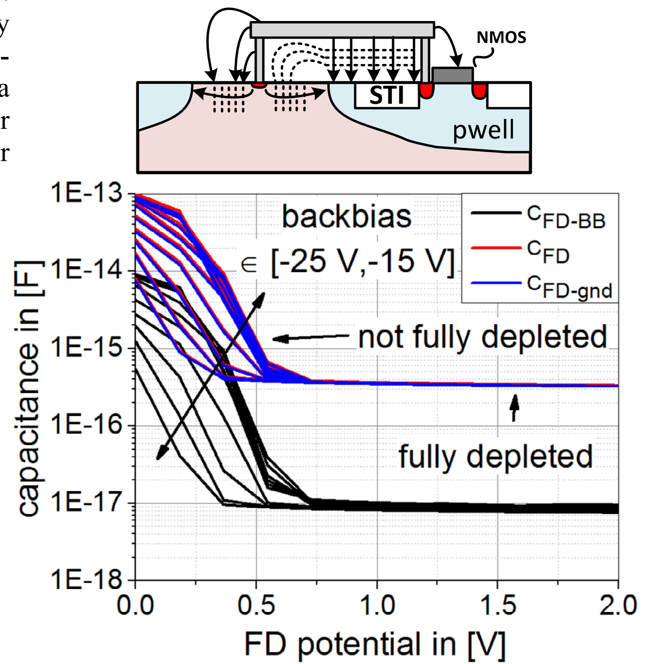

Figure 4: Cross-sectional view of sense node (top) detector junction capacitance vs. bias (bottom) (TCAD).

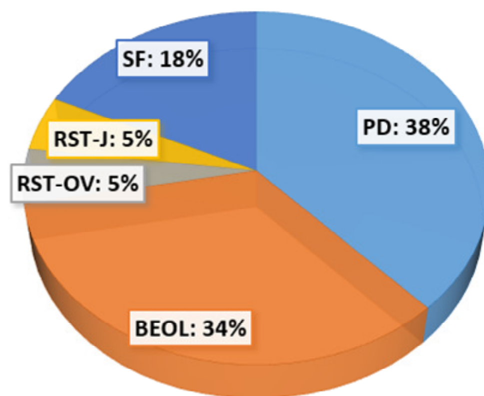

Figure 5: Sense node capacitance contributions (simulation).

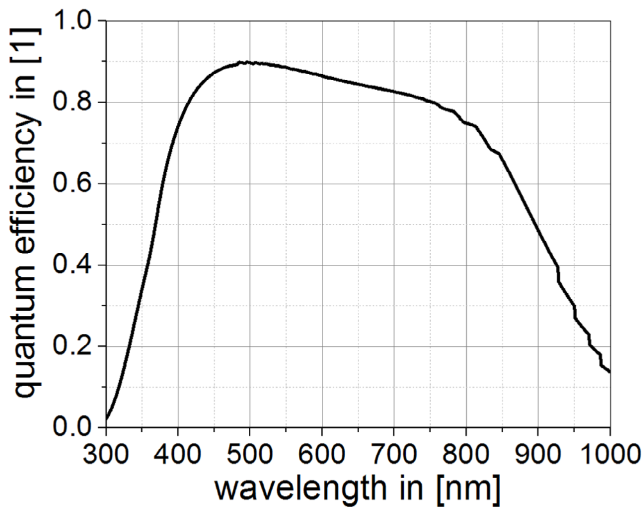

Figure 6: Quantum efficiency vs. wavelength (simulation).

Expected quantum efficiency is given in Fig. 6. The 30 µm epitaxial layer ensures high collection efficiency in red and infrared. The efficiency in UV and blue is limited by the backside interface and contact quality. The 50 nm SiN anti-reflective coating limits the peek quantum efficiency to about 90 %. For higher sensitivity in UV, imec offers dedicated coatings yielding 50-70 % peak QE between 250-300 nm [13].

III. Device Evaluation

The pixel concept was implemented in a 48x48 pixel test vehicle (Fig. 7 left). A picture captured by projecting a USAF resolution target onto the sensor is depicted in Fig. 7 (right).

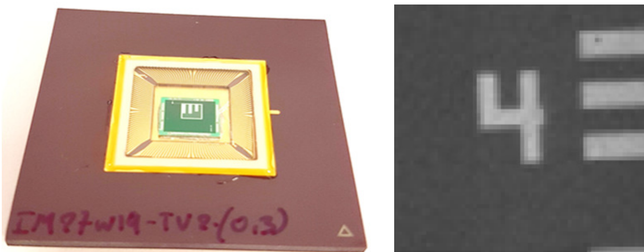

Figure 7: Test vehicle microphotograph (left) and image of a projected USAF resolution target (right).

Fig. 8 depicts pixel-wise input referred photon transfer curve measurements. An FD referred conversion gain of 80 µV/e^- has been extracted. The noise level amounts to ~7 e^-_{rms}. Saturation occurs at 10 ke^-. It is limited by the voltage swing the readout circuit can handle. In addition, the swing is limited by the minimum required potential at the FD to ensure full depletion and fast carrier transport. As the pWell is biased at 0 V, the FD should be operated at 2 V

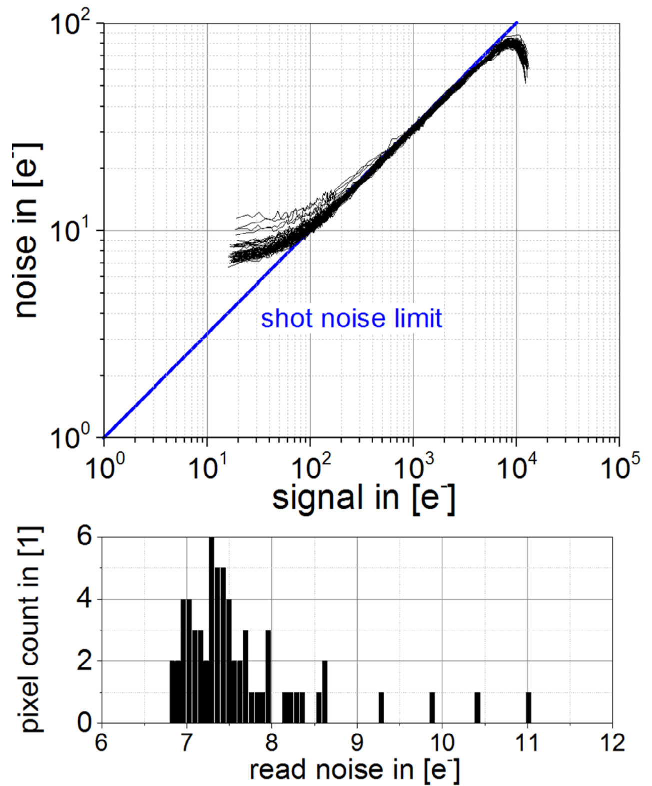

Figure 8: Measured photon transfer curves (top) and input referred noise distribution with median of 7 e^-_{rms} (bottom).

minimum in order to yield transfer characteristics as given in Fig.3 and 3.3 V maximum to be CMOS compatible. The charge transfer speed was evaluated using a pulsed light response measurement [12]. During the measurement a light pulse that is synchronized to the integration time window with an accuracy of ~1 ns is imaged. In a first order approximation the photocurrent can be understood as the convolution of laser pulse shape and detector impulse response function. Changing the relative time difference between laser excitation and integration time will result in partial integration of the convoluted laser response (Fig.9). Therefore, the rising and falling edges are indicative of the sensor speed. Additionally, jitter and circuit response impact the measurement. A pulsed 349 nm QP-DPSS laser having ~10 ns FWHM was used (Fig. 9). The jitter amounts to ~1 ns and is limited by an asynchronous interface used in the communication between the laser driver and the sequencer. The circuit impulse response function was simulated to amount to ~40 ns. As can be seen in Fig. 9, rising and falling edge are about ~50-60 ns, being in line with above explanation.

Table 1: State of the art overview.

	Sensor Creations [5]	Espros, OpenUniv. [7]	OpenUniv. [4]	Microsoft [6]	Univ. Bonn, Espros [2]	Univ. Bonn, Lfoundry [3]	Ritsumeikan Univ., Astrodesign, Osaka Univ., TU Delft, imec [8]	imec [9]	**imec this work**
pitch	15 µm	40 µm	10 µm	10 µm	40 µm	33 µm x 125 µm	15 µm	10 µm	**52 µm**
GS	yes	Yes	no	yes	no	no	yes	no	**Yes**
FWC	10 ke-	200 ke-	15 ke-	100 ke-	n.a.	n.a.	n.a.	8 ke-	**10 ke-**
CG	n.a.	27 µV/e-	80 µV/e-	26 µV/e-	100 µV/e- (amplified)	8 µV/e- amplified	n.a.	75 µV/e-	**80 µV/e- (@ FD)**
linearity	n.a.	n.a.	n.a.	n.a.	n.a.	n.a.	n.a.	n.a.	**< 5%**
σ_{read}	10 e-	12 e-	8 e-	12.3 e-	30 e-rms	120 e-	n.a.	15 e-	**7 e-**
speed	100 ns TINT	n.a.	n.a.	130 MHz	1 µs discharge time	~25 ns	~1 ns	n.a.	**typ. 6 ns (TCAD)**
epi	200 µm	50 µm	18 µm	n.a.	50 µm	n.a.	30 µm	n.a.	**30 µm**

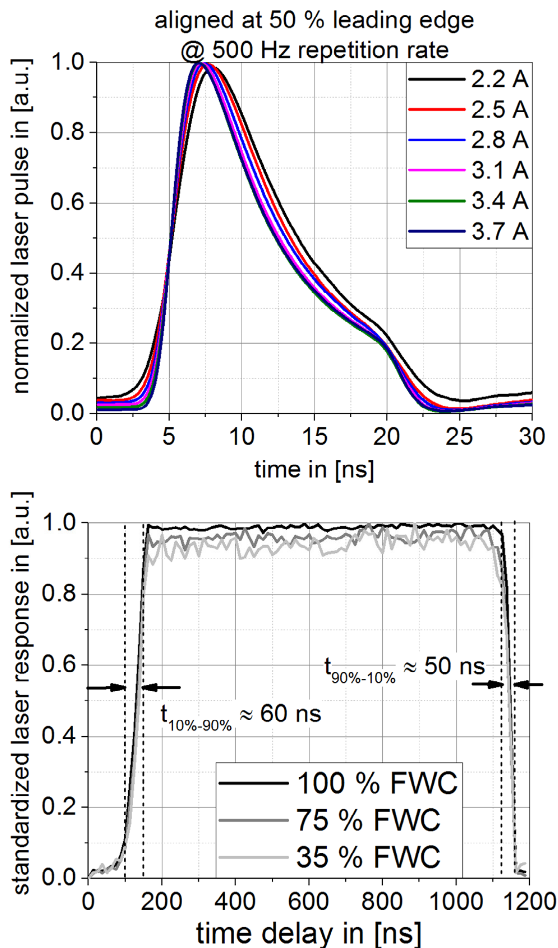

Figure 9: Measured laser source pulse shape using a 1 GHz high-speed photoreceiver (top) and measured sensor pulse response vs. relative delay between integration time and laser trigger (bottom).

IV. Conclusion

Table 1 summarizes the performance and compares it to published fully depleted CIS. Our pixel technology achieves a state-of-the-art trade-off in the speed, detectivity and sensitivity, which is of key importance to advanced imaging applications such as single photon X-ray detection, time-of-flight and ultra-high-speed imaging.

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